

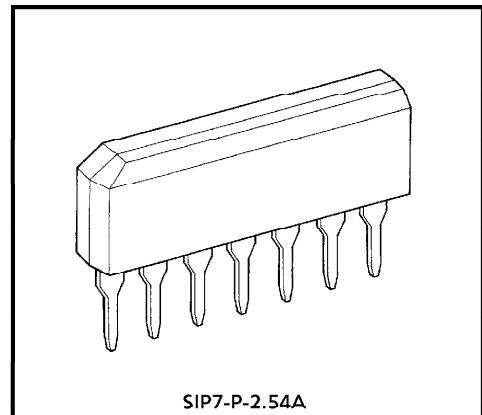
TA8749S

4 f_{sc} CLOCK GENERATOR

The TA8749S provides the function for CCD clock driver, and generate 4 times frequency signal of the input f_{sc} signal by PLL Circuit.

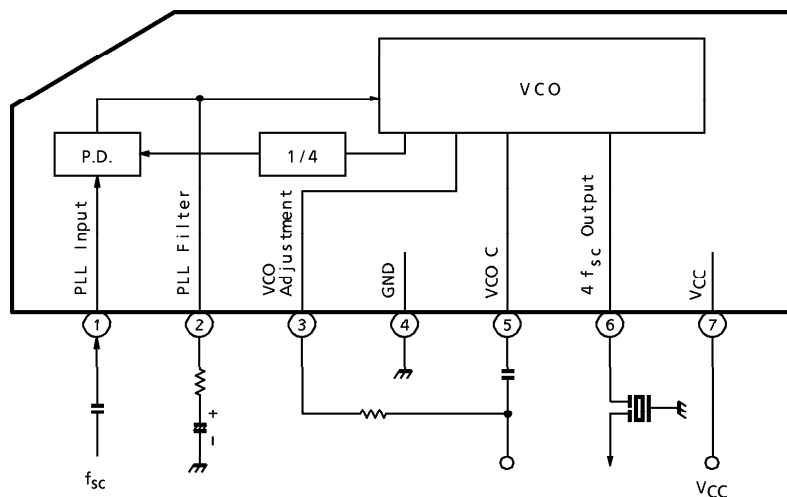
FEATURES

- 4 f_{sc} VCO
- Phase comparator



SIP7-P-2.54A
Weight : 0.72g (Typ.)

BLOCK DIAGRAM



961001EBA2

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	15	V
Input Signal Level	e _{in}	5	V _{p-p}
Power Dissipation	P _D (Note)	400	mW
Operating Temperature	T _{opr}	- 20~65	°C
Storage Temperature	T _{stg}	- 55~150	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 4mW for each increase of 1°C.

ELECTRICAL CHARACTERISTICS

DC characteristics (Unless otherwise specified, V_{CC} = 9V, Ta = 25°C)

PIN No.	PIN NAME	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	PLL Input	V ₁	—	—	4.2	4.5	4.8	V
2	PLL Filter	V ₂	—	—	3.1	3.6	4.1	V
3	VCO Adjustment	V ₃	—	—	4.4	4.6	4.8	V
4	GND	—	—	—	—	0	—	V
5	VCO C	—	—	—	—	—	—	V
6	4 f _{sc} Output	V ₆	—	—	—	6.5	—	V
7	V _{CC}	—	—	—	—	9	—	V
7	V _{CC}	I ₇	—	—	9	11	15	mA

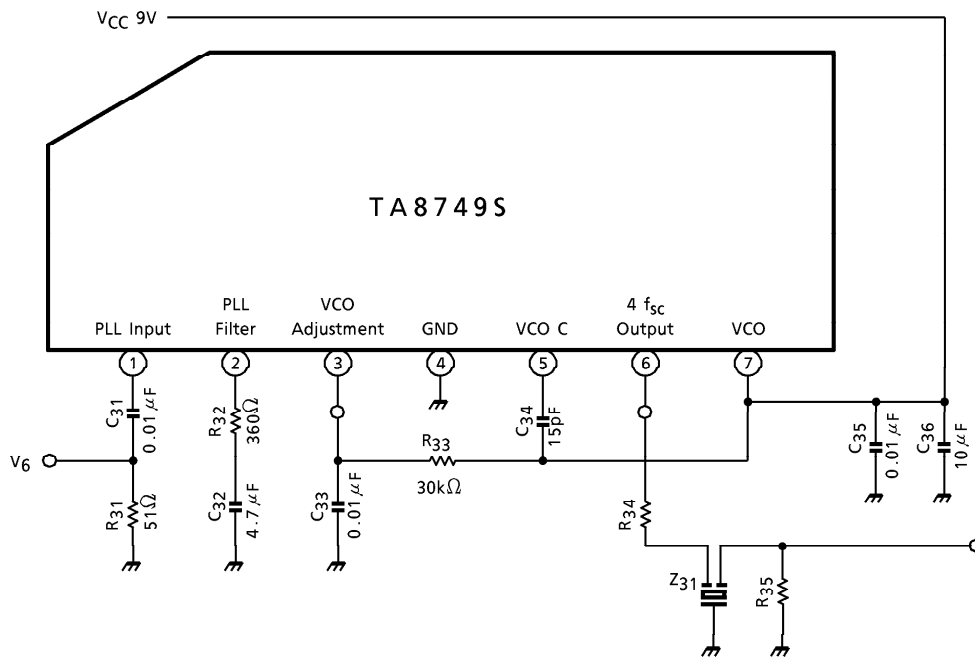
AC characteristics (Unless otherwise specified, V_{CC} = 9V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
4 f _{sc} Level	Pin 6	V ₆	—	(Note 1)	1.0	1.5	2.0	V _{p-p}
	Pin 5	V ₅			0.4	0.5	0.6	
VCO Variable Range	High	f _{ch}	—	(Note 2)	15.3	18.0	—	MHz
	Low	f _{cl}			—	11.0	13.3	
Input Sensitivity	V _i	—	—	(Note 3)	—	—	0.1	V _{p-p}
PLL Pull-in Range	High	f _{ph}	—	(Note 4)	3.78	3.90	—	MHz
	Low	f _{pl}			—	3.20	3.38	
f _{sc} Leak Level	f _s	—	—	(Note 5)	50	60	—	dB

TEST CONDITION

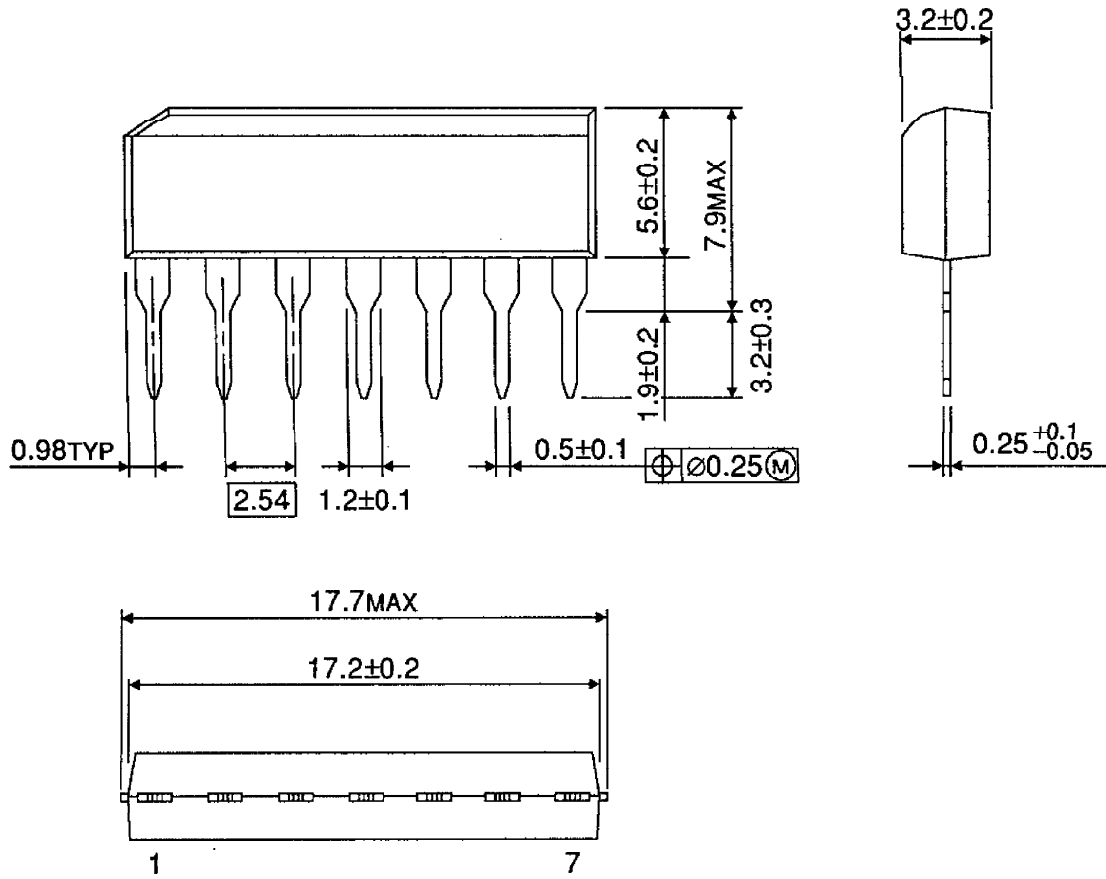
NOTE No.	ITEM		MEASUREMENT CONDITION ($V_{CC} = 9.0V, T_a = 25^{\circ}C$)	
			SW & VR MODE	MEASUREMENT METHOD
1	4 f_{SC} Level	Pin 6	—	(1) No signal input (2) Measure amplitude of 4 f_{SC} at pin 6 and pin 5.
		Pin 5	—	
2	VCO Variable Range	High	—	(1) No signal input (2) Measure the frequency of output signal at pin 6. (3) Measure the frequency at each mode. ① Pin 2 = 7.5V ② Pin 2 = 1.5V
		Low	—	
3	Input Sensitivity		—	(1) V_6 input : $f_o = 3.58MHz$ level variable (2) Monitor pin 6 output wave form. Change the input level higher, and get the level to pull-in.
4	PLL Pull-in Range	High	—	(1) V_6 input : $f = \text{sweep}, 300mV_{p-p}$ CW (2) Change the input frequency ① \rightarrow high ② \rightarrow Low, and get the frequency to pull-in by sweeping.
		Low	—	
5	f_{SC} Leak Level		—	(1) V_6 input : $f_o = 3.58MHz, 300mV_{p-p}$ CW (2) Monitor pin 6 output, and calculate $14.32MHz / 3.58MHz$.

TEST CIRCUIT



OUTLINE DRAWING
SIP7-P-2.54A

Unit : mm



Weight : 0.72g (Typ.)