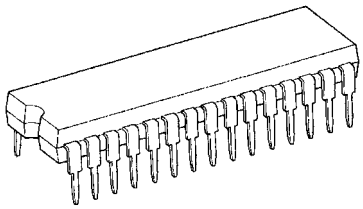
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8772AN

PAL / SECAM / NTSC BASE BAND 1H DELAY SYSTEM FOR COLOR TV OR VCR

The TA8772AN has two chips, a bipolar chip and a CCD chip, in a package.
CCD chip consist of two delaylines which operate to delay R-Y and B-Y signal. Bipolar chip operate to control the signals which is processed by CCD stage.



SDIP30-P-400-1.78

Weight: 1.99g (Typ.)

FEATURES

Bipolar stage

- AGC circuit (For correcting output level)
- L.P.F. (For reducing CCD clock)
- DC clamp circuit (For reducing the difference of DC l vel between delay signal and direct ignal.)
- Mode SW (For control output signal by PAL, NTSC or SECAM ident)
- 225f_H VCO circuit (For making CCD clock)

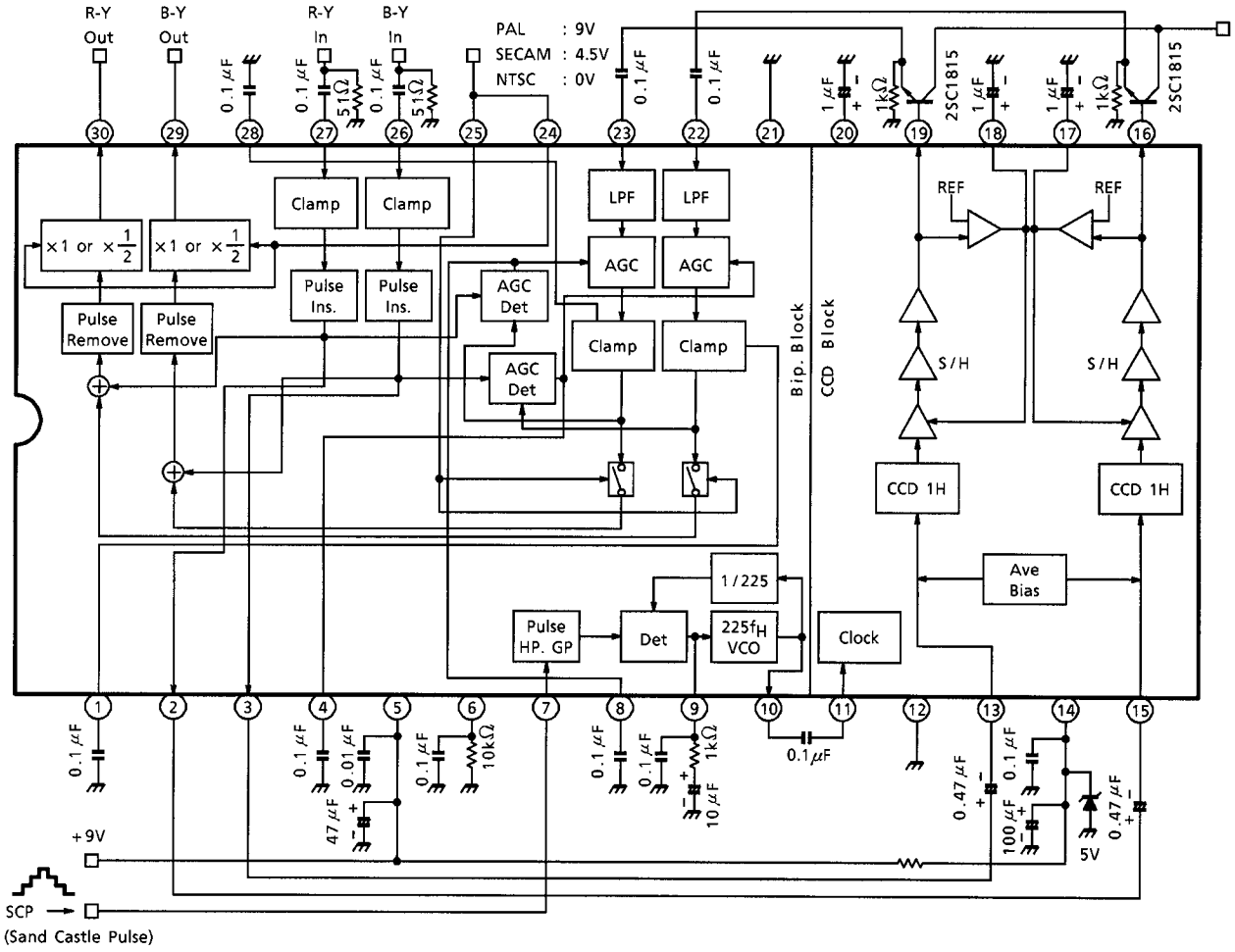
CCD stage

- CCD drive circuit
- Sample & Hold circuit
- Input bias circuit
- Synctip clamp circuit (This device's dynamic range bear no relation to change of APL on adopt this circuit)
- Delay time of 1H consist of supply 225f_H clock.

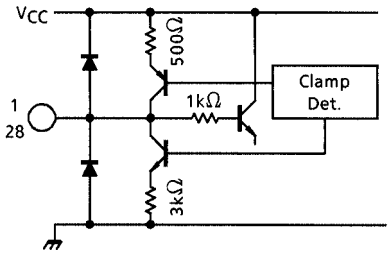
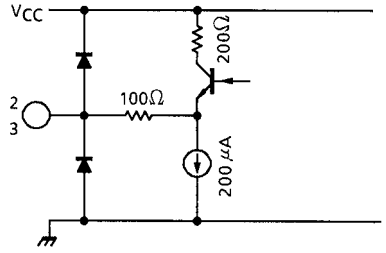
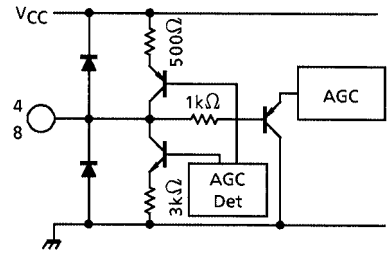
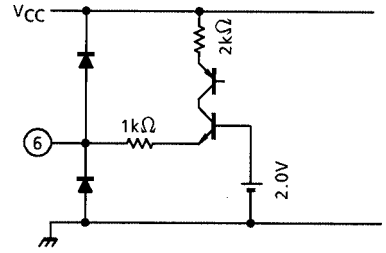
TOTAL

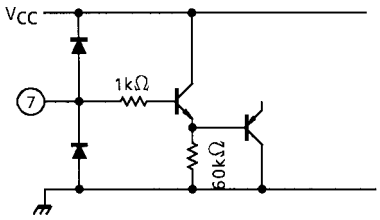
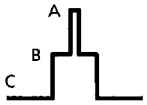
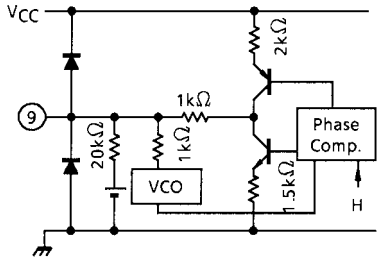
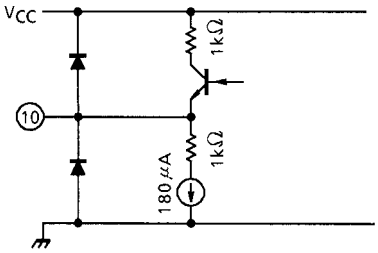
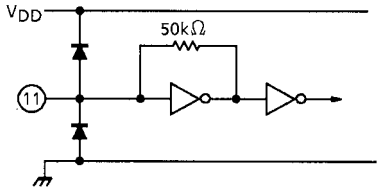
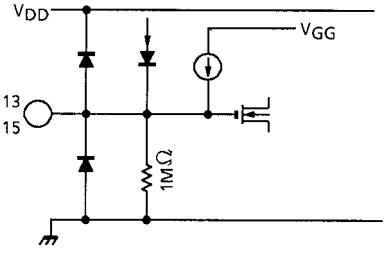
- This device can operate by the smallest external parts because of include CCD drive circuit, bias generator circuit and output amplifier for support CCD circuit.

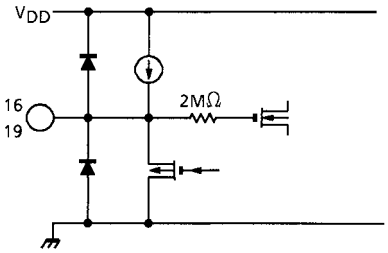
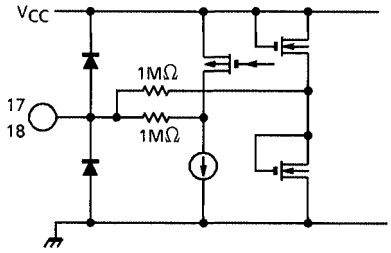
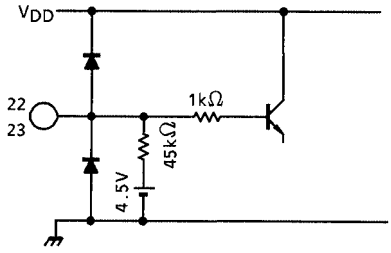
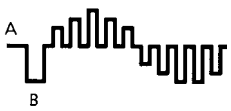
BLOCK DIAGRAM

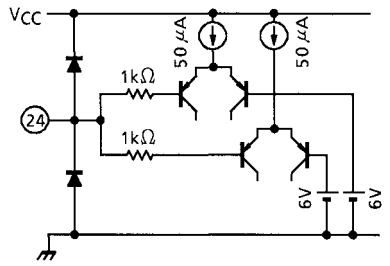
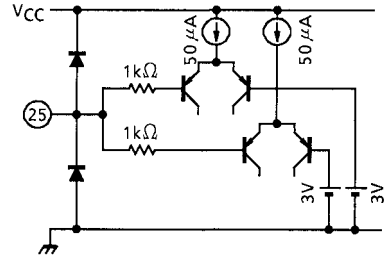
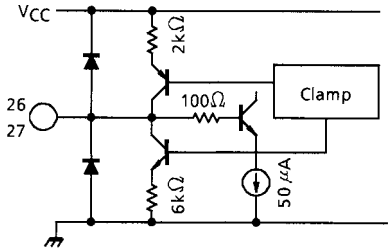
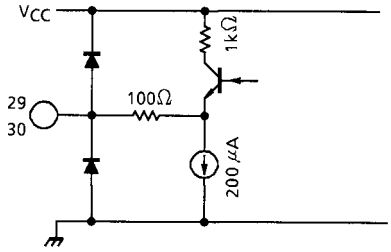


TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	TERMINAL SIGNAL
1	R-Y Clamp Det.	This is a terminal for detecting DC clamp level of R-Y signal.		DC 4.5V
28	B-Y Clamp Det.	This is a terminal for detecting DC clamp level of R-Y signal.		
2	R-Y to CCD	This is output terminal of R-Y signal. This terminal connects to pin 15 of CCD circuit.		 160mVp-p A : 4.30V B : 4.55V
3	B-Y to CCD	This is output terminal of B-Y signal. This terminal connects to pin 13 of CCD circuit.		 180mVp-p A : 4.30V B : 4.55V
4	R-Y AGC Det.	This is terminal for detecting AGC.		DC 3.9V
8	B-Y AGC Det.	This is terminal for detecting AGC.		
5	V_{CC}	This is power supply terminal for supplying 9V (Typ.) to bipolar circuit.	—	—
6	Filter Adj.	This terminal is connected to GND via 10kΩ, This is terminal for adjusting internal filter.		DC 1.3V

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	TERMINAL SIGNAL
7	S.C.P. In	This is input terminal for S.C.P.		 A : 7.80V B : 4.45V C : 0.40V
9	PLL Det.	This terminal outputs result of phase comparison between internal VCO and horizontal input signal.		DC 4.2V
10	Clock	This terminal outputs clock pulse which is used by CCD circuit.		 $0.4V_{p-p}$ DC 2.3V
11	Clock In	This terminal receives clock pulse for CCD circuit.		 $0.4V_{p-p}$ DC 2.3V
12	V_{SS}	This terminal is V_{SS} terminal for CCD circuit. Connect this terminal to GND.	—	—
13	V_{IN1}	This is input terminal of B-Y signal for CCD circuit		 $180mV_{p-p}$ A : 2.50V B : 2.25V
15	V_{IN2}	This is input terminal of B-Y signal for CCD circuit		 $160mV_{p-p}$ A : 2.50V B : 2.25V

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	TERMINAL SIGNAL
14	V_{DD}	This terminal is power supply terminal for supplying 5V (Typ.) to CCD circuit.	—	—
16	V_{OUT2}	This terminal outputs delayed signal of R-Y.		 230mV$_{p-p}$ A : 3.50V B : 3.15V
19	V_{OUT1}	This terminal outputs delayed signal of B-Y.		 270mV$_{p-p}$ A : 3.50V B : 3.15V
17	V_{OB2}	This terminal controls output DC level of pin 16.		DC 1.5V
18	V_{OB1}	This terminal controls output DC level of pin 19.		
20	V_{GG}	This terminal is applied V_{CC}×2 voltage by internal voltage booster.	—	DC 10.5V
21	GND	This terminal is GND terminal for bipolar circuit.	—	—
22	R-Y from CCD	This is input terminal of delayed R-Y signal.		 230mV$_{p-p}$ A : 4.50V B : 4.15V
23	B-Y from CCD	This is input terminal of delayed B-Y signal.		 270mV$_{p-p}$ A : 4.50V B : 4.15V

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT	TERMINAL SIGNAL
24	MODE SW_1	This terminal controls the gain of internal circuit for PAL, SECAM or NTSC. Threshold level is 6V (Typ.).		DC PAL :8.3V SECAM :4.6V NTSC :0.0V
25	MODE SW_2	This terminal controls sw of calculator for delayed signal and direct signal. Threshold level is 3V (Typ.).		DC PAL :8.3V SECAM :4.6V NTSC :0.0V
26	B-Y In	This is input terminal of B-Y signal.		 350mV$_{p-p}$ DC : 5.25 V
27	R-Y In	This is input terminal of R-Y signal.		 320mV$_{p-p}$ DC : 5.25 V
29	B-Y Out	This is output terminal of B-Y signal.		 350mV$_{p-p}$ DC : 4.55 V
30	R-Y Out	This is output terminal of R-Y signal.		 320mV$_{p-p}$ DC : 4.55 V

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC} / V_{DD}	12 / 6	V
Power Dissipation	P_D (Note)	1.6	W
Operating Temperature	T_{opr}	−20~65	°C
Storage Temperature	T_{stg}	−55~150	°C
Input Signal Voltage	e_{in}	0.8	V_{p-p}
Terminal Voltage	V_{in} / CCD	GND − 0.3~V_{CC} + 0.3 / GND − 0.3~V_{DD} + 0.3	V

Note: When using the device at above Ta = 25°C, decrease the power dissipation by 12.8mW for each increase of 1°C.

RECOMMENDED OPERATING CONDITION

PIN No.	PIN NAME	MIN	TYP.	MAX	UNIT
5	V_{CC} (Bip.)	8.1	9.0	9.9	V
14	V_{DD} (CCD)	4.75	5.0	5.25	V

ELECTRICAL CHARACTERISTICS

DC characteristics

Bipolar electrical characteristics (Unless otherwise specified, V_{CC} = 9V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Current		I_{CC}	—	(Note B1)	17.7	25.0	32.3	mA
Terminal Voltage	Pin 1	V_1	—	(Note B2)	3.95	4.50	5.05	V
	Pin 2	V_2		(Note B2)	4.28	4.50	4.72	
	Pin 3	V3		(Note B2)	4.28	4.50	4.72	
	Pin 4	V_4		(Note B3)	2.85	4.50	6.15	
	Pin 6	V_6		(Note B4)	1.157	1.300	1.443	
	Pin 8	V_8		(Note B3)	2.85	4.50	6.15	
	Pin 9	V_9		(Note B4)	1.82	2.15	2.48	
	Pin 10	V_{10}		(Note B4)	1.82	2.15	2.48	
	Pin 22	V_{22}		(Note B5)	4.28	4.50	4.72	
	Pin 23	V_{23}		(Note B5)	4.28	4.50	4.72	
	Pin 26	V_{26}		(Note B2)	4.98	5.20	5.42	
	Pin 27	V_{27}		(Note B2)	4.98	5.20	5.42	
	Pin 28	V_{28}		(Note B2)	3.95	4.50	5.05	
	Pin 29	V_{29}		(Note B6)	4.28	4.50	4.72	
	Pin 29 Difference	dV_{29}		(Note B6)	−0.005	0	0.005	
	Pin 30	V_{30}		(Note B7)	4.28	4.50	4.72	
	Pin 30 Difference	dV_{30}		(Note B7)	−0.005	0	0.005	

CCD DC electrical characteristics (Unless otherwise specified, V_{DD} = 5V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Current		I_{CC}	—	(Note C1)	4.0	12.0	24.0	mA
Terminal Voltage	Pin 11	V_{11}	—	(Note C2)	1.8	2.5	3.3	V
	Pin 13	V_{13}		(Note C2)	1.4	2.4	3.4	
	Pin 15	V_{15}		(Note C2)	1.4	2.4	3.4	
	Pin 16	V_{16}		(Note C2)	2.4	3.1	4.1	
	Pin 17	V_{17}		(Note C2)	0.5	1.3	2.1	
	Pin 18	V_{18}		(Note C2)	0.5	1.3	2.1	
	Pin 19	V_{19}		(Note C2)	2.4	3.1	4.1	
	Pin 20	V_{20}		(Note C2)	9.0	10.5	12.0	

AC characteristics
Bipolar electrical characteristics (Unless otherwise specified, V_{CC} = 9V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Dynamic Range	B-Y in (26)	D_{R1}	1	(Note B8)	1.3	1.4	1.5	V_{p-p}
	R-Y in (27)	D_{R2}		(Note B9)	1.3	1.4	1.5	
Linearity	B-Y in (26)	L_{ty1}	1	(Note B10)	−2.0	0.0	2.0	%
	R-Y in (27)	L_{ty2}		(Note B11)	−2.0	0.0	2.0	
Output Level	pin 2	V_{o1}	1	(Note B12)	0.39	0.40	0.41	V_{p-p}
	pin 3	V_{o2}		(Note B13)	0.39	0.40	0.41	
Pulse Insert Level	pin 2	P_{IL1}	1	(Note B14)	0.225	0.25	0.275	V
	pin 3	P_{IL2}		(Note B15)	0.225	0.25	0.275	
RP Pulse Delay Time		R_{PD}	1	(Note B16)	0.00	0.70	1.00	μs
L.P.F. f_0 (1)		F_{f01}	1	(Note B17)	1.50	1.60	1.70	MHz
L.P.F. f_0 (2)		F_{f02}	1	(Note B18)	1.50	1.60	1.70	MHz
TRAP f_0 (1)		T_{f01}	1	(Note B19)	3.20	3.40	3.55	MHz
TRAP f_0 (2)		T_{f02}	1	(Note B20)	3.20	3.40	3.55	MHz
TRAP Attenuation Value 1		T_{at1}	1	(Note B21)	—	−40	−30	dB
TRAP Attenuation Value 2		T_{at2}	1	(Note B22)	—	−40	−30	dB
Input Inpedance	Pin 22	Z_{i1}	1	(Note B23)	34.0	50.5	67.0	kΩ
	Pin 23	Z_{i2}		(Note B24)	34.0	50.5	67.0	
SW_1 Threshold Voltage		V_{th1}	1	(Note B25)	5.9	6.0	6.1	V
SW_2 Threshold Voltage		V_{th2}	1	(Note B26)	2.9	3.0	3.1	V
VCO Center Frequency		f_{cen}	1	(Note B27)	2.45	3.50	4.60	MHz
VCO Max Oscillation Frequency		f_{max}	1	(Note B28)	3.75	4.80	6.00	MHz
VCO Min Oscillation Frequency		f_{min}	1	(Note B29)	1.00	2.20	3.30	MHz

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
VCO Freq. Control Sensitivity	f_{sen}	1	(Note B30)	1.40	1.80	2.30	kHz / V
APC Pull in Range (+)	F_{pp}	1	(Note B31)	4.6	5.3	—	kHz
APC Pull in Range (−)	F_{pm}	1	(Note B32)	−4.6	−5.3	—	kHz
VCO Output Level	FL_{ev}	1	(Note B33)	0.22	0.35	0.45	V_{p-p}
AGC Max Gain	G_{max}	1	(Note B34)	6.5	7.5	9.5	dB
AGC Min Gain	G_{min}	1	(Note B35)	−5.5	−3.5	−2.5	dB
AGC Knee Level (+)	G_{k+}	1	(Note B36)	5.5	6.5	—	dB
AGC Knee Level (−)	G_{k-}	1	(Note B37)	—	−6.5	−5.5	dB
CLAMP DET (+)	C_{d+}	1	(Note B38)	−10	0	10	mV
CLAMP DET (−)	C_{d-}	1	(Note B39)	−10	0	10	mV
HP PULSE Threshold Voltage	HP_{th}	1	(Note B40)	3.3	3.5	3.7	V
GP PULSE Threshold Voltage	GP_{th}	1	(Note B41)	6.8	7.0	7.2	V

CCD electrical characteristics (Unless otherwise specified, V_{DD} = 5V, Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input-Output Gain (*)		V_{OUT1} /V_{IN1}	G_1	—	(Note C3)	1.8	4.0	6.2	dB
		V_{OUT2} /V_{IN2}	G_2		(Note C3)	1.8	4.0	6.2	
Freq. Characteristic (*)		Pin 19	f_{ch1}	—	(Note C4)	−3.0	−2.0	−1.0	dB
		Pin 16	f_{ch2}		(Note C4)	−3.0	−2.0	−1.0	
Output Inpedance (*)		Pin 19	Z_{o1}	—	(Note C5)	150	300	450	Ω
		Pin 16	Z_{o2}		(Note C5)	150	300	450	
Linearity	REF Pulse Level	Pin 19	V_{rpl1}	—	(Note C6)	120	125	130	%
		Pin 16	V_{rpl2}		(Note C6)	120	125	130	
	LOW Pulse Level	Pin 19	V_{LL1}		(Note C6)	95	100	105	
		Pin 16	V_{LL2}		(Note C6)	95	100	105	
	HIGH Level	Pin 19	V_{HL1}		(Note C6)	95	100	105	
		Pin 16	V_{HL2}		(Note C6)	95	100	105	
Clock LeakageLevel		Pin 19	L_{CLK1}	—	(Note C7)	—	—	70.0	mV_{rms}
		Pin 16	L_{CHK2}		(Note C7)	—	—	70.0	

*: It is necessary that external bais voltage is added to input circuit when sine-wave is inpted. Please control external bias voltage so that input terminal voltage is 0.2V higher than no signal level.

TEST CONDITION

Note: GP PULSE ON : Firstly, Apply SAND CASTLE PULSE to pin 7.
Then, Apply the voltage equal to GATE-PULSE level to pin 7.

RP PULSE ON : Firstly, Apply SAND CASTLE PULSE to pin 7.
Then, Apply the voltage equal to H-PULSE level to pin 7.

PULSE OFF : Firstly, Apply SAND CASTLE PULSE to pin 7. Then, Apply the voltage equal to LOW level to pin 7.

Note B1: Power Supply Current.
(1) Pin 7 : Pulse OFF.
(2) Measure the current that flow into IC.

Note B2: Pin 1~3, 26~28 Terminal Voltage.
(1) Pin 7 : GP Pulse ON.
(2) Measure the voltage of each terminals.

Note B3: Pin 4, 8 Terminal Voltage.
(1) Pin 7 : RP Pulse ON.
(2) Measure the voltage of each terminals.

Note B4: Pin 6, 9, 10 Terminal Voltage.
(1) Pin 7 : Pulse OFF.
(2) Measure the voltage of each terminals.

Note B5: Pin 22, 23 Terminal Voltage.
(1) Pin 7 : OPEN.
(2) Measure the voltage of each terminals.

Note B6: Pin 29 Terminal Voltage and Change.
(1) Pin7 : GP Pulse ON.
(2) Apply 0V to pin 24 (SW_2 on).
(3) Apply 0V to pin 25 (SW_1 on).
(4) Measure the voltage pin 29 (V_{29}).
(5) Apply 0V to pin 24 (SW_2 on).
(6) Apply 9V to pin 25 (SW_2 off).
(7) Measure the voltage pin 29 (V_{29a}).
(8) The voltage of pin 29 is V_{29}.
(9) The voltage change at pin 29 is $V_{29} - V_{29a}$.

Note B7: Pin 30 terminal voltage and change.
(1) Pin 7 : GP Pulse ON.
(2) Apply 0V to pin 24 (SW_2 on).
(3) Apply 0V to pin 25 (SW_1 on).
(4) Measure the voltage pin 30 (V_{30}).
(5) Apply 0V to pin 24 (SW_2 on).
(6) Apply 9V to pin 25 (SW_2 off).
(7) Measure the voltage pin 30 (V_{30a}).
(8) The voltage of pin 29 is V_{30}.
(9) The voltage change at pin 30 is $V_{30} - V_{30a}$.

Note B8: Pin 26 Input Dynamic Range.
(1) Pin 7 : Pulse OFF.
(2) Apply 100kHz sin curve signal to pin 26 with, 5.2V bias.
(3) Observe pin 3 with spectrum analyzer measure input signal amplitude when 3rd harmonic is −40dB against fundamental wave.

Note B9: Pin 27 Input Dynamic Range.

(1) Pin 7 : Pulse OFF.
(2) Apply 100kHz sin curve signal to pin 27 with, 5.2V bias.
(3) Observe pin 2 with spectrum analyzer measure input signal amplitude when 3rd harmonic is −40dB against fundamental wave.

Note B10: Pin 26 Linearity

(1) Pin 7 : Pulse OFF.
(2) Measure $V_{3a} - V_{3f}$ at condition mentioned in below table.

Applied voltage to pin 26	4.70V	5.00V	5.05V	5.35V	5.50V	5.80V
Measured voltage at pin 3	V_{3a}	V_{3b}	V_{3c}	V_{3d}	V_{3e}	V_{3f}

(3) Calculate followings.

1) Get the slopes.
$G_1 = (V_{3b} - V_{3a}) \div 0.3$
$G_2 = (V_{3d} - V_{3c}) \div 0.3$
$G_3 = (V_{3f} - V_{3e}) \div 0.3$

2) Get the linearitys.
$LN1 = 100 \times (G_1 - G_2) \div G_2$
$LN2 = 100 \times (G_2 - G_3) \div G_3$
$LN3 = 100 \times (G_3 - G_1) \div G_1$

Note B11: Pin 27 Linearity.

(1) Pin 7 : Pulse OFF.
(2) Measure $V_{2a} - V_{2f}$ at condition mentioned in below table.

Applied voltage to pin 27	4.70V	5.00V	5.05V	5.35V	5.50V	5.80V
Measured voltage at pin 2	V_{2a}	V_{2b}	V_{2c}	V_{2d}	V_{2e}	V_{2f}

(3) Calculate followings.

1) Get the slopes.
$G_1 = (V_{2b} - V_{2a}) \div 0.3$
$G_2 = (V_{2d} - V_{2c}) \div 0.3$
$G_3 = (V_{2f} - V_{2e}) \div 0.3$

2) Get the linearitys.
$LN1 = 100 \times (G_1 - G_2) \div G_2$
$LN2 = 100 \times (G_2 - G_3) \div G_3$
$LN3 = 100 \times (G_3 - G_1) \div G_1$

Note B12: Pin 2 Output Level.

(1) Pin 7 : Pulse OFF.
(2) Apply 100kHz, $0.8V_{p\text{-}p}$, sine signal to pin 27 with, 5.2V bias.
(3) Measure the output level of pin 2.

Note B13: Pin 3 Output Level.

(1) Pin 7 : Pulse OFF.
(2) Apply 100kHz, $0.8V_{p\text{-}p}$, sine signal to pin 26 with, 5.2V bias.
(3) Measure the output level of pin 3.

Note B14: Pin 2 Pulse Ins. Level.

(1) Pin 7 : Input Sand Castle Pulse.
(2) Observe pin 2, Measure amplitude of pulse.

Note B15: Pin 3 Pulse Ins. Level.

(1) Pin 7 : Input Sand Castle Pulse.
(2) Observe pin 3, Measure amplitude of pulse.

Note B16: RP Pulse Delay Time.

(1) Pin 7 : Input Sand Castle Pulse.
(2) Observe pin 7 and 3, Measure the period from leading at edge at pin 7 to trailing edge at pin 3.

Note B17: L.P.F. f_0 (1)

(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 2.0V to pin 8.
(3) Apply 4.5V to pin 28.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 23, Measure frequency response at pin 29.
Note: Get the frequency when amplitude is −3dB against amplitude at 100kHz.

Note B18: L.P.F. f_0 (2)
(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 4.5V to pin 1.
(3) Apply 2.0V to pin 4.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 23, Measure frequency response at pin 30.
Note: Get the frequency when amplitude is −3dB against amplitude at 100kHz.

Note B19: TRAP f_0 (1)
(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 2.0V to pin 8.
(3) Apply 4.5V to pin 28.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 23, Measure frequency response at pin 29.
Note: Get the frequency at the TRAP.

Note B20: TRAP f_0 (2)
(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 4.5V to pin 1.
(3) Apply 2.0V to pin 4.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 22, Measure frequency response at pin 30.
Note: Get the frequency at the TRAP.

Note B21: TRAP Attenuation Value (1).
(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 2.0V to pin 8.
(3) Apply 4.5V to pin 28.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 23, Measure frequency response at pin 29.
Note: Get the level at 3.54MHz against level at 100kHz.

Note B22: TRAP Attenuation (2)
(1) Pin 7 : Input Sand Castle Pulse.
(2) Apply 4.5V to pin 1.
(3) Apply 2.0V to pin 4.
(4) Pin 24 : OPEN.
(5) Apply 9.0V to pin 25.
(6) Input $0.8V_{p\text{-}p}$ sin wave signal to pin 22, Measure frequency response at pin 30.
Note: Get the level at 3.54MHz against level at 100kHz.

Note B23: Pin 22 Impedance.
(1) Apply 4.6V to pin 22.
(2) Measure the current that flows into pin 22. (I_{22a})
(3) Apply 5.0V to pin 22.
(4) Measure the current that flows into pin 22. (I_{22b})
(5) Calculate impedance. $400 / (I_{22b} - I_{22a})$

Note B24: Pin 23 Impedance.
(1) Apply 4.6V to pin 23.
(2) Measure the current that flows into pin 23. (I_{23a})
(3) Apply 5.0V to pin 23.
(4) Measure the current that flows into pin 23. (I_{23b})
(5) Calculate impedance. $400 / (I_{23b} - I_{23a})$

Note B25: SW_1 Threshold Voltage.
(1) Pin 7 : Pulse OFF.
(2) Pin 25 : OPEN.
(3) Input 100kHz, $0.8V_{p\text{-}p}$, sine wave to pin 26 with, 5.2V bias.
(4) Connect external voltage supply to pin 24 observe pin 29 with changing supply voltage, Measure the voltage of when output level is changed supply voltage to pin 24.

Note B26: SW_2 Threshold Voltage.
(1) Pin 7 : Pulse OFF.
(2) Pin 24 : OPEN.
(3) Input 100kHz, $0.8V_{p\text{-}p}$, sine wave to pin 23.
(4) Apply 4.5V to pin 28.
(5) Apply 4.5V to pin 8.
(6) Connect external voltage supply to pin 25 observe pin 29 with changing supply voltage, Measure the voltage of when the signal appear at pin 29.

Note B27: VCO Free-run Frequency.
(1) Pin 7 : Pulse OFF.
(2) Measure the frequency of output signal at pin 10.

Note B28: VCO Max. Frequency.
(1) Pin 7 : Pulse OFF.
(2) Apply 3.0V to pin 9.
(3) Measure the frequency of output signal at pin 10.

Note B29: VCO Min. Frequency.
(1) Pin 7 : Pulse OFF.
(2) Apply 3.0V to pin 9.
(3) Measure the frequency of output signal at pin 10.

Note B30: Frequency Control Sensitivity.
(1) Pin 7 : Pulse OFF.
(2) Apply 4.2V to pin 9. (f_{10a})
(3) Measure the frequency of output signal at pin 10.
(4) Apply 4.8V to pin 9. (f_{10b})
(5) Measure the frequency of output signal at pin 10.
(6) Calculate frequency control sensitivity. $(f_{10b} - f_{10a}) / 0.6$

Note B31: APC Pull-in Range (+)
(1) Input 0.3V, 15.734kHz, 10μs pulse to pin 7.
(2) Observe pin 9 contain AFC is locked.
(3) Increase input frequency due to unlock APC. Then decrease input frequency measure the input frequency when APC is locked again. (f_{7a})
(4) Calculate pull-in frequency. (f_{7a} − 15.734kHz)

Note B32: APC Pull-in Range (−)
(1) Input 0.3V, 15.734kHz, 10μs pulse to pin 7.
(2) Observe pin 9 contain AFC is locked.
(3) Increase input frequency due to unlock APC. Then decrease input frequency measure the input frequency when APC is locked again. (f_{7b})
(4) Calculate pull-in frequency. (f_{7b} − 15.734kHz)

Note B33: VCO Output Level.
(1) Input Sand Castle Pulse to pin 7.
(2) Measure amplitude of output signal at pin 10.

Note B34: AGC Max. Gain.

(1) Input Sand Castle Pulse to pin 7.
(2) Pin 24 : OPEN.
(3) Apply 9.0V to pin 25.
(4) Apply 2.0V to pin 8.
(5) Input 100kHz, sine wave signal, which is synchronized with f_H, to pin 23.
(6) Observe pin 29, Measure input signal amplitude. At pin 23 when output signal amplitude is 0.8Vp-p at pin 29. (V_{23a})
(7) Calculate gain. G = 20ℓog (0.8 / V_{23a})

Note B35: AGC Min. Gain.

(1) Input Sand Castle Pulse to pin 7.
(2) Pin 24 : OPEN.
(3) Apply 9.0V to pin 25.
(4) Apply 7.0V to pin 8.
(5) Input 100kHz, sine wave signal, which is synchronized with f_H, to pin 23.
(6) Observe pin 29, Measure input signal amplitude. At pin 23 when output signal amplitude is $0.8V_{p\text{-}p}$ at pin 29. (V_{23b})
(7) Calculate gain. G = 20ℓog (0.8 / V_{23b})

Note B36: AGC Knee Level (+)

(1) Input Sand Castle Pulse to pin 7.
(2) Apply 9.0V to pin 24.
(3) Apply 9.0V to pin 25.
(4) Input 100kHz, sine wave signal, which is synchronized with f_H, to pin 26.
(5) Connect pin 3 to pin 23 via amplifier.
(6) Set the input level at pin 23 is $0.8V_{p\text{-}p}$ by adjusting gain of amplifier.
(7) Measure output signal at pin 29. (V_{29})
(8) Measure input signal amplitude at pin 23 when the output signal amplitude at pin 29 is 0.5dB bigger than V_{29} with adjusting gain of amplifier. (V_{23a})
(9) Calculate knee level. 20ℓog (V_{23a} / 0.8)

Note B37: AGC Knee Level (−)

(1) Input Sand Castle Pulse to pin 7.
(2) Apply 9.0V to pin 24.
(3) Apply 9.0V to pin 25.
(4) Input 100kHz, sine wave signal, which is synchronized with f_H, to pin 26.
(5) Connect pin 3 to pin 23 via amplifier.
(6) Set the input level at pin 23 is $0.8V_{p\text{-}p}$ by adjusting gain of amplifier.
(7) Measure output signal at pin 29. (V_{29})
(8) Measure input signal amplitude at pin 23 when the output signal amplitude at pin 29 is −0.5dB bigger than V_{29} with adjusting gain of amplifier. (V_{23b})
(9) Calculate knee level. 20ℓog (V_{23b} / 0.8)

Note B38: Clamp Det (+)

(1) Pin 7 : GP Pulse ON.
(2) Apply 2.0V to pin 8.
(3) Apply 9.0V to pin 25.
(4) Pin 24 : OPEN.
(5) Apply 4.5V to pin 23.
(6) Measure voltage at pin 29. (V_{29})
(7) Apply 5.0V to pin 23.
(8) Measure voltage at pin 29. (V_{29a})
(9) Calculate voltage change. ($V_{29a} - V_{29}$)

Note B39: Clamp Det (−)

(1) Pin 7 : GP Pulse ON.
(2) Apply 2.0V to pin 8.
(3) Apply 9.0V to pin 25.
(4) Pin 24 : OPEN.
(5) Apply 4.5V to pin 23.
(6) Measure voltage at pin 29. (V_{29})
(7) Apply 4.0V to pin 23.
(8) Measure voltage at pin 29. (V_{29b})
(9) Calculate voltage change. ($V_{29b} - V_{29}$)

Note B40: HP Pulse Threshold Voltage.

(1) Input Sand Castle Pulse to pin 7.
(2) Decrease H.BLK level until disappear normal pulse at pin 3. Then, Increase H.BLK level. Measure H.BLK level when normal pulse appear at pin 3.

Note B41: GP Pulse Threshold Voltage.

(1) Input Sand Castle Pulse to pin 7.
(2) Decrease Gate-Pulse level until voltage at pin 26 isn't clamped to 5.2V, Then increase Gate-Pulse level. Measure Gate-Pulse level when voltage at pin 26 is clamped to 5.2V.

Note C1: Power Supply Current.

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.
(2) Pin 13 and 15 are no input. (S_1, S_2 = b)
(3) After 20s from (1), Measure the current from power supply.

Note C2: Pin 11~20 Terminal Voltage.

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.
(2) Pin 13 and 15 are no input. (S_1, S_2 = b)
(3) Measure the voltage at each pin.

Note C3: Input-Output Gain.

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.
(2) Apply external bias voltage to pin 13 and 15 so that the voltage at pin 13 and 15 are 0.2V higher than voltage when no input.
(3) Input f = 15kHz, Lev = 0.3$V_{p\text{-}p}$ signal to pin 13 and 15. (S_1, S_2 = c) (V_{IN})
(4) Measure output signal amplitude at pin 16 and 19. (V_{OUT})
(5) Calculate gain.

G_1 (G_2) = 20ℓog (V_{OUT} / V_{IN}) [dB]

Note C4: Frequency Response

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.
(2) Apply external bias voltage to pin 13 and 15 so that the voltage at pin 13 and 15 are 0.2V higher than voltage when no input.
(3) Input f = 1.17MHz, Lev = 0.3$V_{p\text{-}p}$ signal to pin 13 and 15. (S_1, S_2 = c) (V_{IN})
(4) Measure output signal amplitude at pin 16 and 19. (V_{OUT})
(5) Calculate gain.

G = 20 λog (V_{OUT} / V_{IN}) [dB]

Calculate frequency response.

f_{ch1} (f_{ch2}) = G_1 (G_2) −G [dB]

Note C5: Output Impedance.

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.
(2) Apply external bias voltage to pin 13 and 15 so that the voltage at pin 13 and 15 are 0.2V higher than voltage when no input.
(3) Input f = 15kHz, Lev = 0.3$V_{p\text{-}p}$ signal to pin 13 and 15. (S_1, S_2 = c)
(4) Measure output level (15KHz component) at pin 16 and 19. (V_{outa})
(5) Measure output level (15KHz component) with load at pin 16 and 19. (V_{outb})
(6) Calculate output impedance.

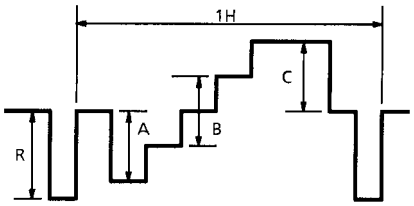
$$Z_{o1}\ (Z_{o2}) = (10^{\frac{V_{outa} - V_{outb}}{20}} - 1) \times 300\ [\Omega]$$

Note C6: Linearity

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.

(2) Input 4 step signal to pin 13 and 15. (S_1, S_2 = c)

<Input Signal>



(*) Duty = 50%

(*) Input level

R = 0.25$V_{p\text{-}p}$

A, B, C = 0.2$V_{p\text{-}p}$

(3) Measure output signal (R, A, B, C) amplitude at pin 16 and 19.

(4) Calculate linearity

$$V_{rpl1}\ (V_{rpl2}) = \frac{R}{A} \times 100\ [\%] \qquad V_{HL1}\ (V_{HL2}) = \frac{C}{A} \times 100\ [\%]$$

$$V_{LL1}\ (V_{LL2}) = \frac{B}{A} \times 100\ [\%]$$

Note C7: Clock Leak

(1) Input f = 225f_H, Lev = 0.3$V_{p\text{-}p}$ signal to pin 11.

(2) Pin 13 and 15 are no input. (S_1, S_2 = b)

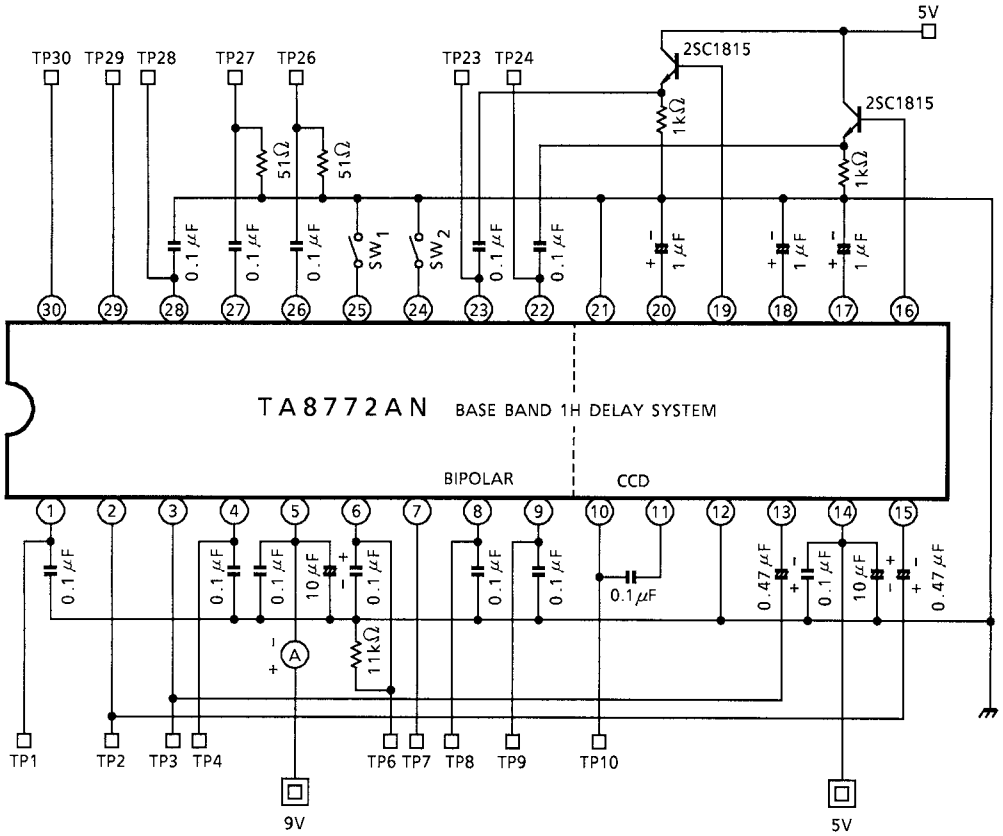
(3) Measure clock level (225f_H component) with spectrum analyzer at pin 11. (V_{in} [dB])

(4) Measure clock level (225f_H component) with spectrum analyzer at pin 16 and 19. (V_{out} [dB])

(6) Measure clock leak.

$$\text{CLOCK LEAK } (L_{clk1} / L_{clk2}) = 10^{\frac{V_{out} - V_{in}}{20}} \times 300 \times \frac{1}{2\sqrt{2}}\ [mV_{rms}]$$

TEST CIRCUIT

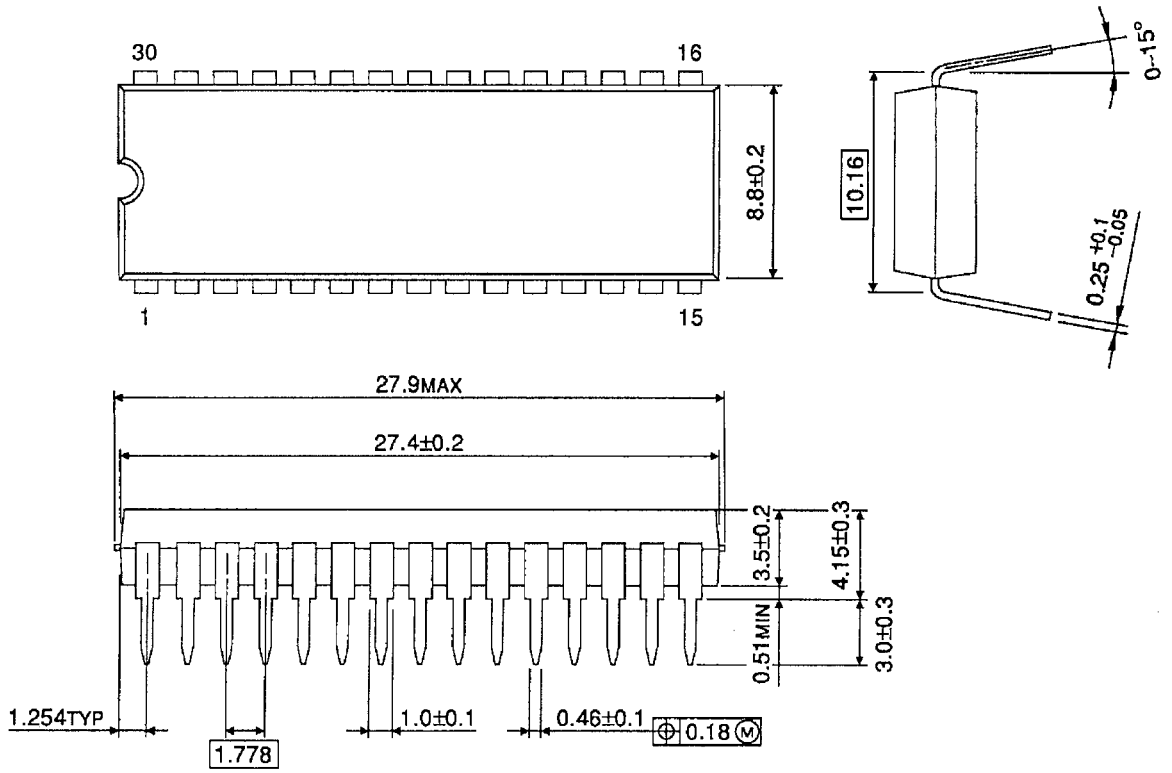


ATTENTION FOR HANDLING

The input and output terminal is high impedance when this IC is not mounted. So, It is necessary that you must protect it from external electronical stress.

PACKAGE DIMENSIONS

SDIP30-P-400-1.78 Unit: mm



Weight: 1.99g (Typ.)

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000707EBA

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