160-W STEREO / 300-W MONO PurePath™ HD DIGITAL-INPUT POWER STAGE

Check for Samples: TAS5616

FEATURES

- **PurePath™ HD Enabled Integrated Feedback Provides:**
  - **Signal Bandwidth up to 80 kHz for High-Frequency Content From HD Sources**
  - **Ultralow 0.03% THD at 1 W into 8 Ω**
  - **Flat THD at All Frequencies for Natural Sound**
  - **80-dB PSRR (BTL, No Input Signal)**
  - **>100-dB (A-weighted) SNR**
  - **Click- and Pop-Free Startup**
  - **Minimal External Components Compared to Discrete Solutions**
- **Multiple Configurations Possible on the Same PCB With Stuffing Options:**
  - **Mono Parallel Bridge-Tied Load (PBTL)**
  - **Stereo Bridge-Tied Load (BTL)**
  - **2.1 Single-Ended Stereo Pair and Bridge-Tied Load Subwoofer**
  - **Quad Single-Ended Outputs**
- **Total Output Power at 10% THD+N**
  - **330 W in Mono PBTL Configuration**
  - **160 W per Channel in Stereo BTL Configuration**
  - **80 W per Channel in Quad Single-Ended Configuration**
- **High-Efficiency Power Stage (>90%) With 120-mΩ Output MOSFETs**
- **Two Thermally Enhanced Package Options:**
  - **PHD (64-Pin QFP)**
  - **DKD (44-Pin PSOP3)**
- **Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting**
- **EMI Compliant When Used With Recommended System Design**

APPLICATIONS

- **Mini Combo System**
- **AV Receivers**
- **DVD Receivers**
- **Active Speakers**

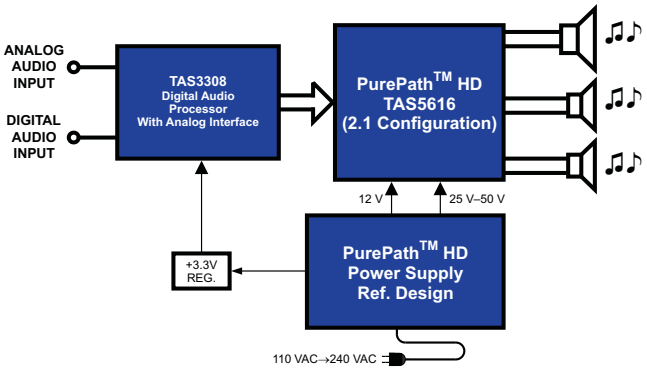
DESCRIPTION

The TAS5616 is a high-performance PWM-input class-D amplifier with integrated closed-loop feedback technology (known as PurePath™ HD technology). It has the ability to drive up to 160-W (1) stereo into 8-Ω speakers from a single 50-V supply.

PurePath™ HD technology enables traditional AB-amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Ultralow 0.03% THD+N is flat across all frequencies, ensuring that the amplifier does not add uneven distortion characteristics, and helps maintain a natural sound.

The efficiency of this class-D amplifier is greater than 90%. Undervoltage protection, overtemperature, clipping, short-circuit and overcurrent protection are all integrated, safeguarding the device and speakers against fault conditions that could damage the system.



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high performance thermal interface material between the package exposed thermal pad and the heat sink should be used to achieve high output power levels.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

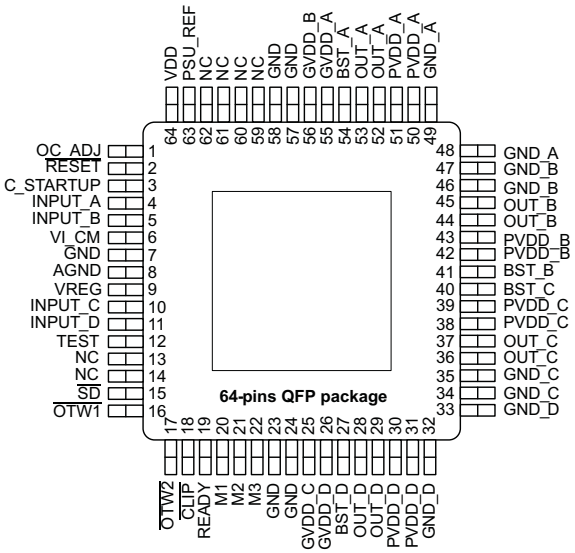
Terminal Assignment

The TAS5616 is available in two thermally enhanced packages:

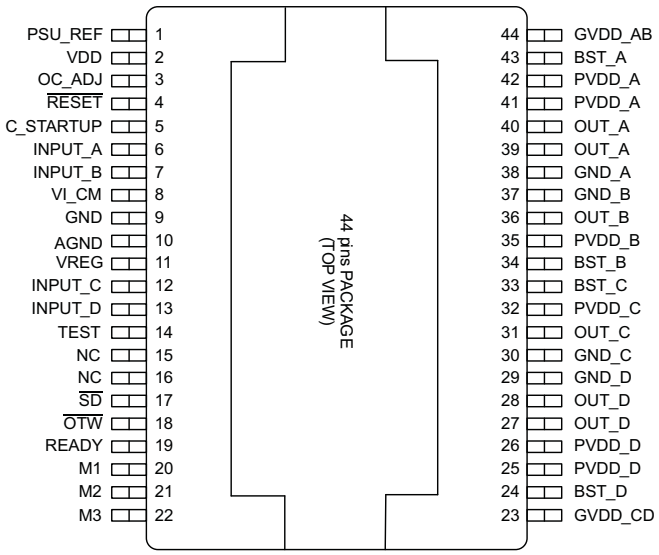
- 44-Pin PSOP3 package (DKD)
- 64-Pin QFP (PHD) Power Package

Both package types contain a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

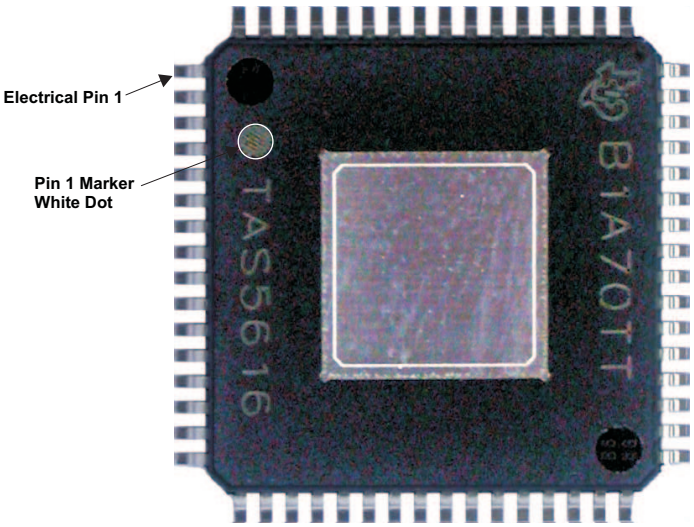
PHD PACKAGE
(TOP VIEW)



DKD PACKAGE
(TOP VIEW)



PIN ONE LOCATION PHD PACKAGE



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MODE SELECTION PINS

MODE PINS			ANALOG INPUT(1)	OUTPUT CONFIGURATION	DESCRIPTION		
M3	M2	M1					
0	0	0	2N	2 × BTL	AD mode		
0	0	1	—	—	Reserved		
0	1	0	2N	2 × BTL	BD mode		
0	1	1	1N	1 × BTL +2 × SE	AD mode		
1	0	0	1N	4 × SE	AD mode		
1	0	1	2N	1 × PBTL	INPUT_C(2)	INPUT_D(2)	
					0	0	AD mode
					1	0	BD mode
1	1	0	Reserved				
1	1	1					

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode (1=VREG and 0=AGND)..

PACKAGE HEAT DISSIPATION RATINGS(1)

PARAMETER	TAS5616PHD	TAS5616DKD
$R_{\theta JC}$ (°C/W) – 2 BTL or 4 SE channels	3.63	2.52
$R_{\theta JC}$ (°C/W) – 1 BTL or 2 SE channel(s)	5.95	3.22
$R_{\theta JC}$ (°C/W) – 1 SE channel	9.9	6.9
Pad Area (2)	49 mm^2	80 mm^2

(1) J_C is junction-to-case, C_H is case-to-heat sink
(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heat sink and both channels active. The $R_{\theta CH}$ with this condition is 1.22°C/W for the PHD package and 1.02°C/W for the DKD package

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
0°C–70°C	TAS5616PHD	64 pin HTQFP
0°C–70°C	TAS5616DKD	44 pin PSOP3

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

TAS5616			UNIT
VDD to AGND		–0.3 to 13.2	V
GVDD to AGND		–0.3 to 13.2	V
PVDD_X to GND_X(2)		–0.3 to 69.0	V
OUT_X to GND_X(2)		–0.3 to 69.0	V
BST_X to GND_X(2)		–0.3 to 82.2	V
BST_X to GVDD_X(2)		–0.3 to 69.0	V
VREG to AGND		–0.3 to 4.2	V
GND_X to GND		–0.3 to 0.3	V
GND_X to AGND		–0.3 to 0.3	V
GND to AGND		–0.3 to 0.3	V
OC_ADJ, M1, M2, M3, VI_CM, C_STARTUP, PSU_REF to AGND		–0.3 to 4.2	V
INPUT_X		–0.3 to 5.0	V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$ to AGND		–0.3 to 7.0	V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$)		9	mA
Maximum operating junction temperature range, T_J		0 to 150	°C
Storage temperature, T_{stg}		–40 to 150	°C
Electrostatic discharge	Human-Body Model (3) (all pins)	±2	kV
	Charged-Device Model (3) (all pins)	±500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.
(3) Failure to follow good anti-static ESD handling during manufacture and rework will contribute to device malfunction. Please ensure operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	25	50	52.5	V
	Half-bridge supply, BTL 4Ω load		25	38	40	
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter according to schematics in the application information section.	7	8		Ω
R_L(SE)			3.5	4		
R_L(PBTL)			3.5	4		
L_{OUTPUT}(BTL)	Output filter inductance	Minimum output inductance under short-circuit condition	14	15		µH
L_{OUTPUT}(SE)			14	15		
L_{OUTPUT}(PBTL)			14	15		
F_{PWM}	PWM frame rate		352	384	500	kHz
T_J	Junction temperature		0		150	°C

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TERMINAL FUNCTIONS

TERMINAL			FUNCTION(1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
AGND	8	10	P	Analog ground
BST_A	54	43	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_A required.
BST_B	41	34	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_B required.
BST_C	40	33	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_C required.
BST_D	27	24	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_D required.
C_STARTUP	3	5	O	Startup ramp requires a charging capacitor of 4.7 nF to AGND
$\overline{\text{CLIP}}$	18	—	O	Clipping warning; open drain; active low
GND	7, 23, 24, 57, 58	9	P	Ground
GND_A	48, 49	38	P	Power ground for half-bridge A
GND_B	46, 47	37	P	Power ground for half-bridge B
GND_C	34, 35	30	P	Power ground for half-bridge C
GND_D	32, 33	29	P	Power ground for half-bridge D
GVDD_A	55	—	P	Gate drive voltage supply requires 0.1 μF capacitor to AGND
GVDD_AB	—	44	P	Gate drive voltage supply requires 0.22 μF capacitor to AGND
GVDD_B	56	—	P	Gate drive voltage supply requires 0.1 μF capacitor to AGND
GVDD_C	25	—	P	Gate drive voltage supply requires 0.1 μF capacitor to AGND
GVDD_CD	—	23	P	Gate drive voltage supply requires 0.22 μF capacitor to AGND
GVDD_D	26	—	P	Gate drive voltage supply requires 0.1 μF capacitor to AGND
INPUT_A	4	6	I	Input signal for half bridge A
INPUT_B	5	7	I	Input signal for half bridge B
INPUT_C	10	12	I	Input signal for half bridge C
INPUT_D	11	13	I	Input signal for half bridge D
M1	20	20	I	Mode selection
M2	21	21	I	Mode selection
M3	22	22	I	Mode selection
NC	59-62	—	—	No connect, pins may be grounded.
NC	13	15	—	No connect, pins may be grounded.
NC	14	16	—	No connect, pins may be grounded.
OC_ADJ	1	3	O	Analog over current programming pin requires resistor to ground. 64 pin QFP package (PHD) = 22 kΩ 44 pin PSOP3 Package (DKD) = 24 kΩ
$\overline{\text{OTW}}$	—	18	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW1}}$	16	—	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW2}}$	17	—	O	Overtemperature warning signal, open drain, active low.
OUT_A	52, 53	39, 40	O	Output, half bridge A
OUT_B	44, 45	36	O	Output, half bridge B
OUT_C	36, 37	31	O	Output, half bridge C
OUT_D	28, 29	27, 28	O	Output, half bridge D
PSU_REF	63	1	P	PSU Reference requires close decoupling of 4.7 μF to AGND
PVDD_A	50, 51	41, 42	P	Power supply input for half bridges A requires close decoupling of 2.2-μF capacitor to GND_A
PVDD_B	42, 43	35	P	Power supply input for half bridges B requires close decoupling of 2.2-μF capacitor to GND_B
PVDD_C	38, 39	32	P	Power supply input for half bridges C requires close decoupling of 2.2-μF capacitor to GND_C
PVDD_D	30, 31	25, 26	P	Power supply input for half bridges D requires close decoupling of 2.2-μF capacitor to GND_D
READY	19	19	O	Normal operation; open drain; active high
$\overline{\text{RESET}}$	2	4	I	Device reset Input; active low
$\overline{\text{SD}}$	15	17	O	Shutdown signal, open drain, active low
TEST	12	14	I	Connect to VREG node

(1) I = Input, O = Output, P = Power

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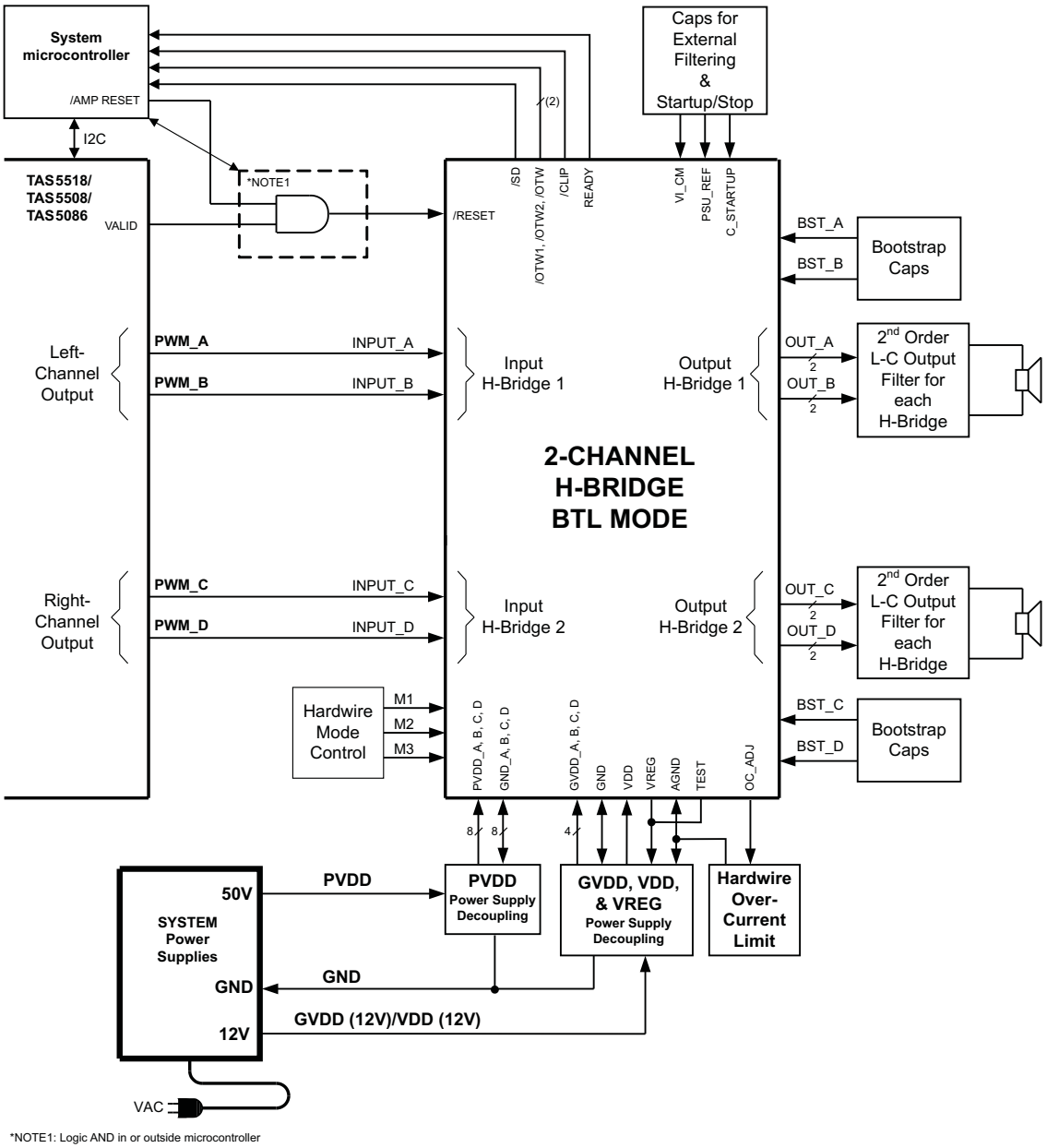
TERMINAL FUNCTIONS (continued)

TERMINAL			FUNCTION(1)	DESCRIPTION
NAME	PHD NO.	DKD NO.		
VDD	64	2	P	Power supply for digital voltage regulator requires a 10-μF capacitor in parallel with a 0.1-μF capacitor to GND for decoupling.
VI_CM	6	8	O	Analog comparator reference input requires close decoupling of 4.7 μF to AGND
VREG	9	11	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND

TYPICAL SYSTEM BLOCK DIAGRAM



*NOTE1: Logic AND in or outside microcontroller

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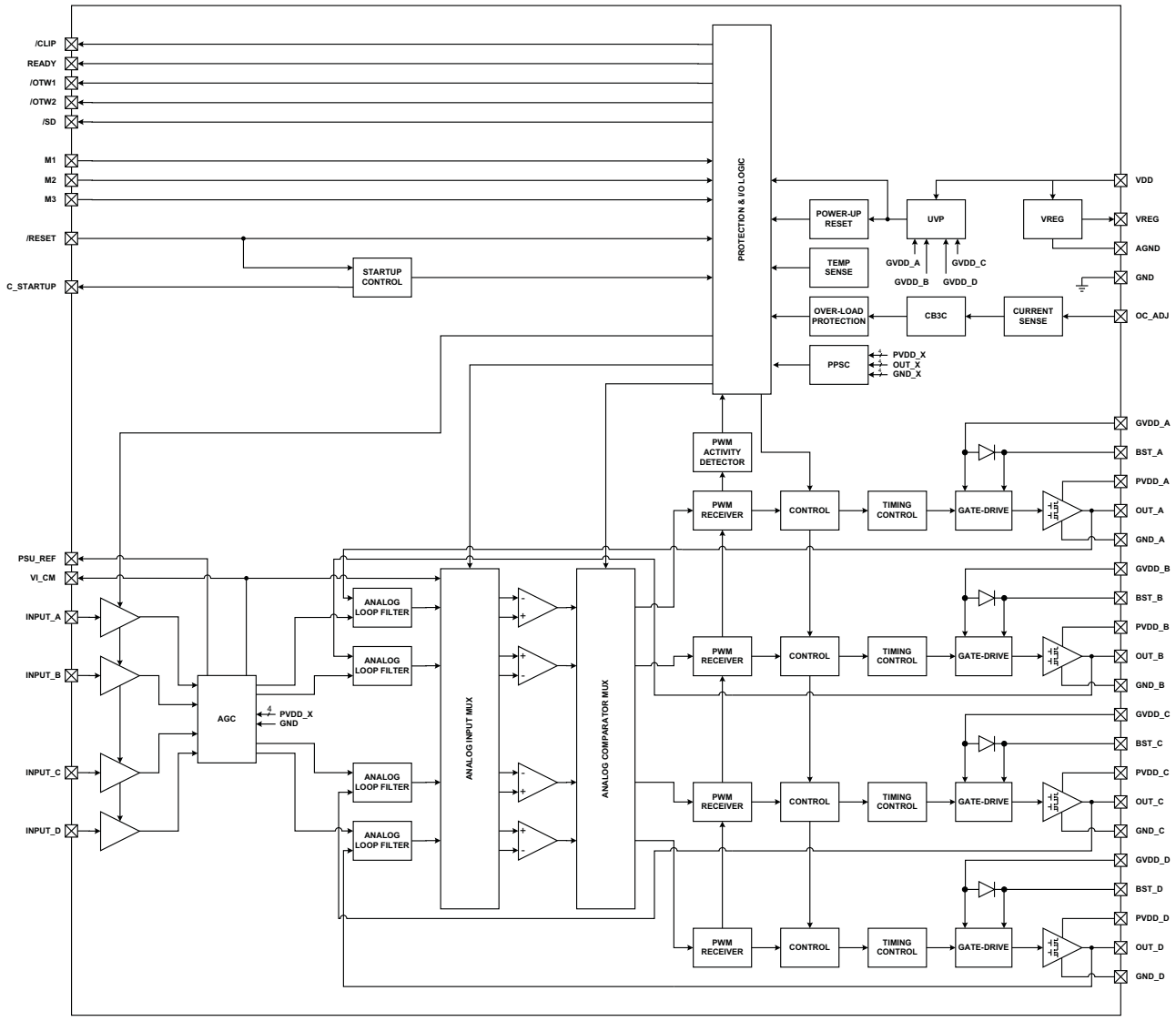
FUNCTIONAL BLOCK DIAGRAM



AUDIO CHARACTERISTICS (BTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM Processor (modulation index limited to 97.7%) and a TAS5616 power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 μH, C_{DEM} = 680 nF, MODE = 000, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 8 Ω, 10% THD+N		160		W
		R_L = 8 Ω, 1% THD+N		125		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, TAS5518 Modulator		185		μV
$\|V_{OS}\|$	Output offset supply	No signal		40	150	mV
SNR	Signal to noise ratio(1)	A-weighted, TAS5518 Modulator		103		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator		103		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		1.8		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

AUDIO SPECIFICATION (Single-Ended Output)

Audio performance is recorded as a chipset consisting of a TAS5086 PWM Processor (modulation index limited to 97.7%) and a TAS5616 power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4Ω, f_S = 384 kHz, R_{OC_PHD} = 22 kΩ, or R_{OC_DLD} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 μH, C_{DEM} = 330 nF, MODE = 100, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 4 Ω, 10%, THD+N		75		W
		R_L = 4 Ω, 0 dBFS		60		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted, TAS5086 modulator		170		μV
SNR	Signal to noise ratio(1)	A-weighted, TAS5086 modulator		98		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5086 modulator		98		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		2		W

(1) SNR is calculated relative to 1% THD+N output level
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATION (PBTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM Processor (modulation index limited to 97.7%) and a TAS5616 power stage. PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4Ω, f_S = 384 kHz, R_{OC_PHD} = 22 kΩ, R_{OC_DKD} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 μH, C_{DEM} = 680 nF, MODE = 101-00, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 4 Ω, 10%, THD+N		300		W
		R_L = 4 Ω, 1%, THD+N		210		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, TAS5518 modulator		180		μV
SNR	Signal to noise ratio(1)	A-weighted, TAS5518 modulator		103		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator		103		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		1.8		W

(1) SNR is calculated relative to 1% THD+N output level
(2) Actual system idle losses are affected by core losses of output inductors.

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ELECTRICAL CHARACTERISTICS

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node	VDD = 12 V	3	3.3	3.6	V
VI_CM	Analog comparator reference node		1.5	1.75	1.9	V
IVDD	VDD supply current	Operating, 50% duty cycle		22.5		mA
		Idle, reset mode		22.5		
I_{GVDD_x}	Gate-supply current per half-bridge	50% duty cycle		8		mA
		Reset mode		1.5		
I_{PVDD_x}	Half-bridge idle current	50% duty cycle without output filter or load		9		mA
		Reset mode, No switching		610		µA
OUTPUT-STAGE MOSFETs						
$R_{DS(on),LS}$	Drain-to-source resistance, (LS)	T_J = 25°C, exclude metallization resistance, GVDD = 12 V		120	200	mΩ
$R_{DS(on),HS}$	Drain-to-source resistance, (HS)			120	200	mΩ
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x			9.5		V
$V_{uvp,hyst}$ (1)				0.6		V
OTW1 (1)	Overtemperature warning 1		95	100	105	°C
OTW2 (1)	Overtemperature warning 2		115	125	135	°C
OTW_{HYST} (1)	Temperature drop needed below OTW temperature for $\overline{OTW}$ to be inactive after $\overline{OTW}$ event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
OTE-$OTW_{differential}$ (1)	OTE-OTW differential			30		°C
OTE_{HYST} (1)	A reset needs to occur for $\overline{SD}$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 384 kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, 64 pin QFP package (PHD) R_{OCP} = 22 kΩ		10		A
		Resistor – programmable, nominal peak current in 1Ω load, 44 pin PSOP3 package (DKD) R_{OCP} = 24 kΩ		10		A
$I_{OC\_LATCHED}$	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 47 kΩ		10		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected half bridge		150		ns
I_{PD}	Output pulldown current of each half bridge	Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	INPUT_X, M1, M2, M3, RESET	2			V
V_{IL}	Low level input voltage				0.8	V
Leakage	Input leakage current				100	µA

(1) Specified by design.

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ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pull-up resistance, $\overline{OTW1}$ to VREG, $\overline{OTW2}$ to VREG, $\overline{SD}$ to VREG		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pull-up resistor	3	3.3	3.6	V
		External pull-up of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
FANOUT	Device fanout $\overline{OTW1}$, $\overline{OTW2}$, $\overline{SD}$, $\overline{CLIP}$, $\overline{READY}$	No external pull-up		30		devices

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC+NOISE vs OUTPUT POWER

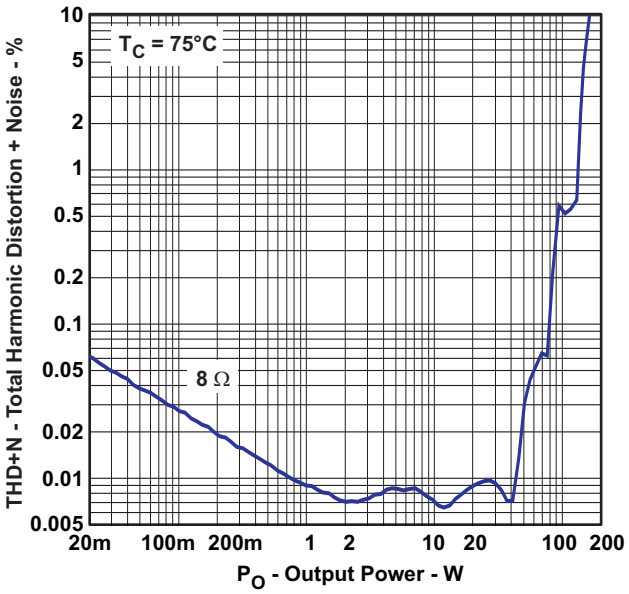

Figure 1.

OUTPUT POWER vs SUPPLY VOLTAGE

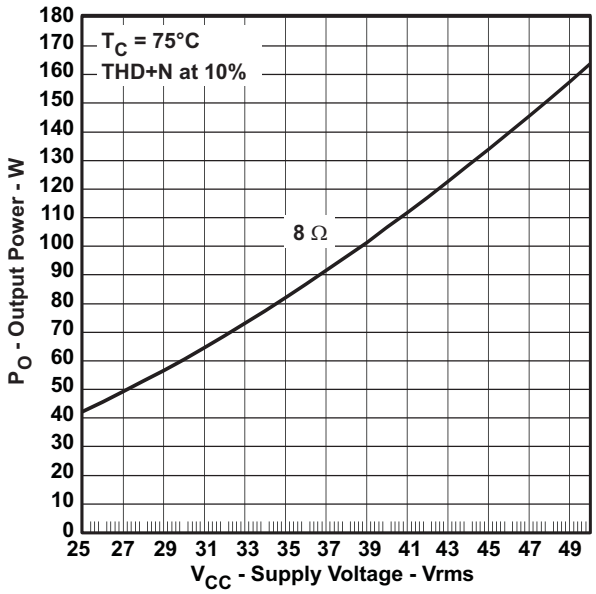

Figure 2.

UNCLIPPED OUTPUT POWER vs SUPPLY VOLTAGE

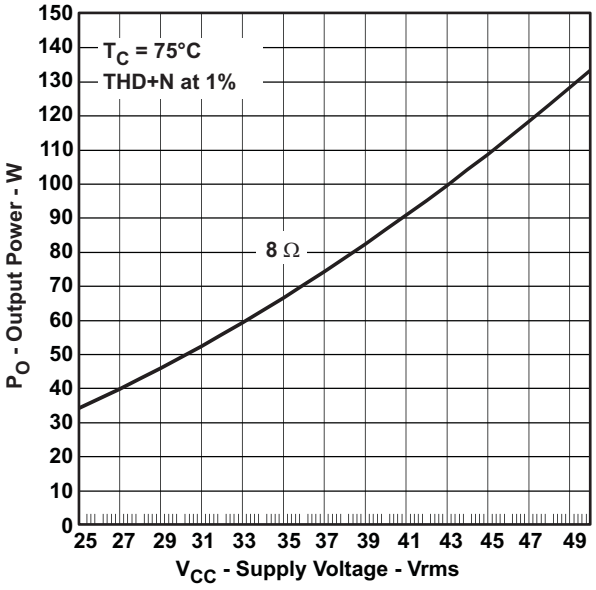

Figure 3.

SYSTEM EFFICIENCY vs OUTPUT POWER

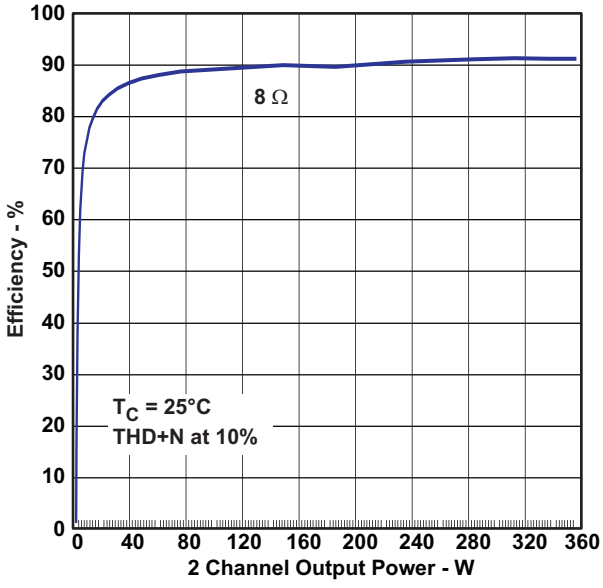

Figure 4.

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

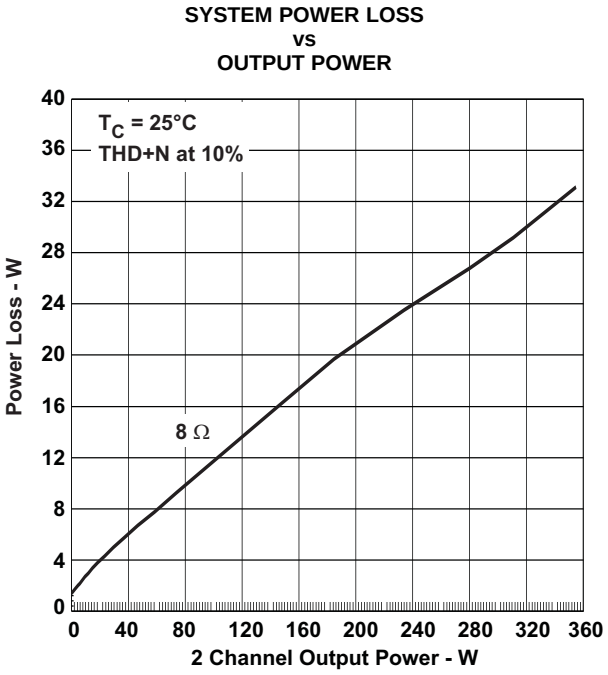

Figure 5.

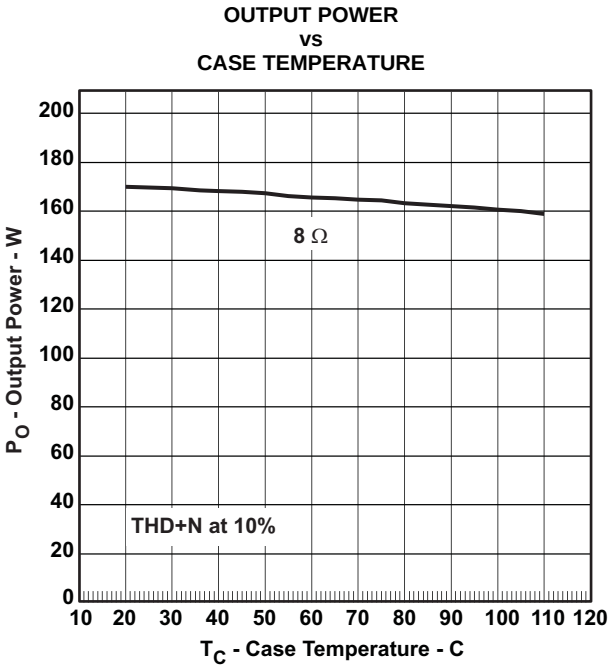

Figure 6.

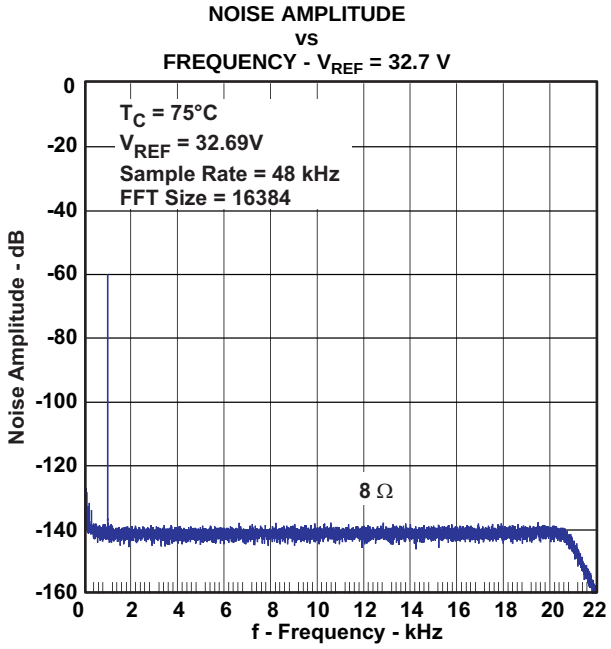

Figure 7.

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TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION vs OUTPUT POWER

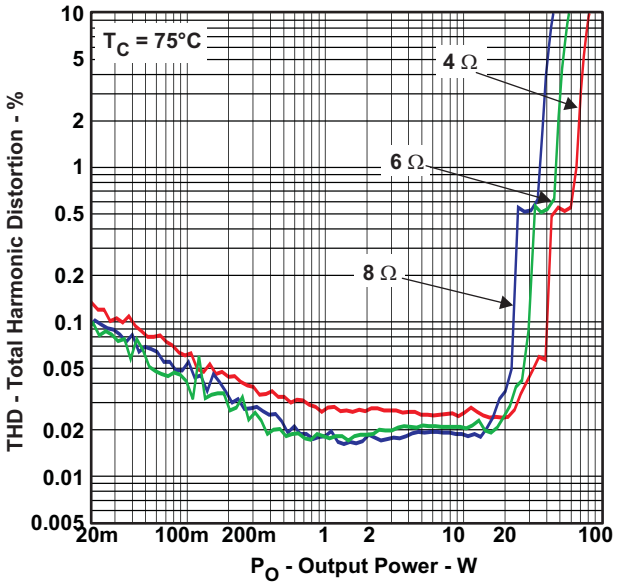

Figure 8.

OUTPUT POWER vs SUPPLY VOLTAGE

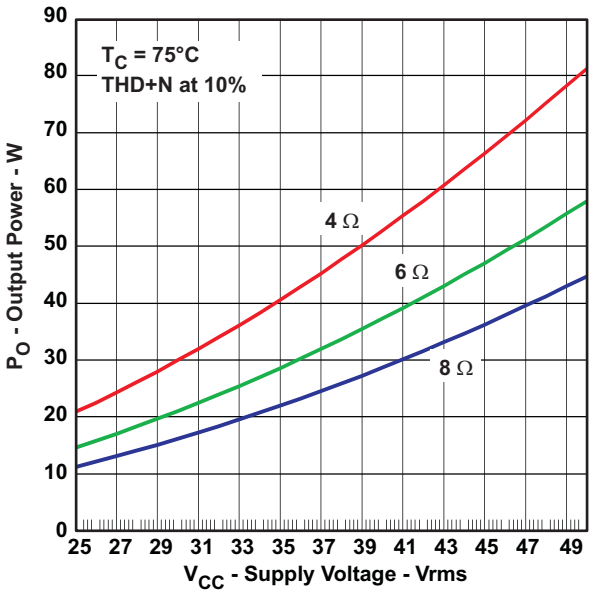

Figure 9.

OUTPUT POWER vs CASE TEMPERATURE

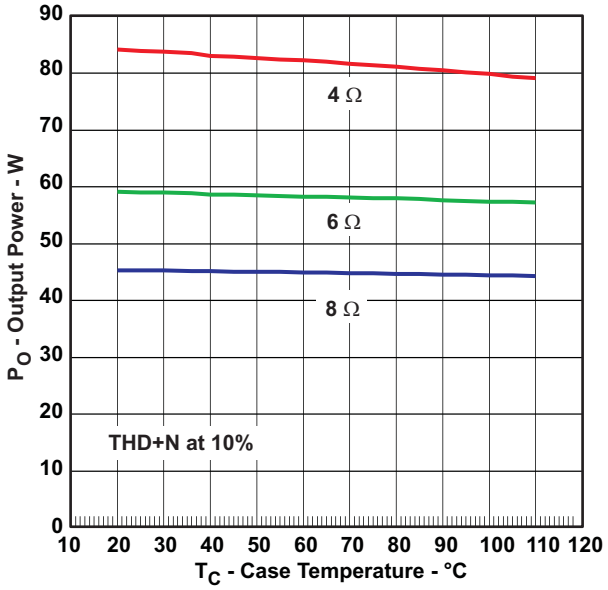

Figure 10.

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

TOTAL HARMONIC DISTORTION vs OUTPUT POWER

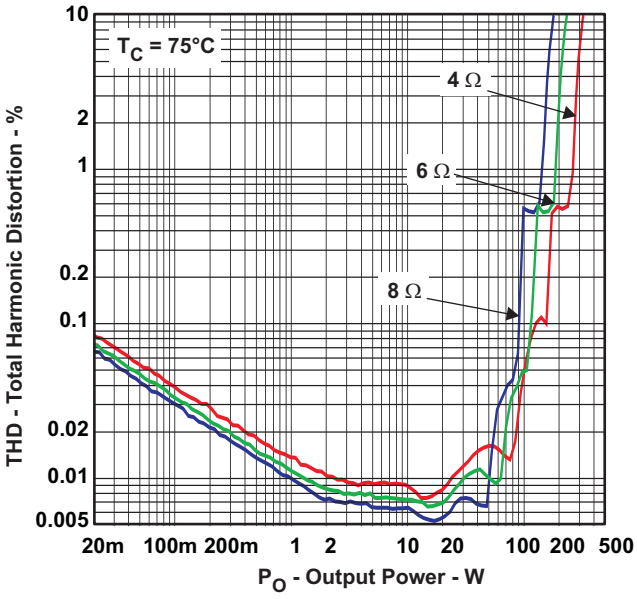

Figure 11.

OUTPUT POWER vs SUPPLY VOLTAGE

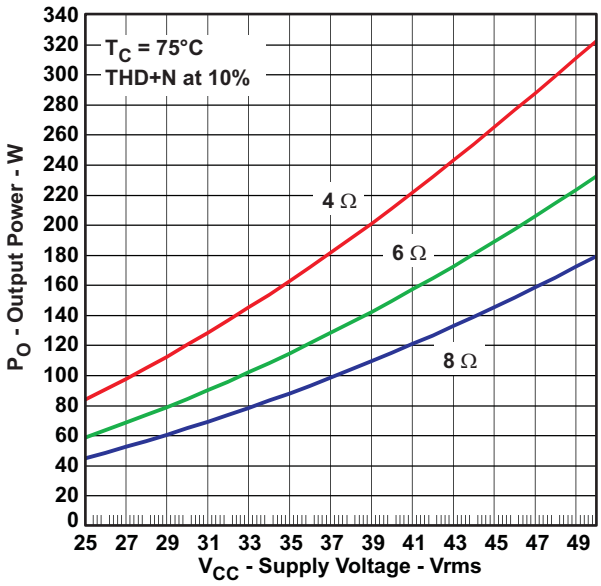

Figure 12.

OUTPUT POWER vs CASE TEMPERATURE

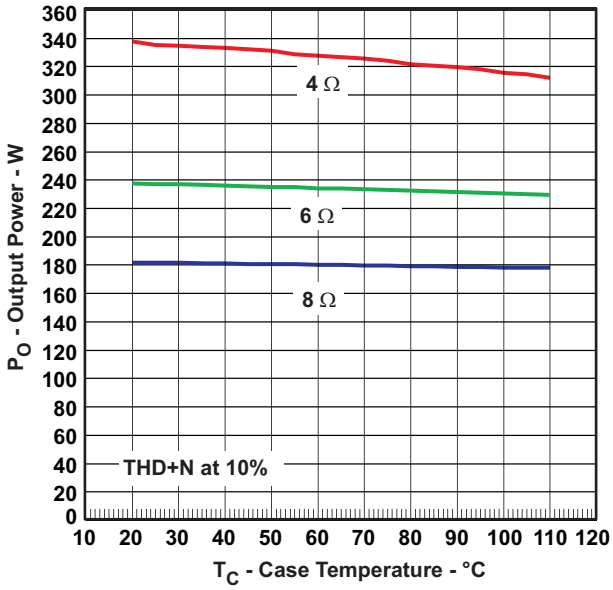

Figure 13.

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APPLICATION INFORMATION

PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 μm) is recommended for use with the TAS5616. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000μF, 63V will support more applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 0.1μF that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63V is required for use with a 50V power supply.

System Design Recommendations

The following schematics and PCB layouts illustrate *best practices* in the use of the TAS5616.

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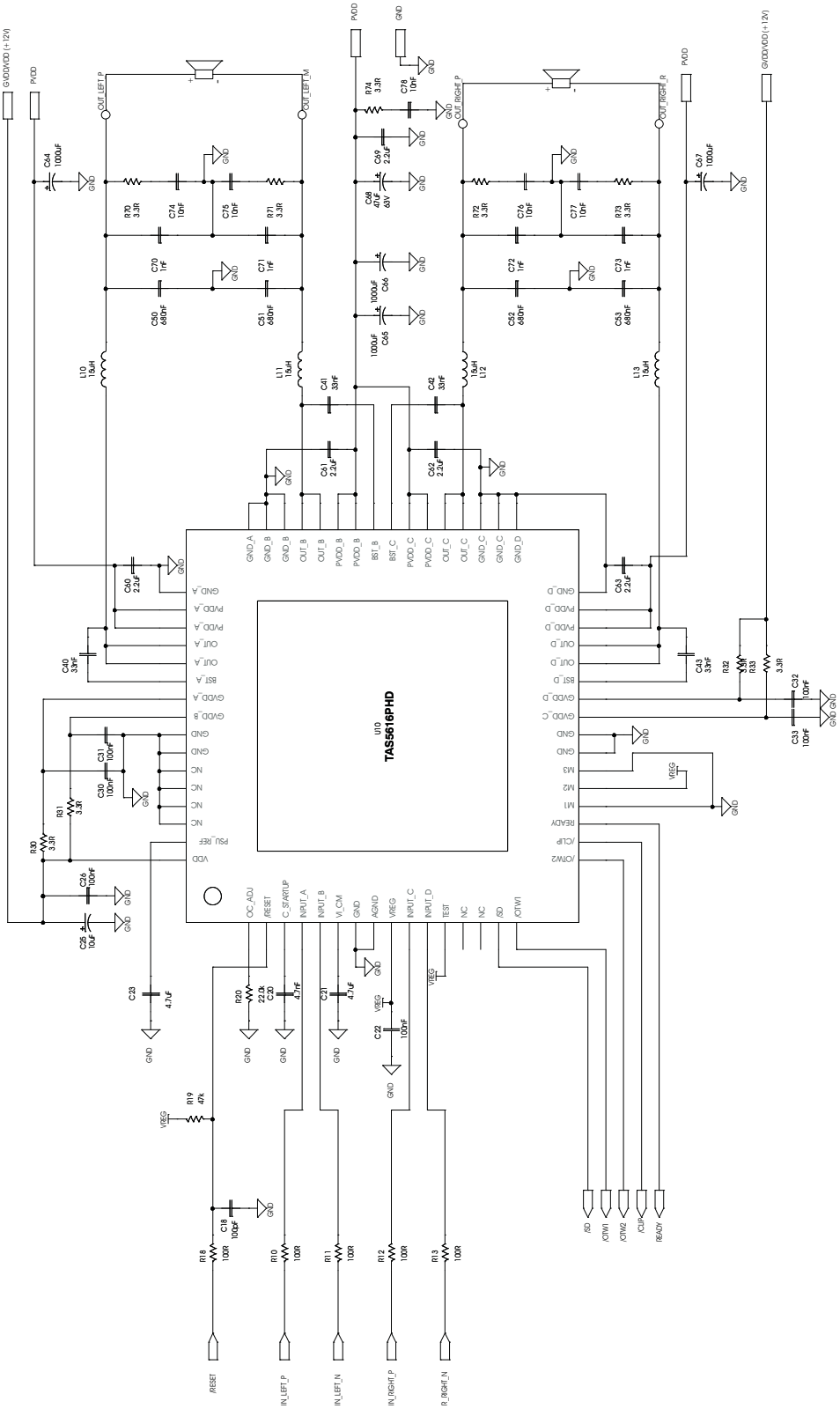

Figure 14. Typical Differential (2N) BTL Application With BD Filters

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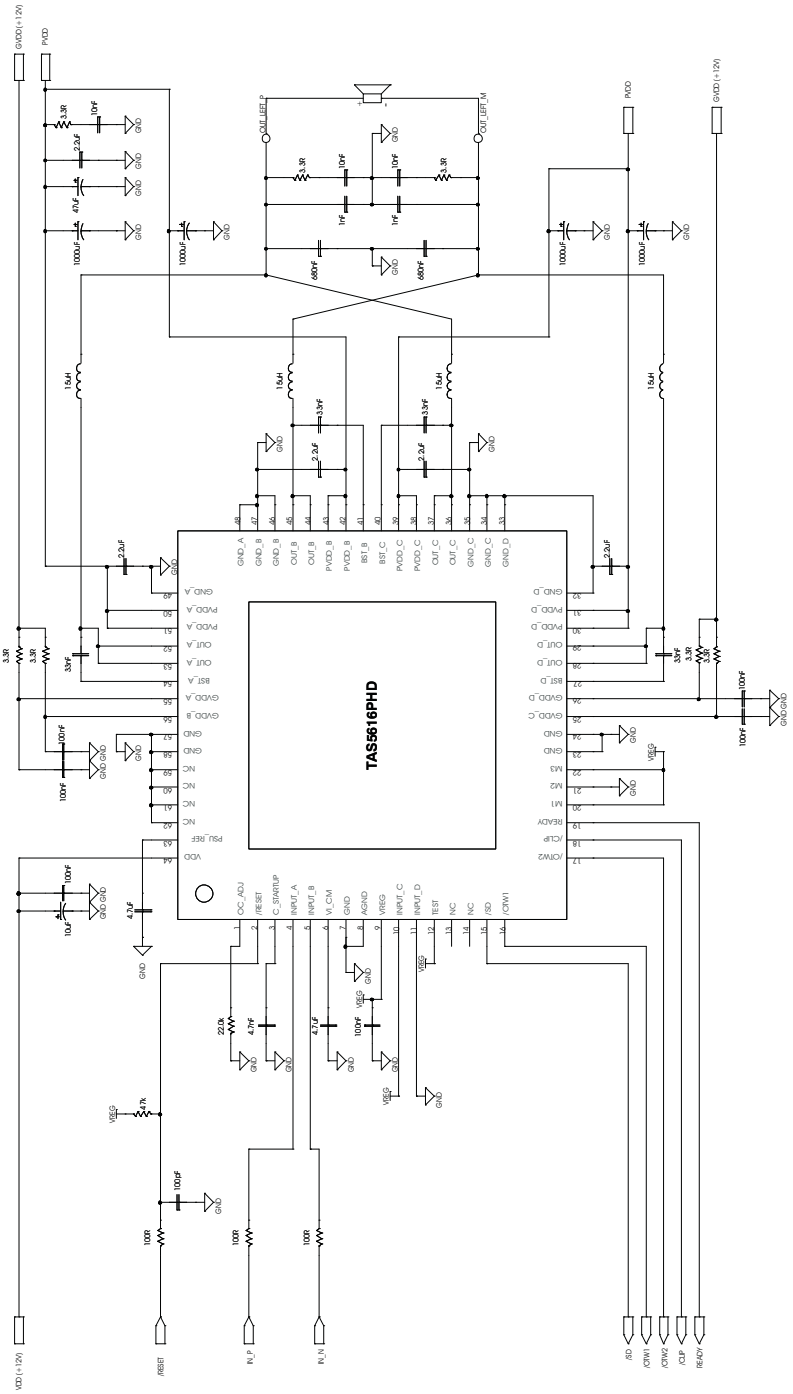

Figure 15. Typical (2N) PBTL Application With AD Modulation Filters

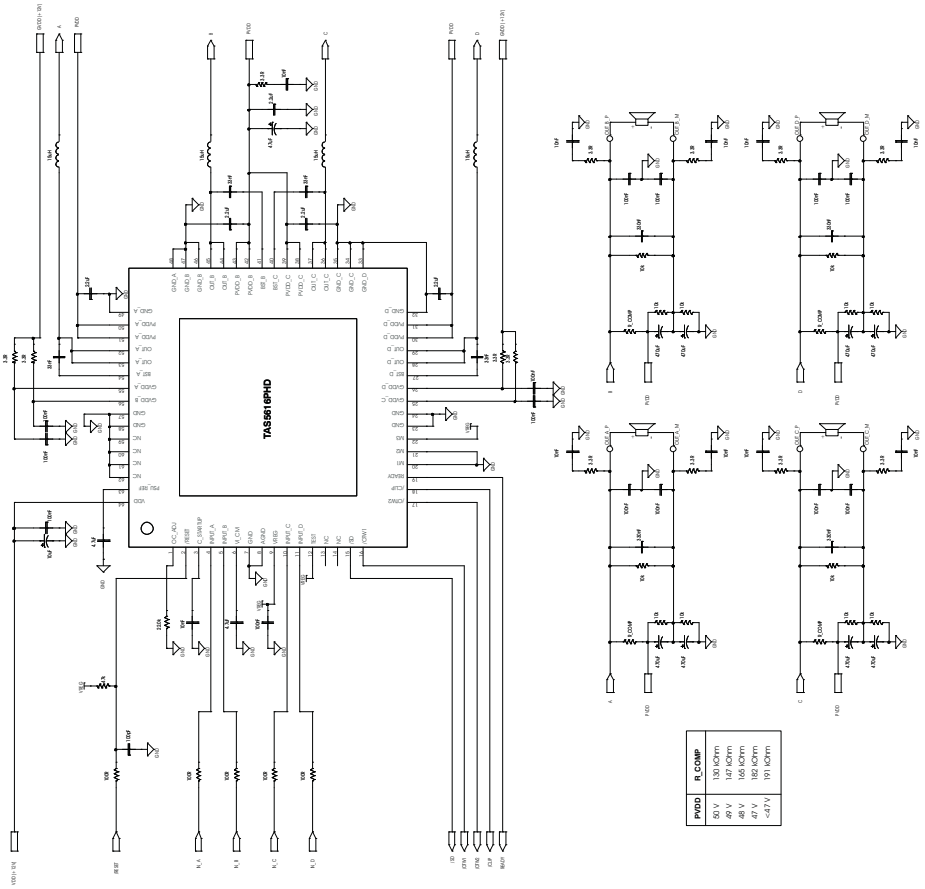

Figure 16. Typical SE Application

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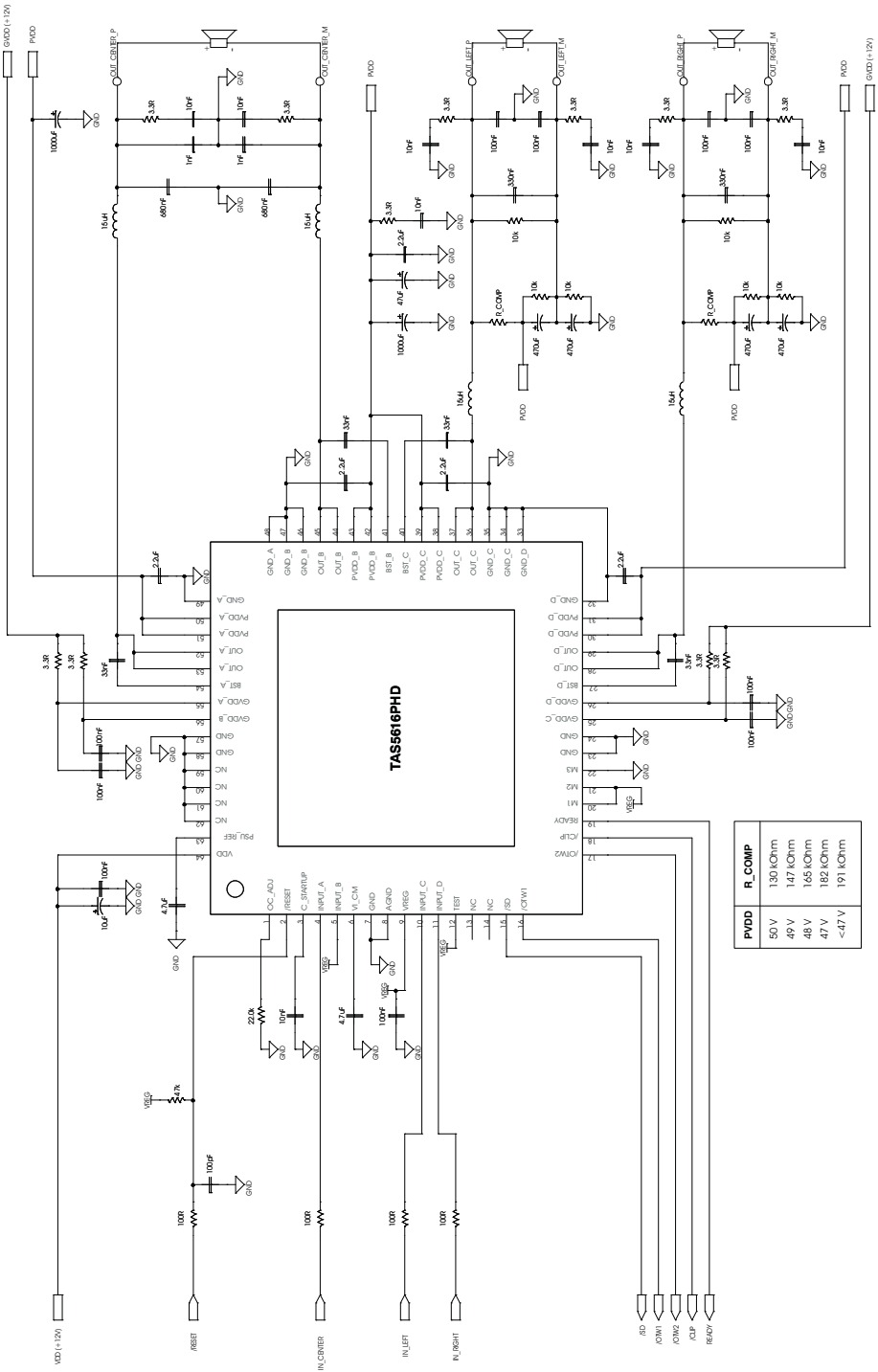

Figure 17. Typical 2.1 System (2N) Input BTL and (1N) Input SE Application

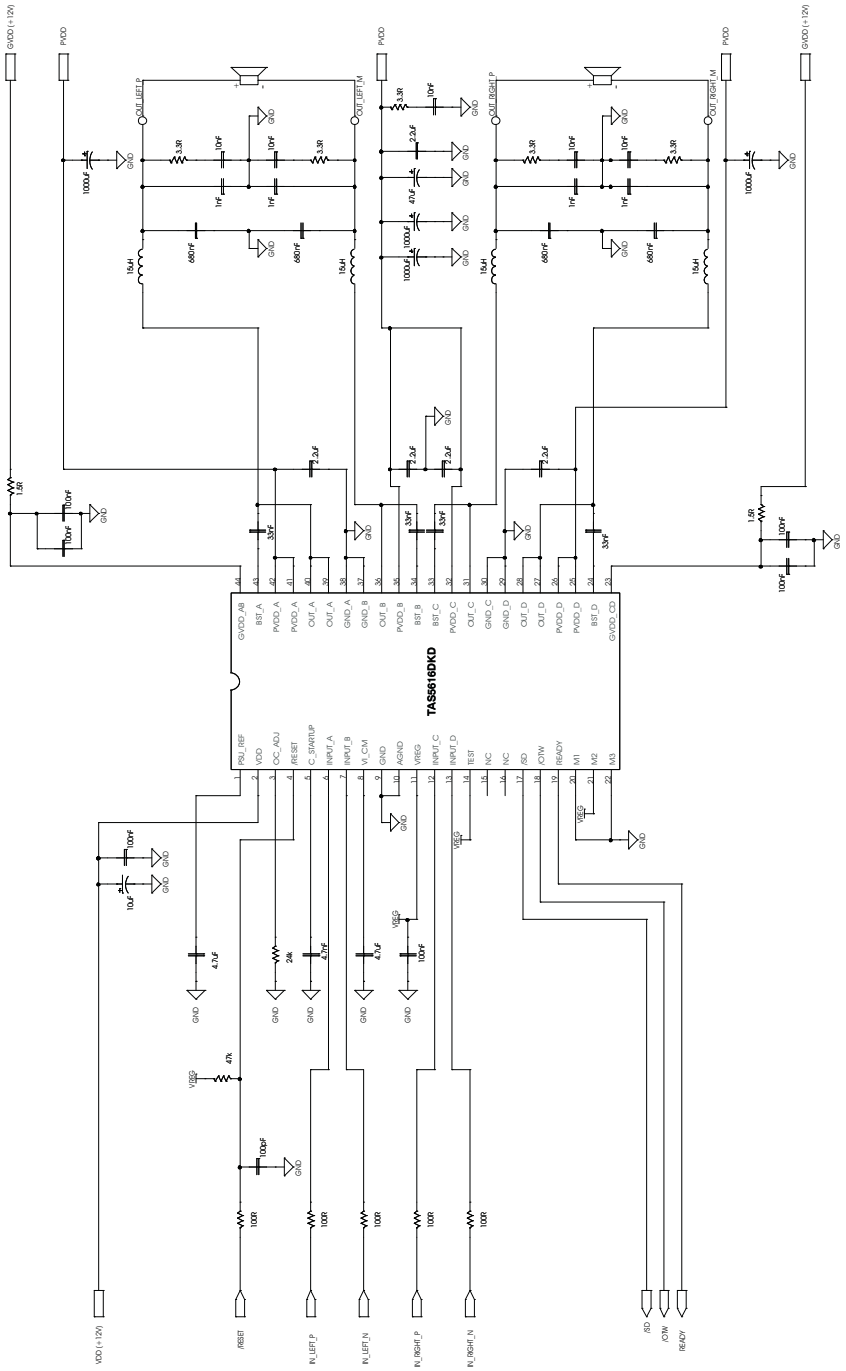

Figure 18. Typical Input BTL Application and BD Modulation Filters DKD Package

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THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5616 needs only a 12V supply in addition to the (typical) 50V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300kHz to 400kHz, it is recommended to use 33nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2.2μF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5616 reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 12V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5616 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5616 does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5616 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks.

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ERROR REPORTING

The $\overline{SD}$, $\overline{OTW}$, $\overline{OTW1}$ and $\overline{OTW2}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ and $\overline{OTW2}$ goes low when the device junction temperature exceeds 125°C and $\overline{OTW1}$ goes low when the junction temperature exceeds 100°C (see the following table).

$\overline{SD}$	$\overline{OTW1}$	$\overline{OTW2}$, $\overline{OTW}$	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{RESET}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the Electrical Characteristics table of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5616 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5616 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{SD}$ pin low. In situations other than overload and over-temperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device will function on errors, as shown in the following table.

BTL MODE		PBTL MODE		SE MODE	
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
A	A+B	A	A+B+B+D	A	A+B
B		B		B	
C	B+D	C		C	B+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge.

PIN-TO-PIN SHORT CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison the OC protection system detects an over current after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The

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typical duration is < 15 ms/μF. While the PPSC detection is in progress, SD is kept low, and the device will not react to changes applied to the RESET pins. If no shorts are present the PPSC detection passes, and SD is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

The two different package options have individual over-temperature protection schemes.

PHD Package

The TAS5616 PHD package option has a three-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW1}$) when the device junction temperature exceeds 100°C (typical), ($\overline{OTW2}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{RESET}$ must be asserted. Thereafter, the device resumes normal operation.

DKD Package

The TAS5616 DKD package option has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{RESET}$ must be asserted. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5616 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the Electrical Characteristics Table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the SD output, i.e., SD is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of SD.

SYSTEM DESIGN CONSIDERATION

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

Apply only audio when the state of READY is high that will start and stop the amplifier without having audible artifacts that is heard in the output transducers. If an overcurrent protection event is introduced the READY signal goes low hence filtering is needed if the signal is intended for audio muting.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply controlling a low and a high rail.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

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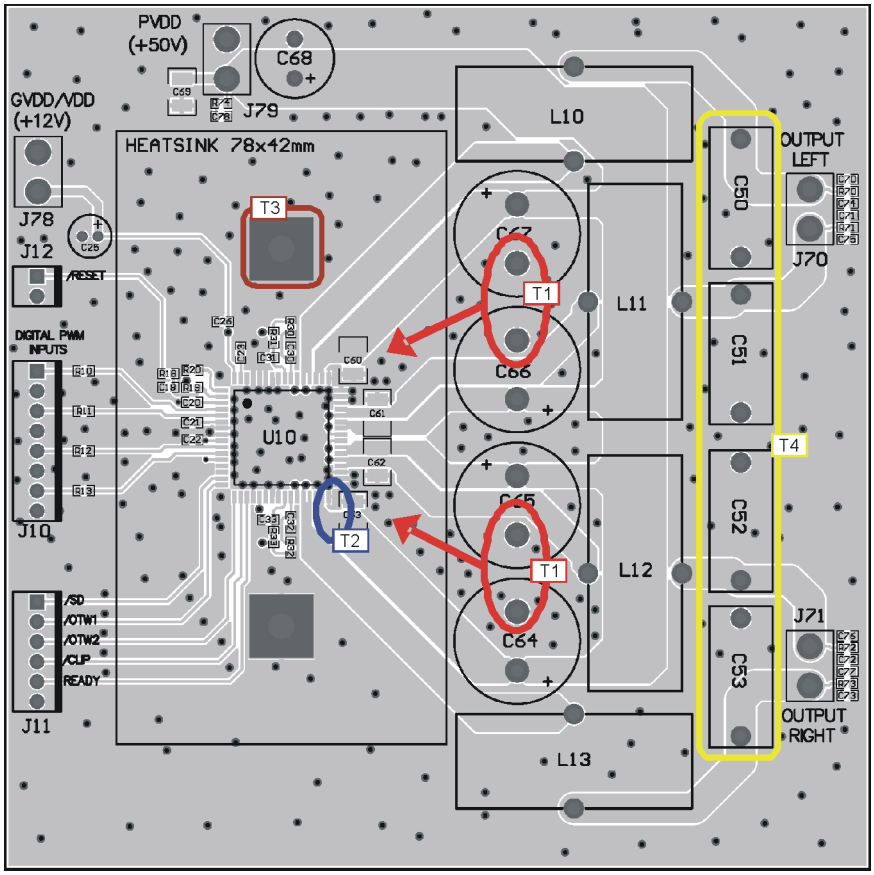
PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high fast switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing the audio input should be kept short and together with the accompanied audio source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce.

Netlist for this printed circuit board is generated from the schematic in Figure 14.



Note T1: PVDD decoupling bulk capacitors C60-C64 should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

Note T3: Heat sink needs to have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range preferable metal film types.

Figure 19. Printed Circuit Board - Top Layer

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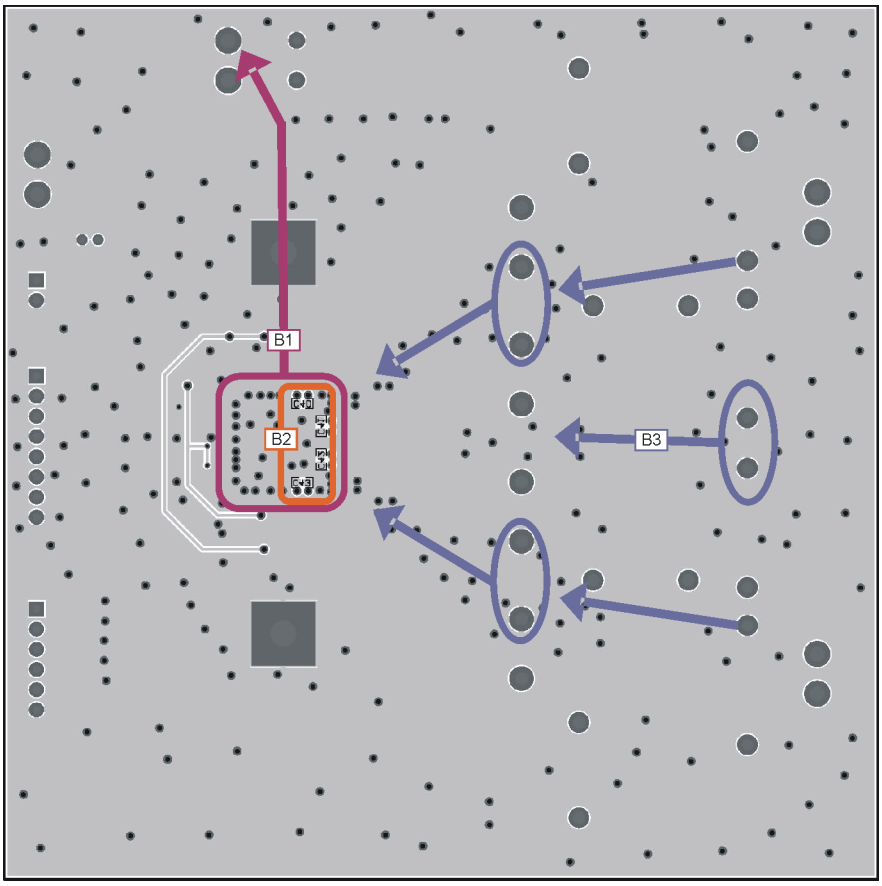

Note B1: It is important to have a direct low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low impedance X7R ceramic capacitors placed on bottom side providing a short low inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors.

Figure 20. Printed Circuit Board - Bottom Layer

REVISION HISTORY

Changes from Original (June 2009) to Revision A — **Page**

- Deleted Product Preview from the PHD package 3

Changes from Revision A (September 2009) to Revision B — **Page**

- NC pin function changed from "I/O" to "—" 5
- OLPC typical value changed from 1.3 ms to 2.6 ms 9
- Changed error-reporting bits from 010 to 011 22

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5616DKD	NRND	HSSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-4-260C-72 HR	0 to 70	TAS5616	
TAS5616DKDR	NRND	HSSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-4-260C-72 HR	0 to 70	TAS5616	
TAS5616PHD	NRND	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-5A-260C-24 HR	0 to 70	TAS5616	
TAS5616PHDR	NRND	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-5A-260C-24 HR	0 to 70	TAS5616	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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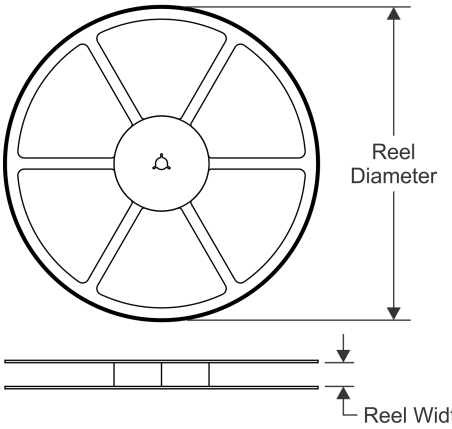
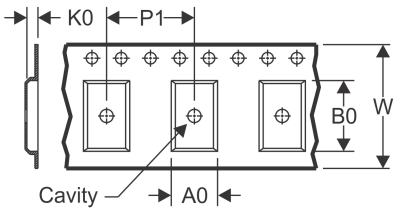
TAPE AND REEL INFORMATION

REEL DIMENSIONS

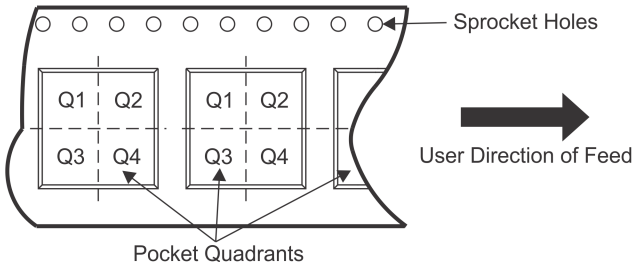


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

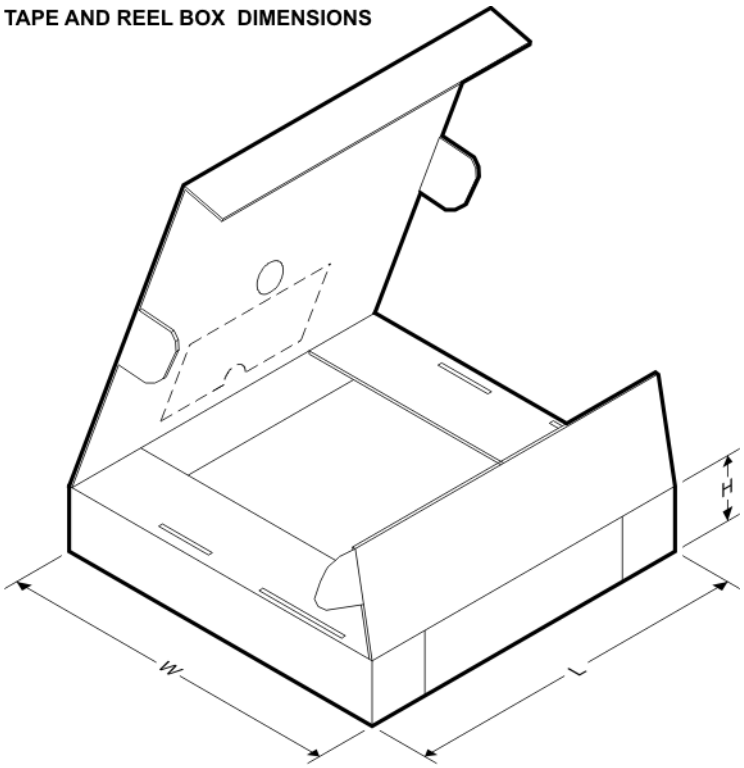
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5616DKDR	HSSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5616PHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



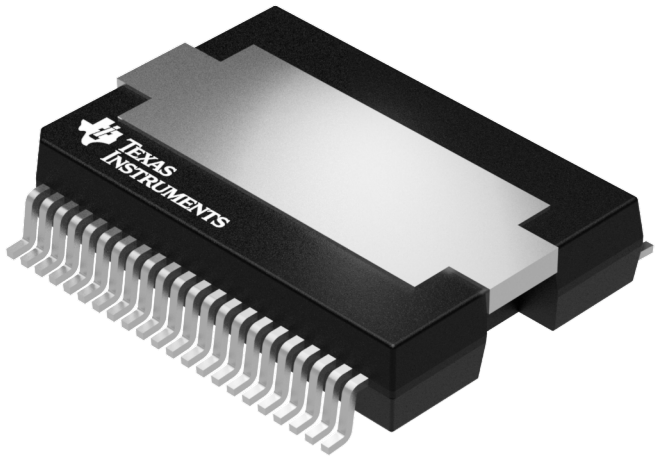
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5616DKDR	HSSOP	DKD	44	500	367.0	367.0	45.0
TAS5616PHDR	HTQFP	PHD	64	1000	367.0	367.0	45.0

GENERIC PACKAGE VIEW

DKD 44 PowerPAD™ HSSOP - 3.6 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

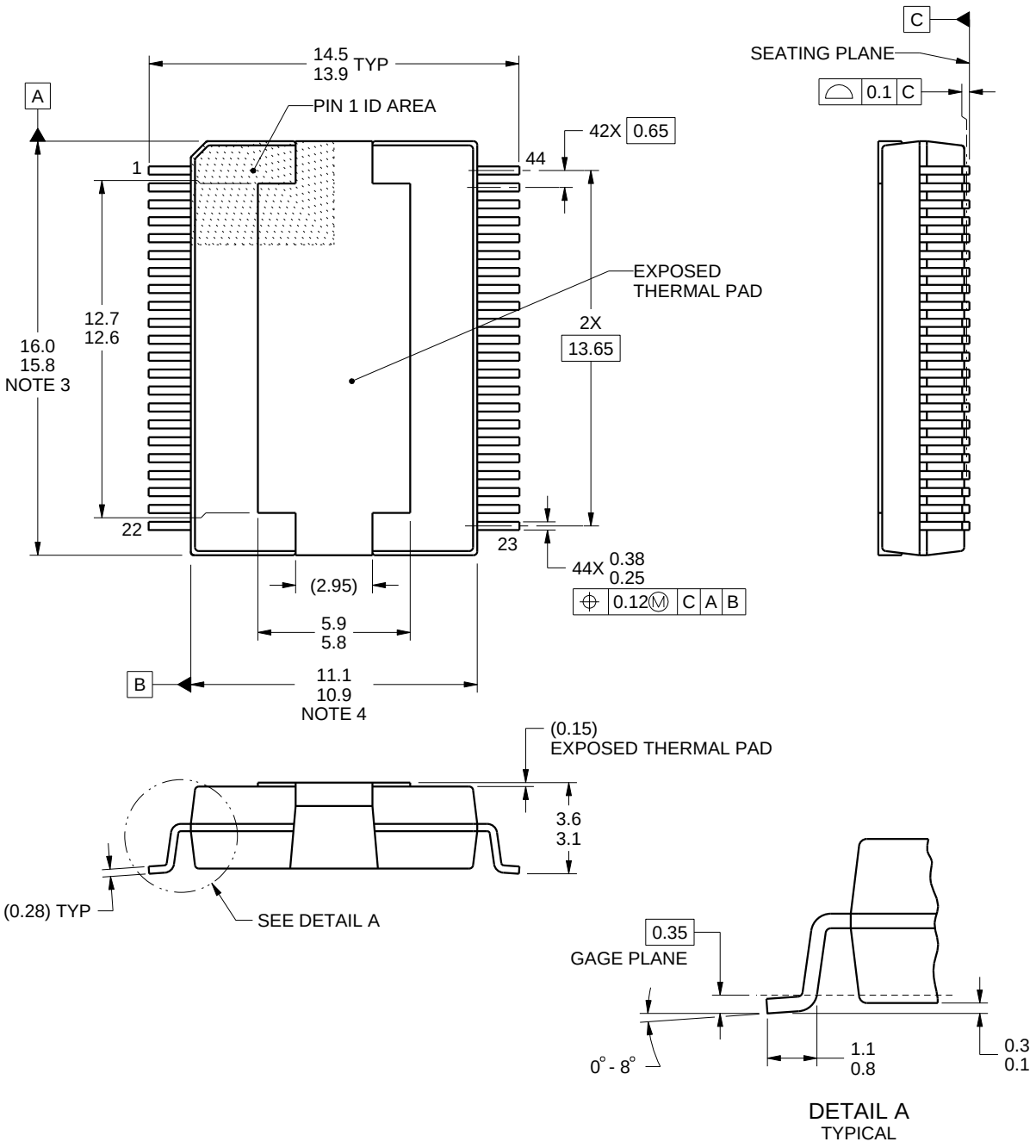
4204421-3/N

PACKAGE OUTLINE

DKD0044A

PowerPAD™ SSOP - 3.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

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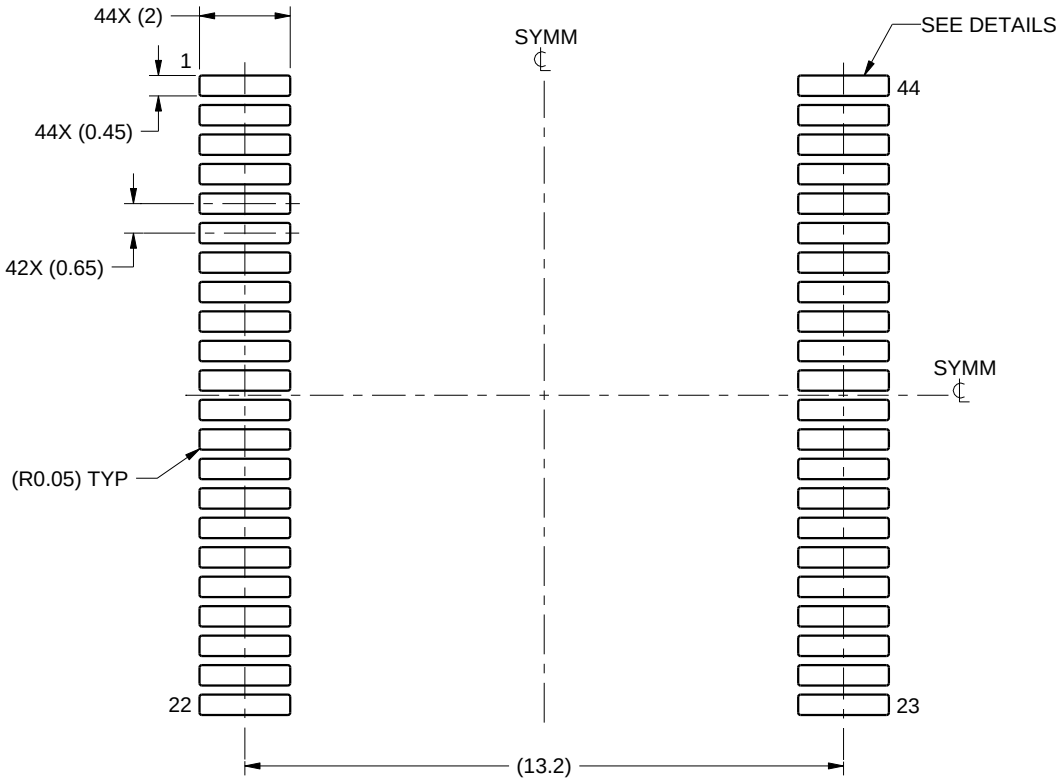
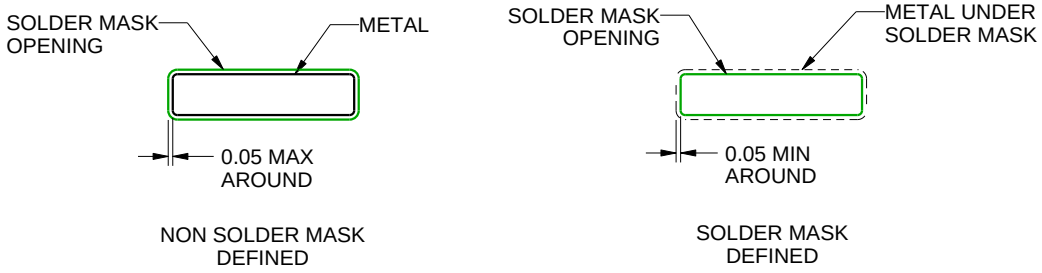
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. The exposed thermal pad is designed to be attached to an external heatsink.



LAND PATTERN EXAMPLE
SCALE:6X

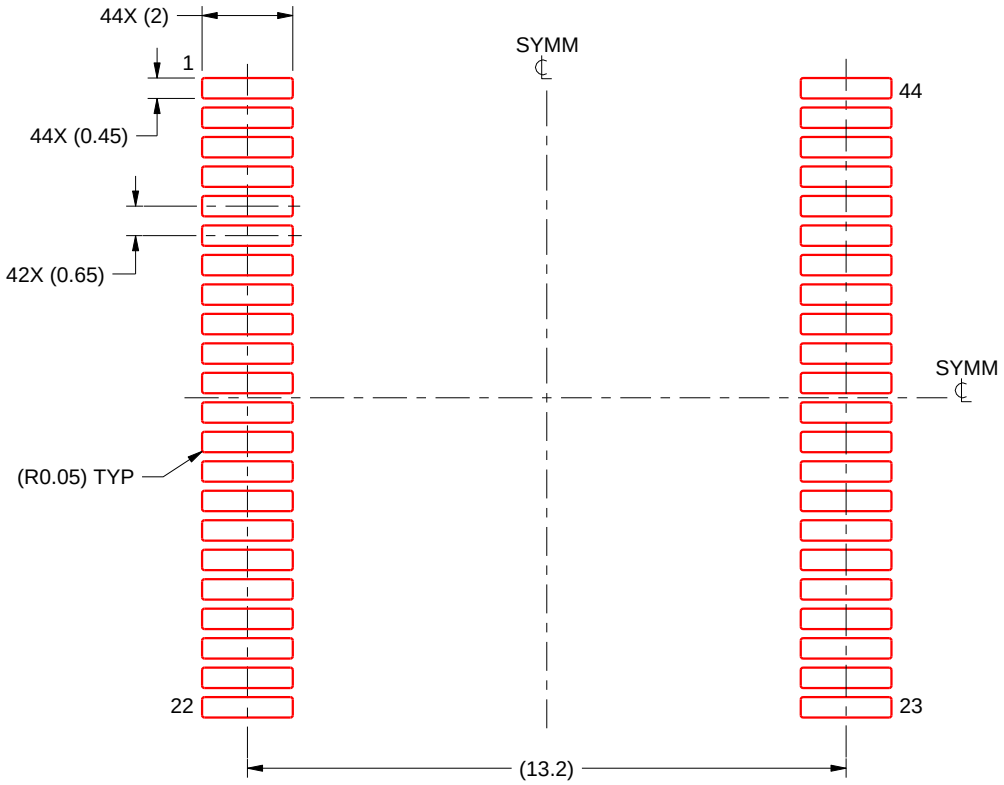


SOLDER MASK DETAILS
NOT TO SCALE

4218846/A 07/2016

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



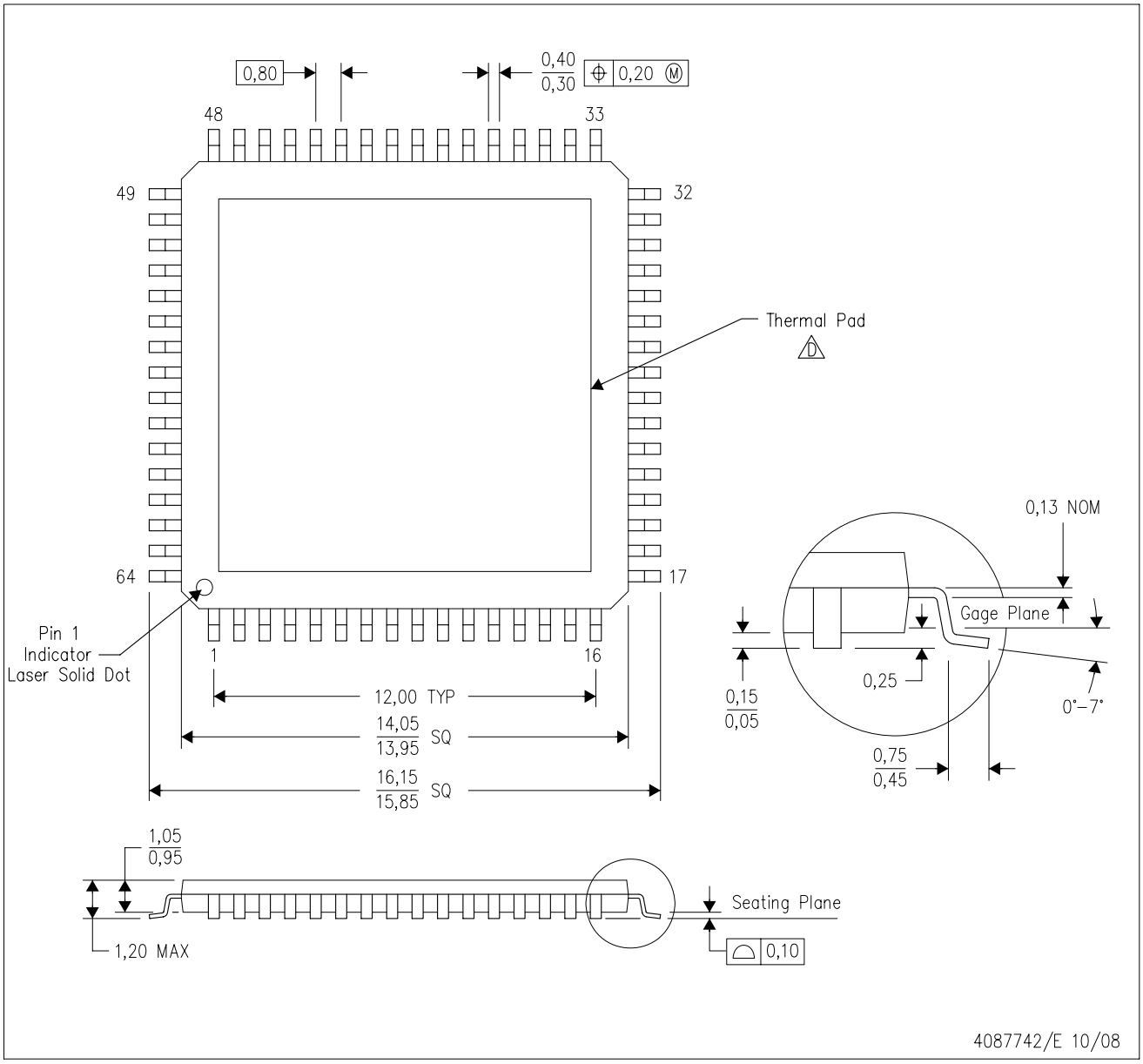
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

4218846/A 07/2016

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

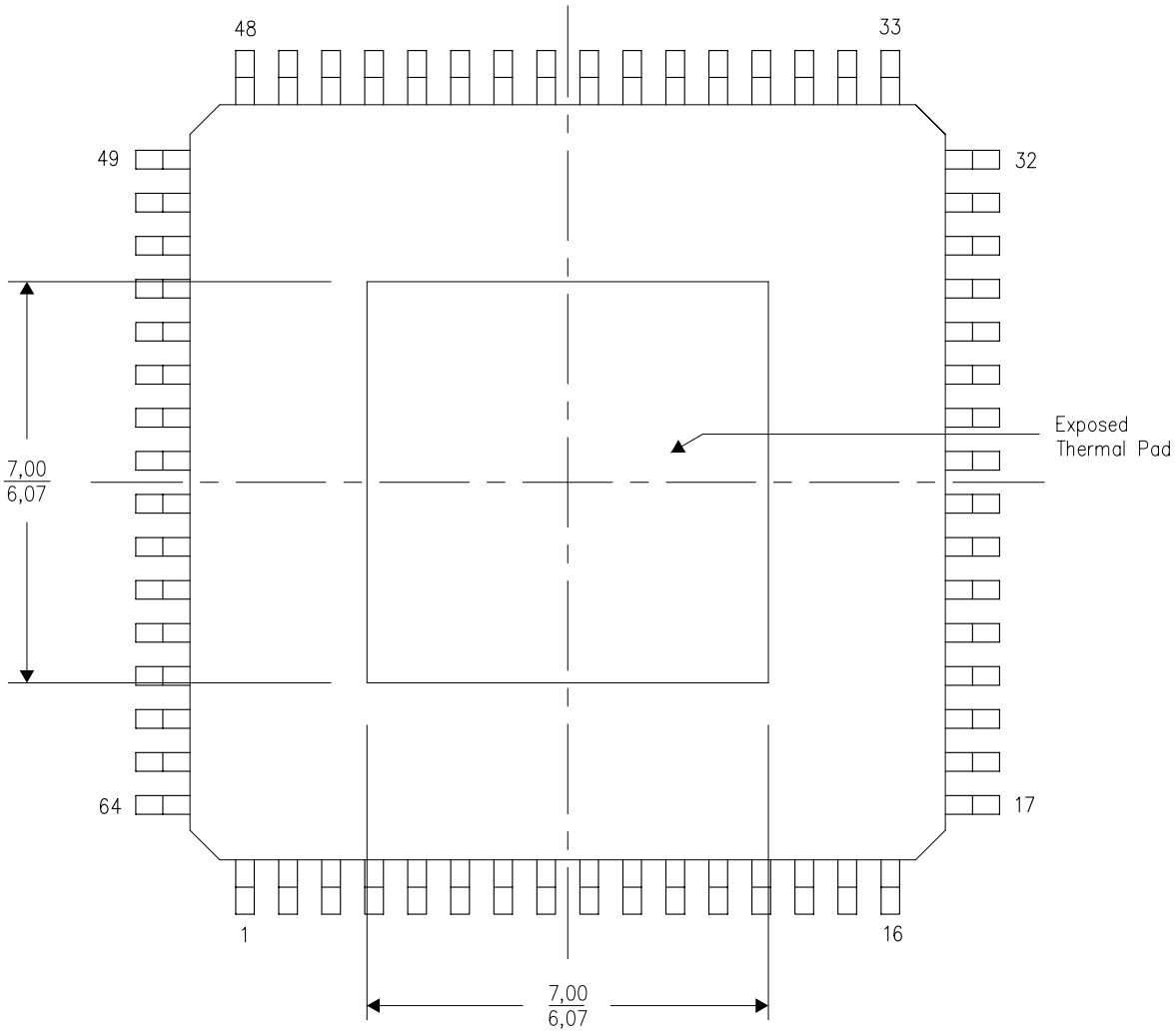
PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206328–4/H 04/11

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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