TAT8801A1H

75 Ω CATV Output Stage Amplifier

Applications

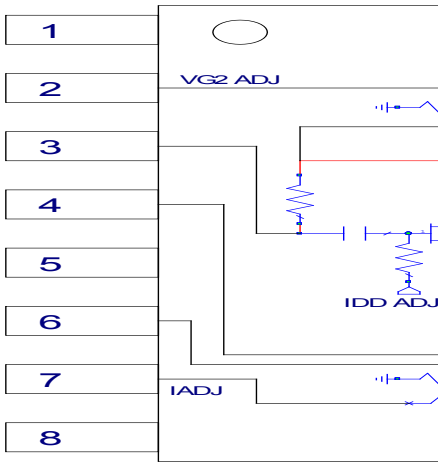
- CATV Line Amplifiers
- HFC Nodes
- Head End Equipment

16-pin SOIC Wide Body Package
with backside ground paddle

Product Features

- Wide Bandwidth (40 MHz – 1 GHz)
- 100% production tested for 80 Ch. NTSC.
- Low Distortion Variation Over Temperature and Production Lots
- In-package ESD Protection
- Flat Gain
- High Power Compression
- Excellent Input / Output Match
- Low DC Power Consumption
- Bias Optimization Through External Voltage

Functional Block Diagram



General Description

The TAT8801A1H is a high power, high linearity GaAs MMIC amplifier intended for output stage amplification in CATV infrastructure applications. Featuring a single die design and providing flat gain with low distortion, this amplifier is ideal for use in CATV distribution systems requiring high output powers and low distortion.

The TAT8801A1H draws 585 mA from a +12 V supply Bias current and voltage may be adjusted externally to optimize output performance for specific applications.

The TAT8801A1H integrates two TQP200002 ESD protection devices that provide bi-directional protection with very low leakage currents and extremely low capacitance. A common mode tuning element within the package allows for improved second order distortion performance.

The TAT8801A1H is packaged in an industry standard 16 pin SOIC WB package.

Pin Configuration

Pin No.	Label
1, 5, 8-9, 12-13, 16	N/C
4	SP TUNE
2	VG2 ADJ
3 / 6	RFIN1 / RFIN2
7	IDD ADJ
10	VDD
11 / 14	RFOUT2 / RFOUT1
15	VDD

Ordering Information

Part No.	Description
TAT8801A1H	CATV Output Stage Amplifier
TAT8801A1H-PCB	40 – 1000 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to 150 °C
Device Voltage (V_{DD})	+16 V
Device Current (I_{DD})	700 mA
RF Input Power (single tone)	75 dBmV

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+11.7	+12	+12.3	V
Case Temperature	−40		+85	°C
Tj for >10^6 hours MTTF			150	°C

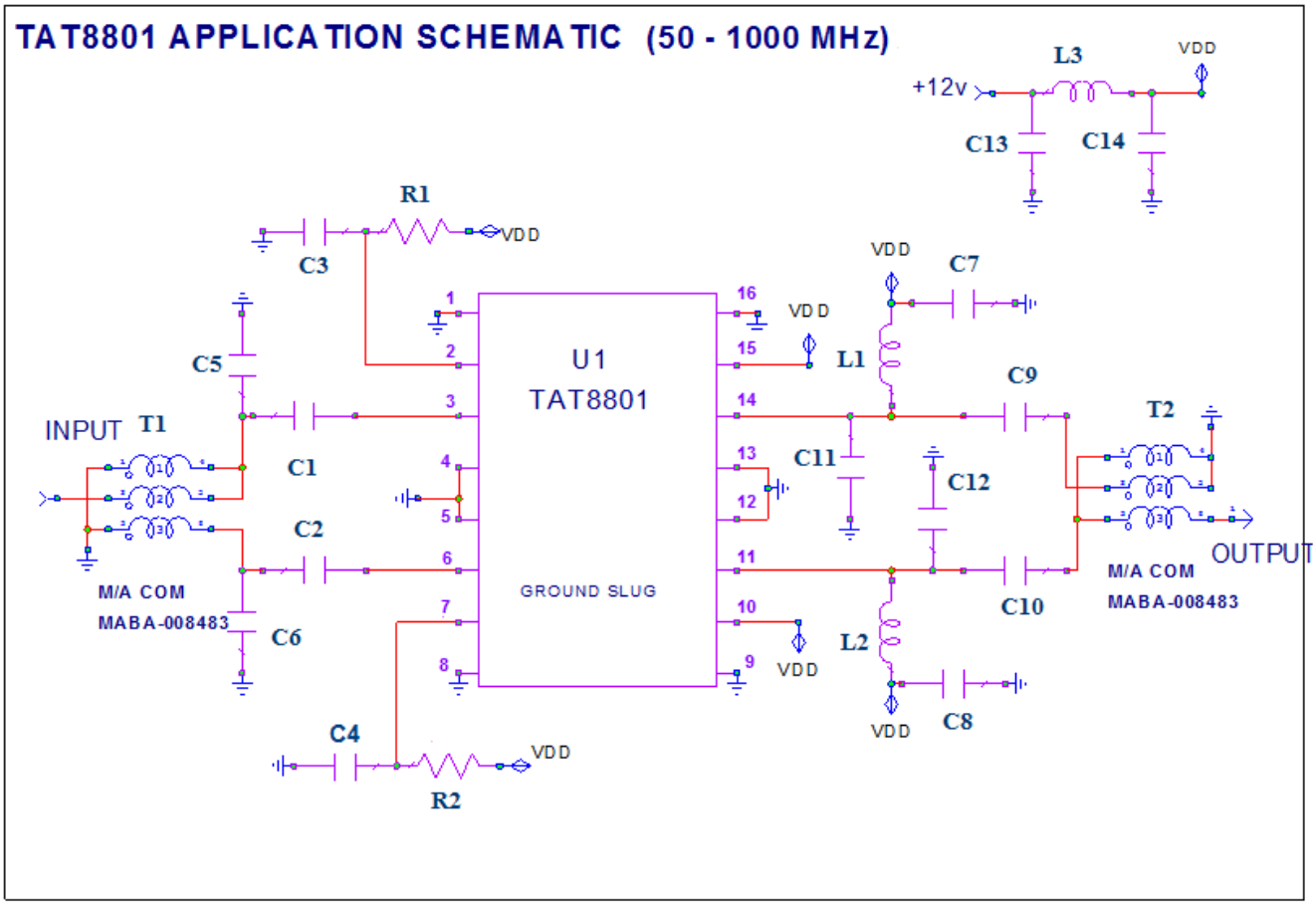
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +12 V, I_{CC} = 585 mA (typ.), $T_{AMBIENT}$ = +25 °C, 75 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		40		1000	MHz
Current			585		mA
Gain		10.5	11.2	11.7	dB
Gain Flatness(1)	Peak deviation from least squared fit curve.		±0.25	±0.3	dB
Gain Slope		−0.5		+0.5	dB
Input Return Loss		14	17		dB
Output Return Loss		17	18		dB
CSO	80 Ch. NTSC, + 56 dBmV/ch at 1002 MHz, 15.6 dB tilt, QAM from 553 MHz to 1002 MHz at 6 dB offset.		−69		dBc
CTB			−72		dBc
XMOD			−72		dBc
CIN			56		dB
Output P1dB			+34		dBm
Output IP3	f_1=225 MHz, f_2=325 MHz, Pout =+17 dBm/tone		+49		dBm
Thermal Resistance, θjc	Junction to case		8.1		°C/W

Application Circuit Schematic – TAT8801A1H-PCB

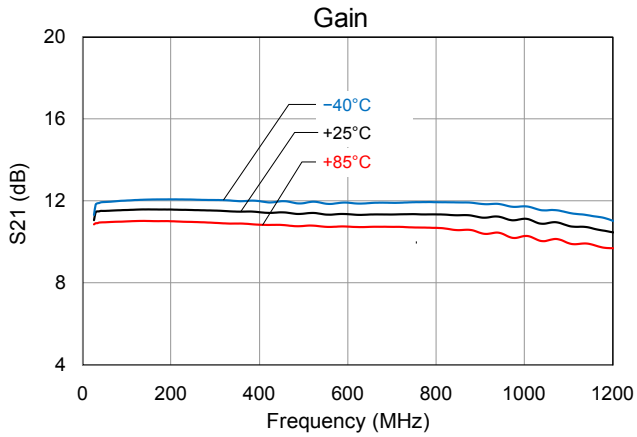


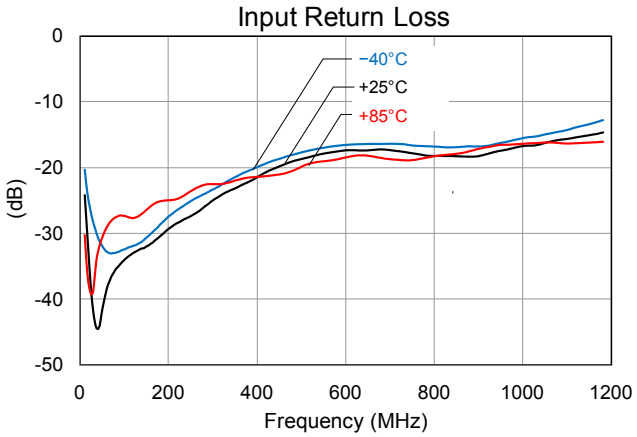
Bill of Material – TAT8801A1H-PCB

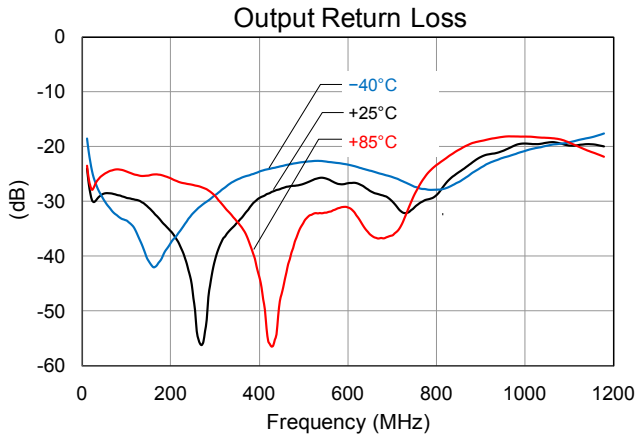
Reference	Value	Description	Manuf.	Part Number
U1	--	40 MHz – 1 GHz, CATV Gain Block	TriQuint	TAT8801A1H
C1, C2, C3, C4	0.01 uF	Cap, Chip, 0402, 16V, 10%	Various	
C5, C6	0.5 pF	Cap, Chip, 0402, 25V, +/-0.05	Various	
C7, C8, C13, C14	0.01 uF	Cap, Chip, 0603, 25V, 5%, X7R	Various	
C9, C10	330 pF	Cap, Chip, 0402, 50V, 10%, X7R		
C11, C12	0.7 pF	Cap, Chip, 0402, 25V, +/-0.075, NPO/COG	Various	
R1	1.82 kΩ	Res, Chip, 0402, 1%, 1/16W	Various	
R2	1.6 kΩ	Res, Chip, 0402, 1%, 1/16W	Various	
L1, L2	500 nH	Ind, Chip, Ferrite, 1206, 10%, 260mA	Murata	LQH31HNR50K03
L3	0.9 uH	Ind, Chip, 1008, 5%, 1.4A	Coilcraft	1008AF-901XJL
TX1, TX2	1:1	SMT, 75 OHM, BALUN 1:1, TLINE, SM-118A, RoHS	M/A-COM	MABA-008483-CT1760

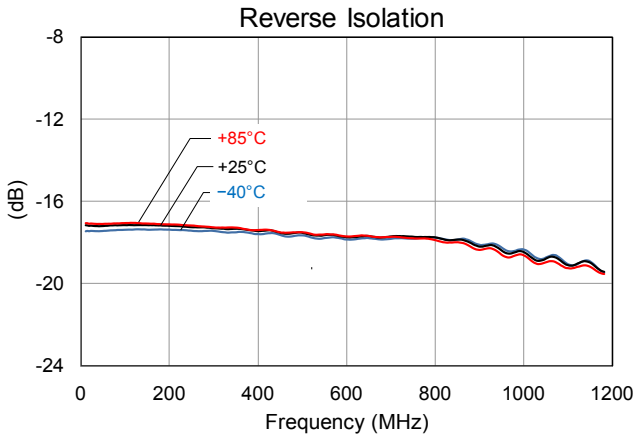
Performance Plots – TAT8801A1H-PCB

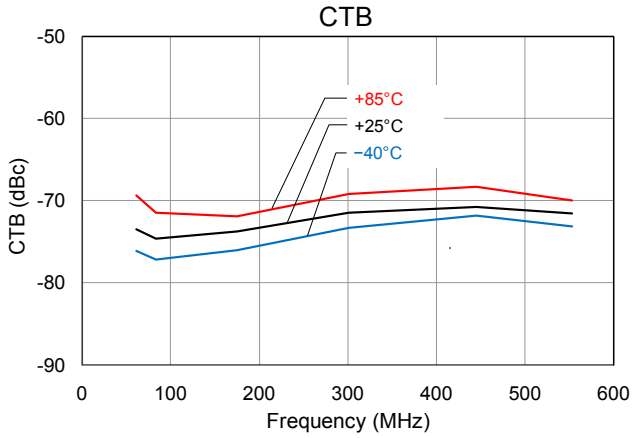
Test conditions unless otherwise noted: V_{DD} = +12 V, I_{CC} = 585 mA (typ.)

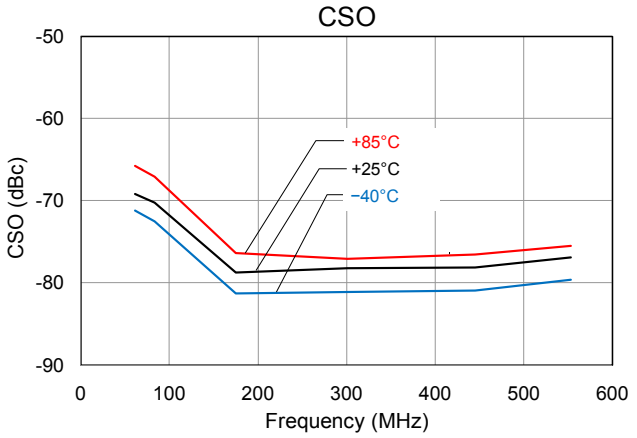








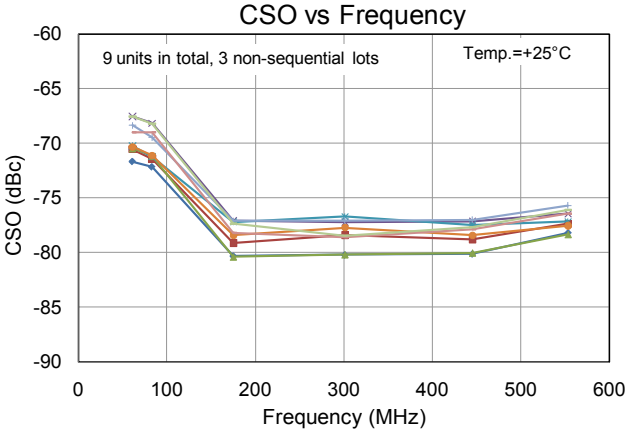




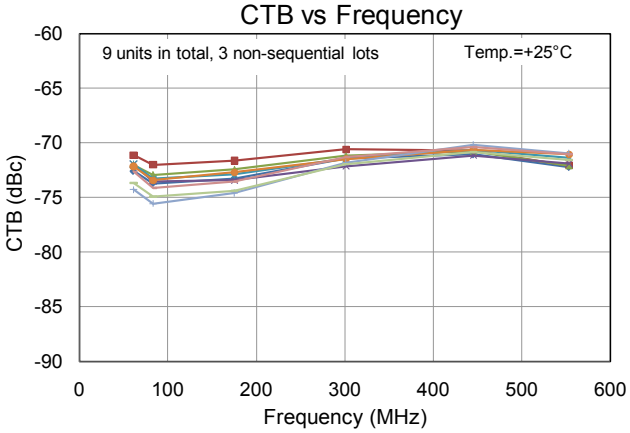
Distortion Performance: Lot to Lot Variation Over Temperature

Test conditions unless otherwise noted: V_{DD} = +12 V, I_{CC} = 585 mA (typ.)

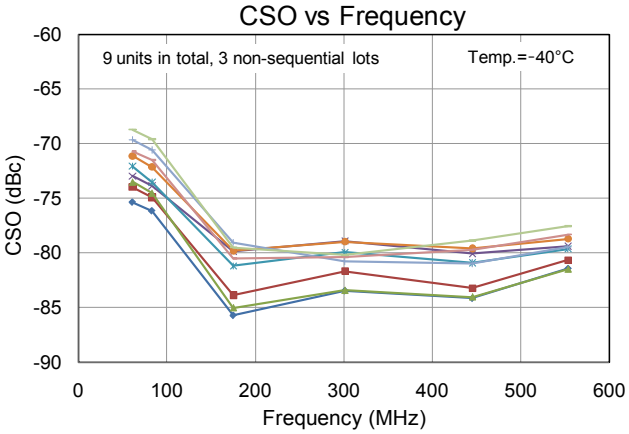
CSO vs Frequency



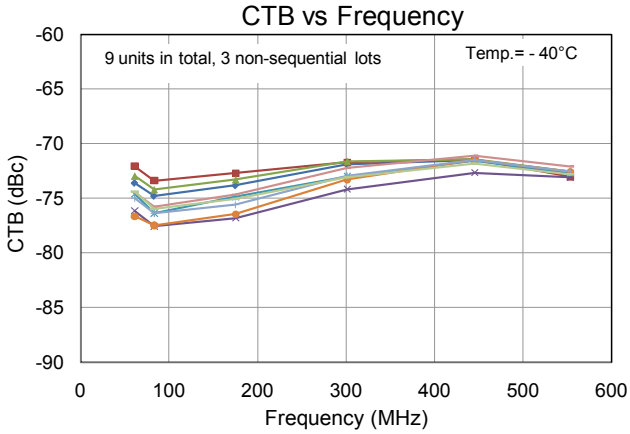
CTB vs Frequency



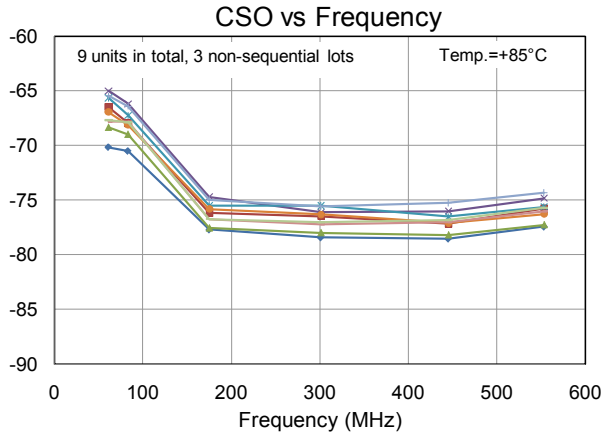
CSO vs Frequency



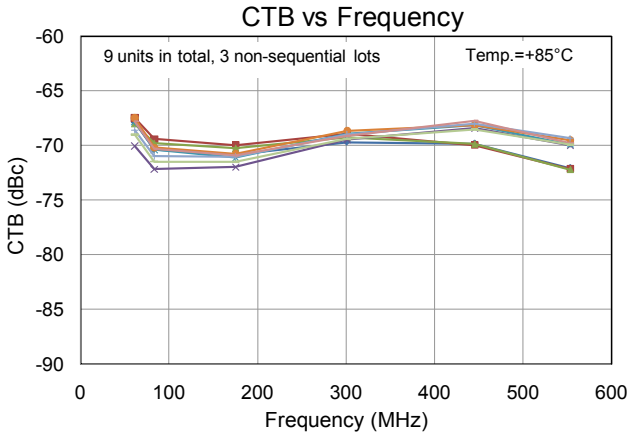
CTB vs Frequency



CSO vs Frequency

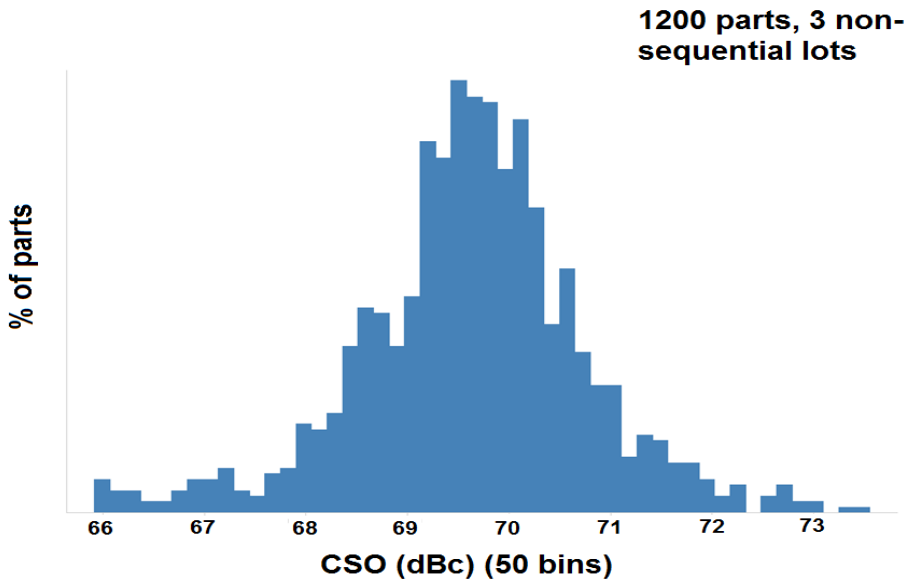


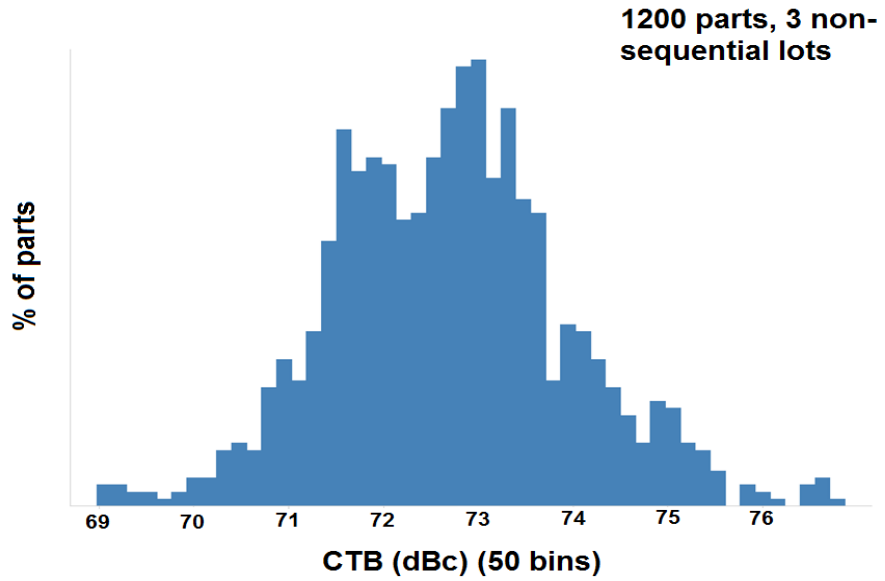
CTB vs Frequency



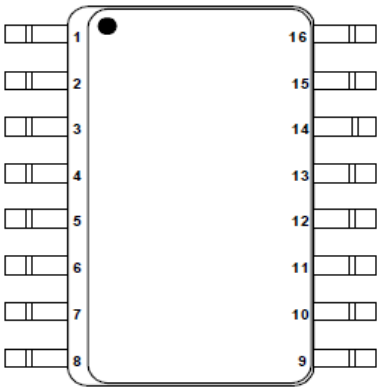
Distortion performance: Variation over production volumes

Measured using production test fixture and 1200 parts from 3 non-sequential lots.





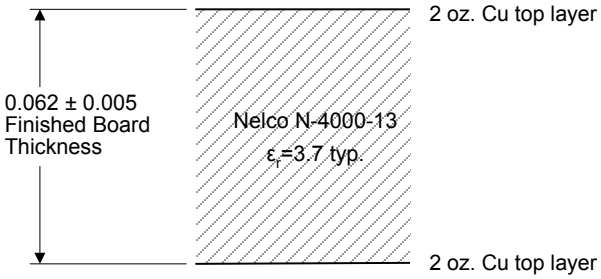
Pin Configuration and Description

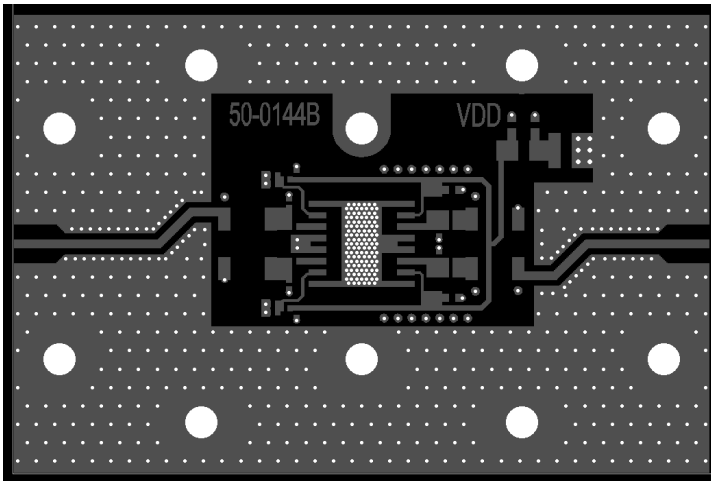


Pin No.	Label	Description
1, 8-9, 12-13, 16	N/C	RF/DC ground. Grounded to backside paddle on PCB.
4	SP TUNE	Connected to internal common-mode tuning element inside package. Pin 4 normally grounded on PCB through vias. May ground Pin 4 to PCB through an RF bead or an inductor to further improve CSO performance.
5	N/C	RF/DC ground. Grounded on PCB through vias.
2	VG2 ADJ	Dropping resistor and bypass capacitor required.
3 / 6	RFINA / RFINB	RF Input A / RF Input B. Impedance matching required
7	IADJ	IDD current adjustment
10	VDD	VDD supply for internal biasing
11 / 14	RFOUTB / RFOUTA	RF Output / DC supply. Impedance matching , DC block and bias choke required
15	VDD	VDD supply for internal biasing
Backside Pad	GND	RF/DC ground.

Evaluation Board PCB Information

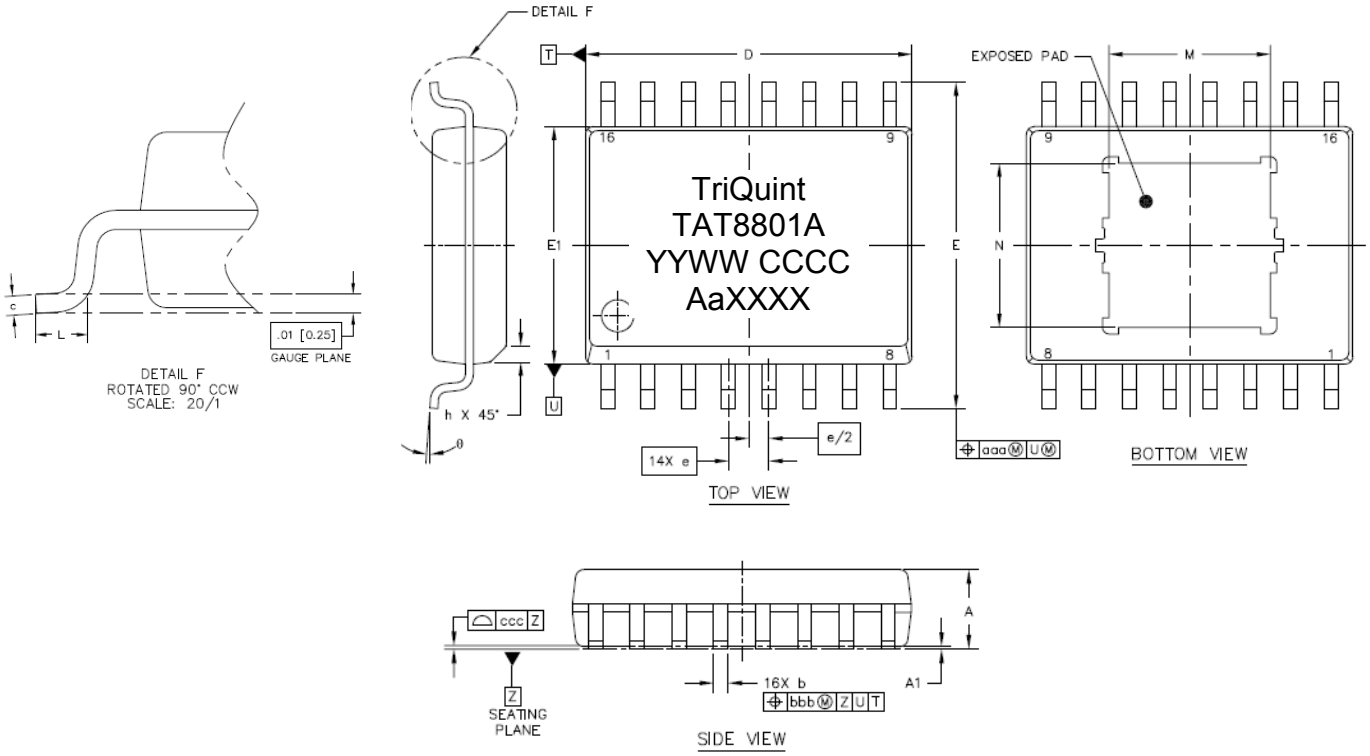
TriQuint Evaluation Board
PCB Materials and Stack Up





Package Marking and Dimensions

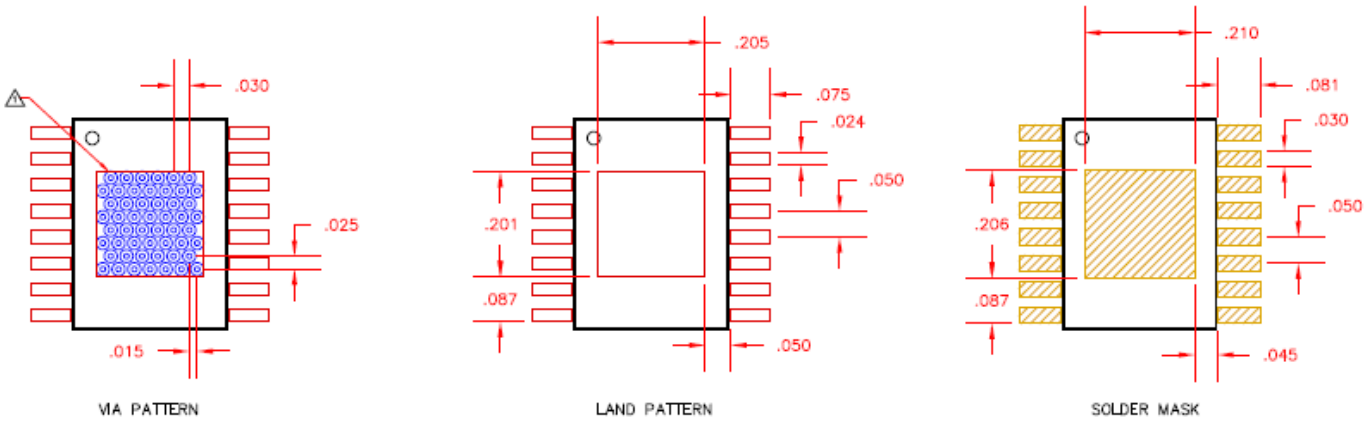
Marking: Part Number – TAT8801A
Year/Week/Country Code – YYWW CCCC
Lot code – AaXXXX



Package Dimensions

	Symbol	MIN	TYP	MAX	MIN	TYP	MAX
TOTAL THICKNESS	A	.087		.098	2.2		2.5
STAND OFF	A1	0		.004	0		0.1
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.009		.013	0.23		0.33
BODY SIZE	D	.400		.411	10.15		10.45
	E1	.291		.299	7.4		7.6
	E	.395		.415	10.05		10.55
LEAD PITCH	e		0.05 BSC			1.27 BSC	
	L	.016		.050	0.4		1.27
	h	.010		.030	0.25		0.75
	θ	0°		8°	0°		8°
EP SIZE	M	.196	.200	.204	4.98	5.08	5.18
	N	.200	.204	.208	5.08	5.18	5.28
LEAD EDGE OFFSET	aaa		.010			0.25	
LEAD OFFSET	bbb		.010			0.25	
COPLANARITY	ccc		.004			0.10	

PCB Mounting Pattern



Notes:

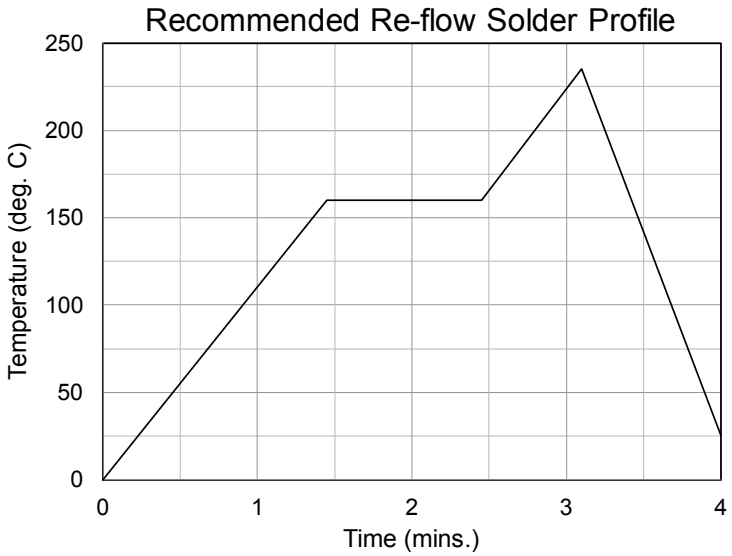
1. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
2. Ensure good package backside paddle solder attach for optimum electrical and thermal performance.
3. All dimensions are in millimeters. Angles are in degrees.

Recommended Solder Re-flow Profile

Solder paste manufacturers will recommend a "typical" solder reflow profile depending on their particular solder paste's flux and metal composition. This typical profile entails the parameters necessary for the solder to properly melt and reflow, and defines the thermal condition of the PCB soldering surface to be within an optimum temperature range. The profile is obtained by mounting a thermo couple directly to the solder surface area of the PCB, and recording the actual local surface temperature during the reflow process.

The solder reflow profile shown at right is for a typical SAC305 lead free solder paste application and assumes that standard PCB layout rules have been followed, such as solder mask to dam in molten solder during reflow to keep it from wicking away from the solder joint.

The "oven profile" required to achieve the "solder reflow profile" will vary depending on reflow equipment, PCB, components loaded on the PCB, and other factors such as fixturing.



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: Passes ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: ESDA/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: Passes ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with J-STD-020, Lead free solder, (260° maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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For technical questions and application information:

Email: sjcapplications.engineering@triquint.com

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