

# **TB-7Z-020-EMC Hardware User Manual**

Rev.1.02

## Revision History

Version	Date	Description	Publisher
Rev 1.00	2013/01/31	Release Version	Yoshioka
Rev 1.01	2013/04/25	Modified Table 7-17 and some typos.	Yoshioka
Rev.1.02	2013/11/13	Modified 7.17 (Description of J6 and J7 was reverse)	Kiguchi

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## Introduction

Thank you for purchasing the TB-7Z-020-EMC board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

### SAFETY PRECAUTIONS

Be sure to observe these precautions




Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

Before using the product, read these safety precautions carefully to assure correct use.

These precautions contain serious safety instructions that must be observed.




After reading through this manual, be sure to always keep it handy.

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

 <b>Danger</b>	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
 <b>Warning</b>	Indicates the possibility of serious injury or death if the product is handled incorrectly.
 <b>Caution</b>	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.

(Examples)



	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.



## Warning

	<p><b>In the event of a failure, disconnect the power supply.</b> If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.</p>
	<p><b>If an unpleasant smell or smoking occurs, disconnect the power supply.</b> If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.</p>
	<p><b>Do not disassemble, repair or modify the product.</b> Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.</p>
	<p><b>Do not touch a cooling fan.</b> As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.</p>
	<p><b>Do not place the product on unstable locations.</b> Otherwise, it may drop or fall, resulting in injury to persons or failure.</p>
	<p><b>If the product is dropped or damaged, do not use it as is.</b> Otherwise, a fire or electric shock may occur.</p>
	<p><b>Do not touch the product with a metallic object.</b> Otherwise, a fire or electric shock may occur.</p>
	<p><b>Do not place the product in dusty or humid locations or where water may splash.</b> Otherwise, a fire or electric shock may occur.</p>
	<p><b>Do not get the product wet or touch it with a wet hand.</b> Otherwise, the product may break down or it may cause a fire, smoking or electric shock.</p>
	<p><b>Do not touch a connector on the product (gold-plated portion).</b> Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.</p>

**Caution**

	<p><b>Do not use or place the product in the following locations.</b></p> <p>Humid and dusty locations          Airless locations such as closet or bookshelf          Locations which receive oily smoke or steam          Locations exposed to direct sunlight          Locations close to heating equipment          Closed inside of a car where the temperature becomes high          Sticky locations          Locations close to water or chemicals          Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.</p>
	<p><b>Do not place heavy things on the product.</b></p> <p>Otherwise, the product may be damaged.</p>

## Disclaimer

This product is an evaluation board for Xilinx Zynq AP SoC FPGA. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- (1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- (2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
- (3) Use of this product against the instructions given in this manual.
- (4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

- (1) Erasure or corruption of data arising from use of this product.
- (2) Any consequences or other abnormalities arising from use of this product, or
- (3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.



## 1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Accessories.

- RS-232C/CAN Bus Cable x1
- microSD card 4GB x1
- Power Supply(DC-12V) x1
- DC Switch Cable x1
- Spacer Set

## 2. Overview

The TB-7Z-020-EMC evaluation board for the Zynq™-7000 All Programmable SoC provides a hardware environment for developing and evaluating designs targeting the Zynq™-7000 XC7Z020-1CLG484. The TB-7Z-020-EMC provides features common to many embedded processing systems, including DDR3 SDRAM component memory, a 10/100/1000 Ethernet PHY, general purpose I/O, a DVI Transmitter, a USB OTG 2.0 Port, a Pmod interface, a CAN interface and a UART interface. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to either of two low pin count (LPC) FMC connectors.

## 3. Feature

Zynq-7000:	Xilinx XC7Z020-1CLG484
Memory:	1GByte (32Mword x 32bit x 8banks) DDR3 SDRAM Component 128Mbit Quad SPI Flash Secure Digital Card (Connector)
Ethernet PHY:	Marvell's 88E1518-XX-NNB2C000 RGMII Interface with RJ45
USB OTG 2.0 Transceiver:	TI's TUSB1210BRHB *1
DVI Complaint Transmitter:	TI's TFP410PAP
RS232 Transceiver:	TI's MAX3232CPW with 2.0 pitch PinHeader*2
FMC Connector:	Samtec's ASP-134604-01 (FMC LPC MC) mounted on bottom side*3 Samtec's ASP-134603-01 (FMC LPC CC) mounted on top side*3 <b>Cation: FMC connetors are only exclusice use</b>
CAN Bus Transceiver:	PHILIPS's TXS0104EPWR with 2.0 pitch PinHeader*2
Pmod Connector:	Digilent Pmod™ compatible headers (2x6)
JTAG Port:	Standard Xilinx JTAG Interface with 14-pin 2.0 pitch PinHeader ARM JTAG + Logic Analyzer function Interface with Mictor-38 Connector
SD Card:	microSD Card connector
Oscillators:	Fixed 33.33333MHz LVCMOS oscillator
Clock Generator:	IDT's 5V49EE504NLGI

**Note \*1: TUSB1210 and Zynq-7000 have a timing incompatibility at hot temperature.**

**Please use TB-7Z-020-EMC at room temperature.**

**Note \*2: Rs-232C and CAN interfaces are connecting by accessory cable.**

**Note \*3: FMC connetors are only exclusice use.**

## 4. Block Diagram

The TB-7Z-020-EMC board block diagram is shown in [Figure 4-1](#) ~~Figure 4-4~~.

PS block is connecting specific memories or interfaces.

PL block is connecting FMC connector and debug interfaces.

For more detail, please refer to each peripheral section

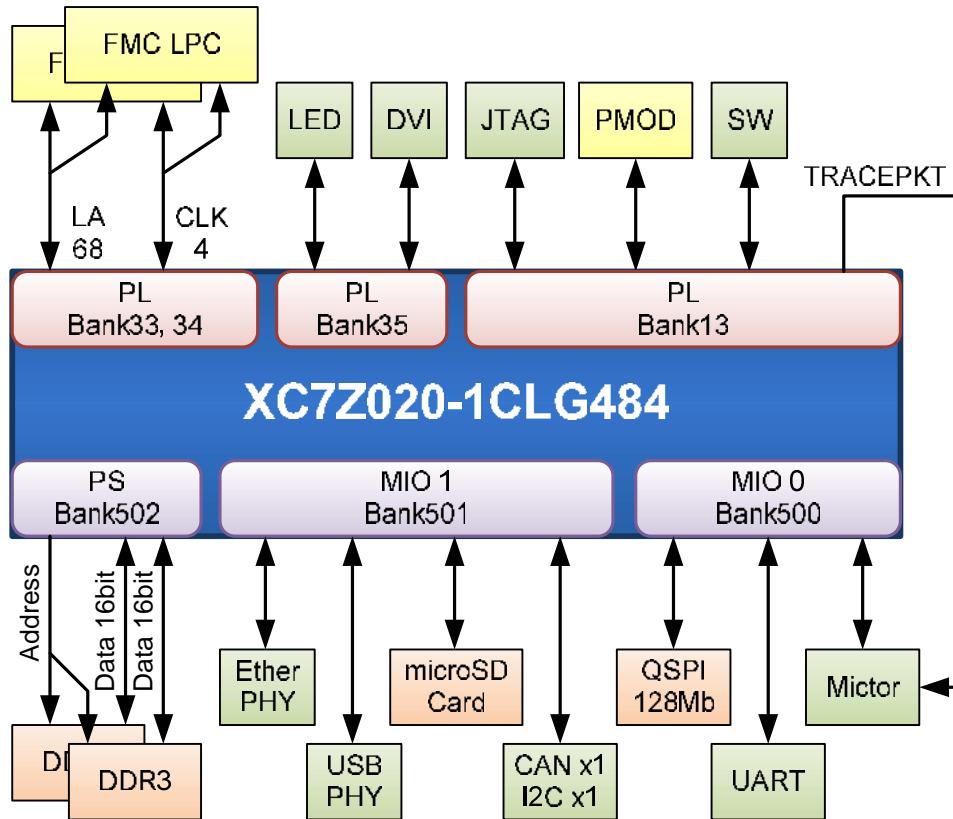


Figure 4-1 Block Diagram

## 5. External View of the Board

The TB-7Z-020-EMC board external view is shown in Figure 5-1 and Figure 5-2.

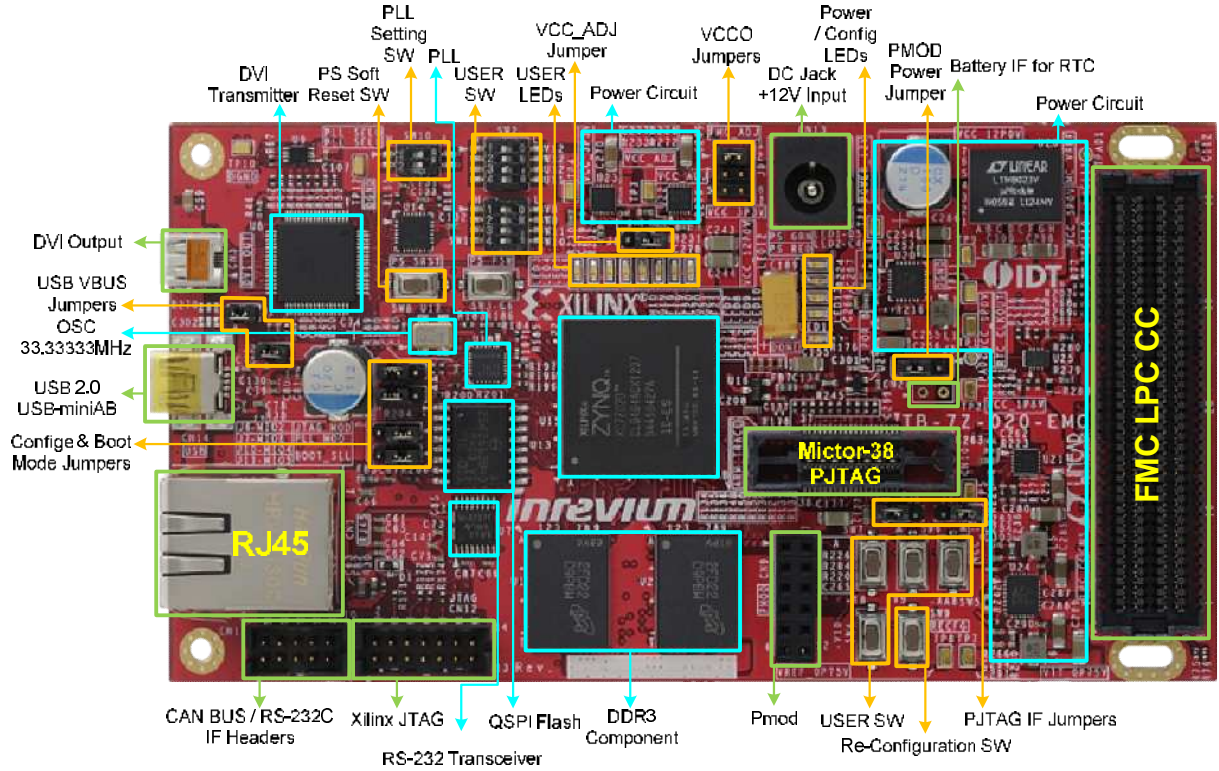


Figure 5-1 Component Side

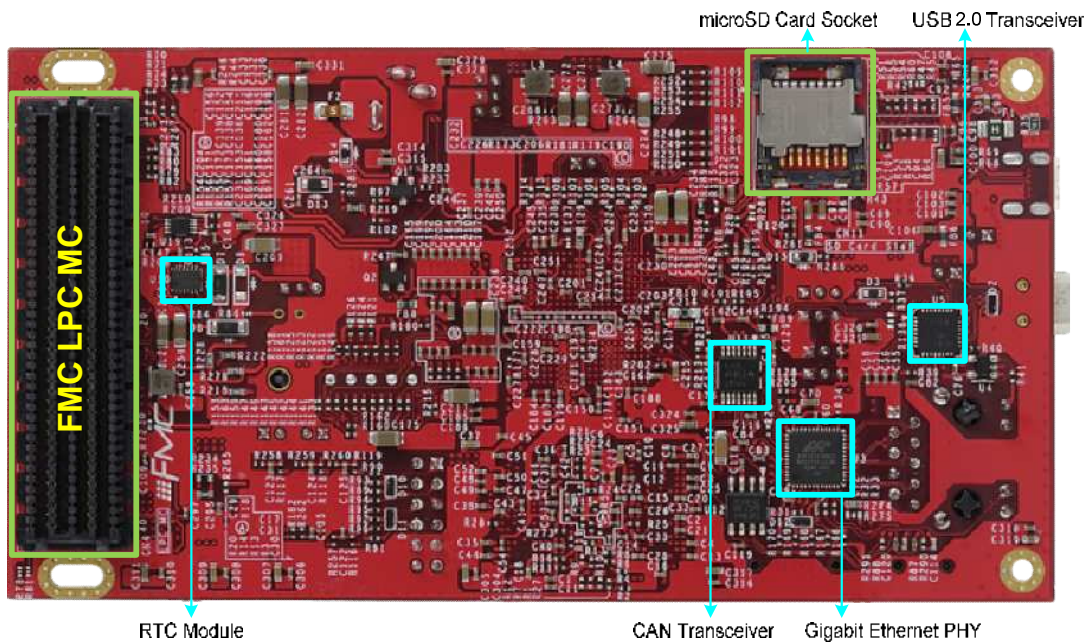


Figure 5-2 Solder Side

## 6. Board Specifications

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The TB-7Z-020-EMC board specifications are showed in Figure 6-1 and Figure 6-2.

External Dimensions:	130 mm (W) x 69 mm (H)
Number of Layers:	12 layers
Board Thickness:	1.6 mm
Material:	FR-4
FMC LPC CC Connector:	Samtec's ASP-134603-01
FMC LPC MC Connector:	Samtec's ASP-134604-01
USB OTG Connector:	Molex's 67803-8020
RJ-45 connector:	HanRun's HR911130C
CAN & RS-232 connector:	one 2.0-pitch Header (2x5)
HDMI/DVI Video connector:	Molex's 046765-1001
Pmod connector:	Samtec's SSW-106-01-F-D
MICTOR Connector:	TE Connectivity's 2-5767004-2
SD Card Slot:	JAE's ST1W008S4ER1500
Xilinx JTAG connector:	Molex's 87832-1420
Power Input connector:	CUI Inc's PJ-006A





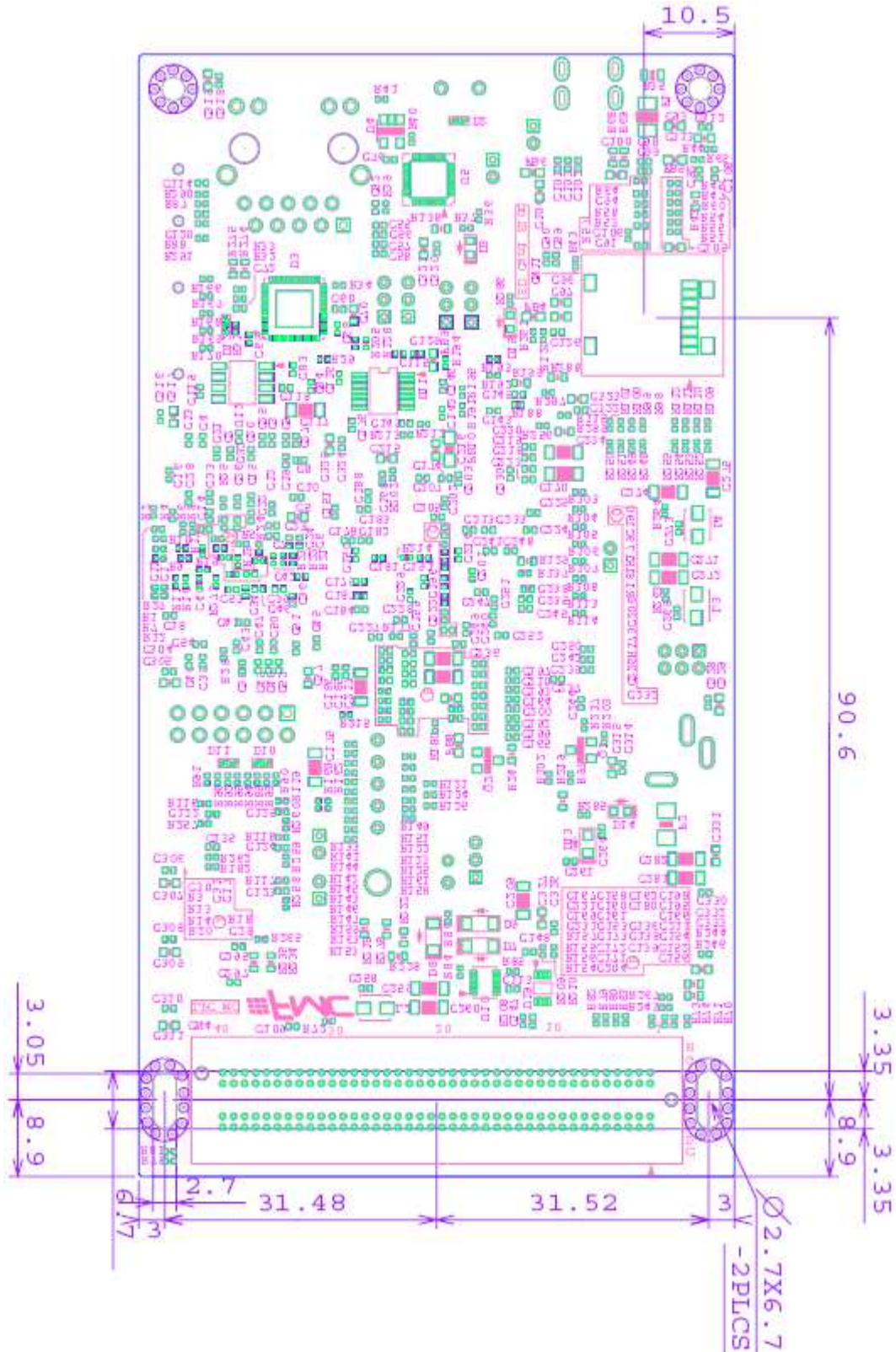
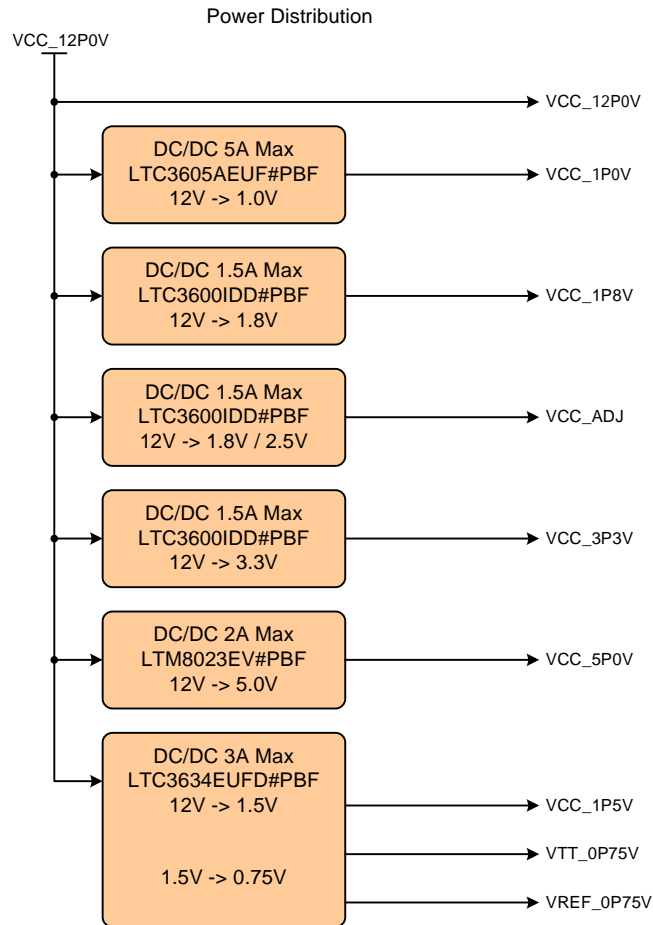


Figure 6-2 Board Dimensions (inclusive of wastable substrate, bottom view)

## 7. Description of Components

### 7.1. Power Supply Structure

TB-7Z-020-EMC board's power supply structure is showed in Figure 7-1.



**Figure 7-1 Power Supply Structure**

#### 7.1.1. DC Jack Connector and Power Switch cable

There is a DC Jack connector for +12V input voltage supply on board.

TB-7Z-020-EMC does not have an on-board power switch. Please always use the power switch cable.



**Figure 7-2 DC Jack Connector and Power Switch Cable**

**Important: Always, TB-7Z-020-EMC needs power from DC Jack connector.**

**When TB-7Z-020-EMC is connected to FPGA evaluation board, it is must be power up first and power down later.**



7.1.2. FP\_VCCO\_ADJ SEL Jumper

Bank 33 and 34 are connecting FMC connector. The bank voltage is depended on connected boards.

TB-7Z-020-EMC has a three selection for bank voltage.

VCC\_3P3V: On-board 3.3V Power supply. Use case is that FMC option board interface is 3.3V.

VCC\_ADJ: On-board 2.5V/1.8V Power supply. Use case is that FMC option board interface is 2.5V/1.8V

Please refer section 7.1.3 VCC\_ADJ SEL Jumper.

FMC\_ADJ: Power supply from main FPGA evaluation board.

There is a 6 pin jumper (J9) for FP\_VCCO\_ADJ(Bank33 and 34) power selection.

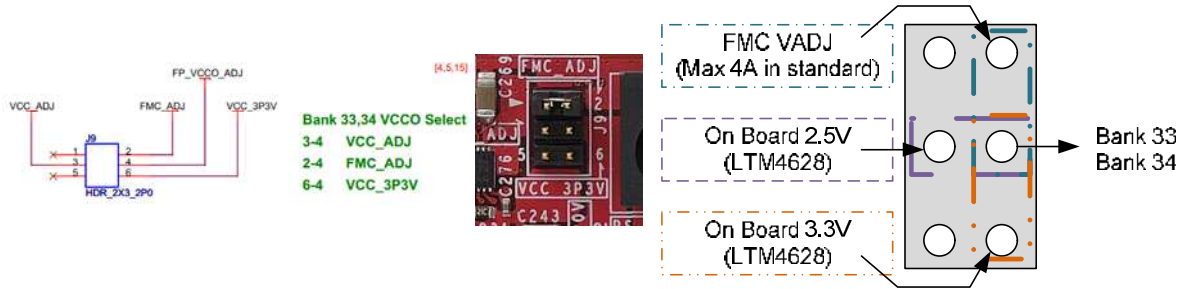


Figure 7-3 FP\_VCCO\_ADJ SEL Jumper

7.1.3. VCC\_ADJ SEL Jumper

TB-7Z-020-EMC has on board power supply of 2.5V/1.8V.

There is a 2 pin jumper (J8) for VCC\_ADJ power selection.



Figure 7-4 VCC\_ADJ SEL Jumper

Table 7-1 Power Setting

Jumper No.	Description	Status	Function
J8	VCC_ADJ select	Short	1.8V
		Open	2.5V
J9	FP_VCCO_ADJ select	2-4	FMC_ADJ
		3-4	VCC_ADJ
		4-6	VCC_3P3V



## 7.2. Clock System

The TB-7Z-020-EMC board's clock system diagram is showed in Figure 7-5.

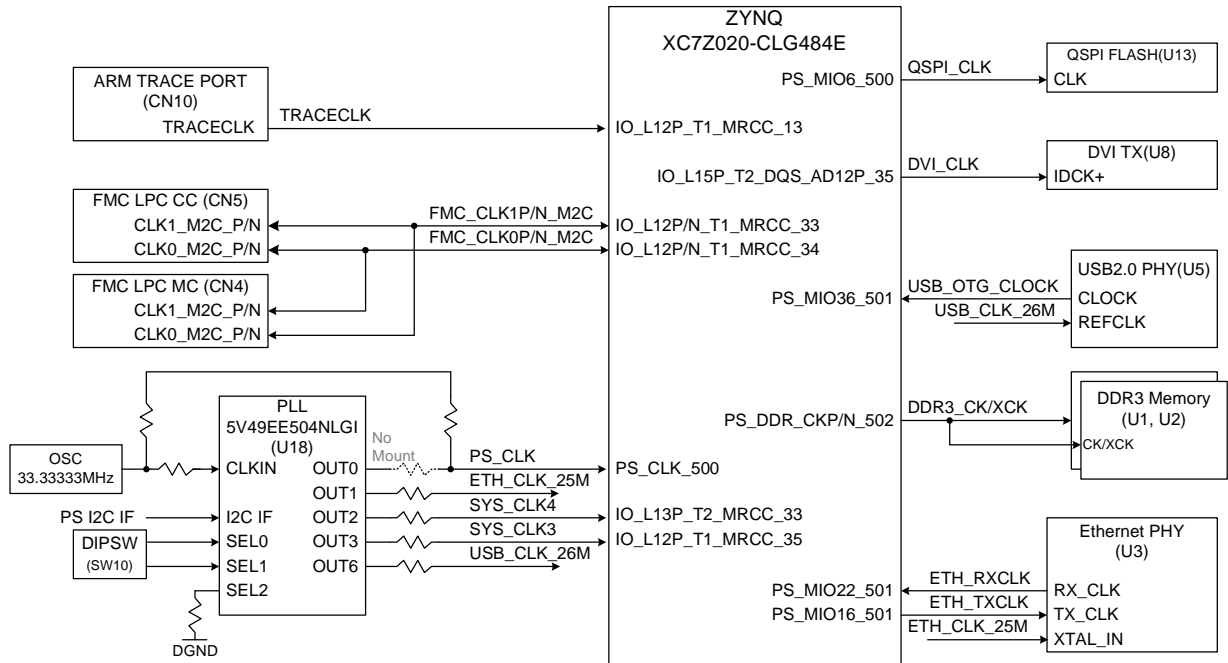


Figure 7-5 Clock System Diagram

Table 7-2 Clock signals pin assign

Zynq Pin#	Zynq Pin Name	Signal Name	Connected component
F7	PS_CLK_500	PS_CLK)	OSC 33.33333MHz
A4	PS_MIO6_500	QSPI_CLK	QSFI FLASH (U13)
D6	PS_MIO16_501	ETH_TXCLK	Ethernet PHY (U3) TX_CLK
A14	PS_MIO22_501	ETH_RXCLK	Ethernet PHY (U3) RX_CLK
A9	PS_MIO36_501	USB_OTG_CLOCK	USB2.0 PHY (U5) Clock
N4	PS_DDR_CKP_502	DDR3_CK	DDR3 (U1, U2) Positive Clock
N5	PS_DDR_CKN_502	DDR3_XCK	DDR3 (U1, U2) Negative Clock
Y9	IO_L12P_T1_MRCC_13	TRACECLK	Mictor 38 (CN10) pin 6
W17	IO_L13P_T2_MRCC_33	SYS_CLK4	PLL (U18) Out 2
D18	IO_L12P_T1_MRCC_35	SYS_CLK3	PLL (U18) Out 3
Y18	IO_L12P_T1_MRCC_33	FMC_CLK1P_M2C	FMC(CN4, CN5) G2
AA18	IO_L12N_T1_MRCC_33	FMC_CLK1N_M2C	FMC(CN4, CN5) G3
L18	IO_L12P_T1_MRCC_34	FMC_CLK0P_M2C	FMC(CN4, CN5) H4
L19	IO_L12N_MRCC_34	FMC_CLK0N_M2C	FMC(CN4, CN5) H5

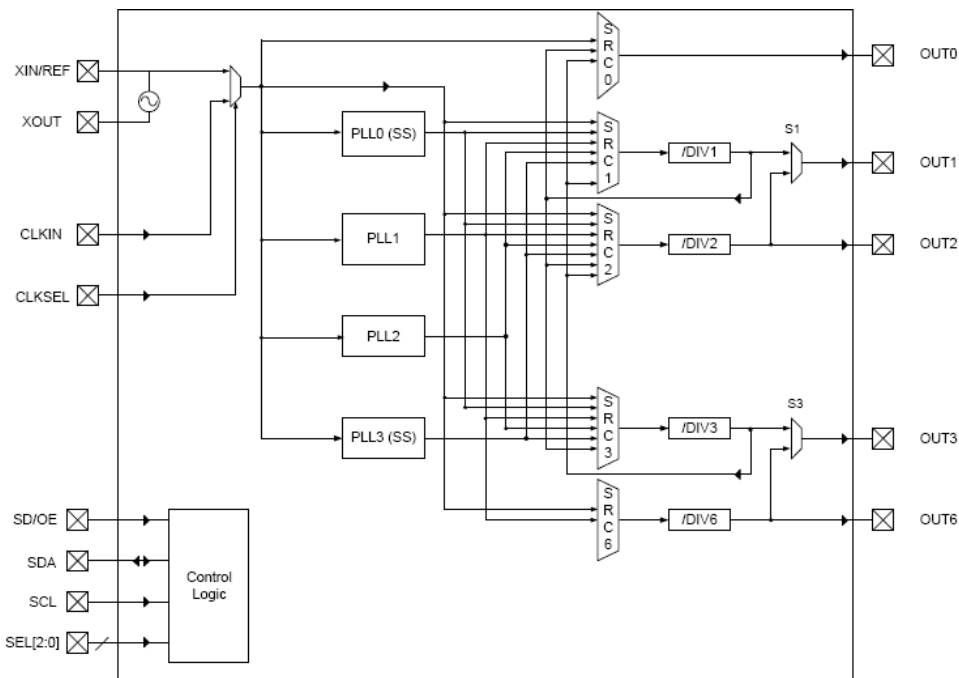
### 7.3. On-board PLL

The TB-7Z-020-EMC has the on-board PLL. Please refer Figure 7-5.

Using IDT VersaClockIII series, 5V49EE504NLGI is an external PLL. It could memory the setting of PLL via I2C interface which connected to PS (Processing System) I2C Bus. Please refer to the reference design of PLL setting and Section 7.4 I2C BUS.

**Table 7-3 External PLL settings**

OUT#	Connect to	Frequency	Note
0	Not connected	(33MHz)	Not Used
1	Ethernet PHY	25MHz	Do not needs to change settings
2	PL Clock	User Define	Default: 148.5MHz(DVI)
3	PL Clock	User Define	Default: 25MHz
6	USB PHY	26MHz	Do not needs to change settings



**Figure 7-6 5V49EE504 EEPROM PROGRAMABLE CLOCK GENERATOR**

Feature of IDT 5V49EE504.

- Four internal PLLs
- Each PLL has a 7-bit reference divider and a 12-bit feedback-divider
- Internal non-volatile EEPROM with I2C.
- Input frequency range: 1 MHz to 200 MHz
- Output frequency range: 4.9 kHz to 200 MHz
- Two independently controlled VDDO (1.8V - 3.3V)
- 8-bit output-divider blocks
- Fractional division capability on one PLL
- Two of the PLLs support spread spectrum generation capability
- Programmable slew rate control
- Programmable loop bandwidth
- Programmable output inversion to reduce bimodal jitter
- Redundant clock inputs with auto and manual switchover options

Configuration software is available from IDT web site.

### 7.4. I2C BUS

The TB-7Z-020-EMC board implements a single I2C port on the Zynq AP SoC PS. The I2C Bus topology is shown in Figure 7-7.

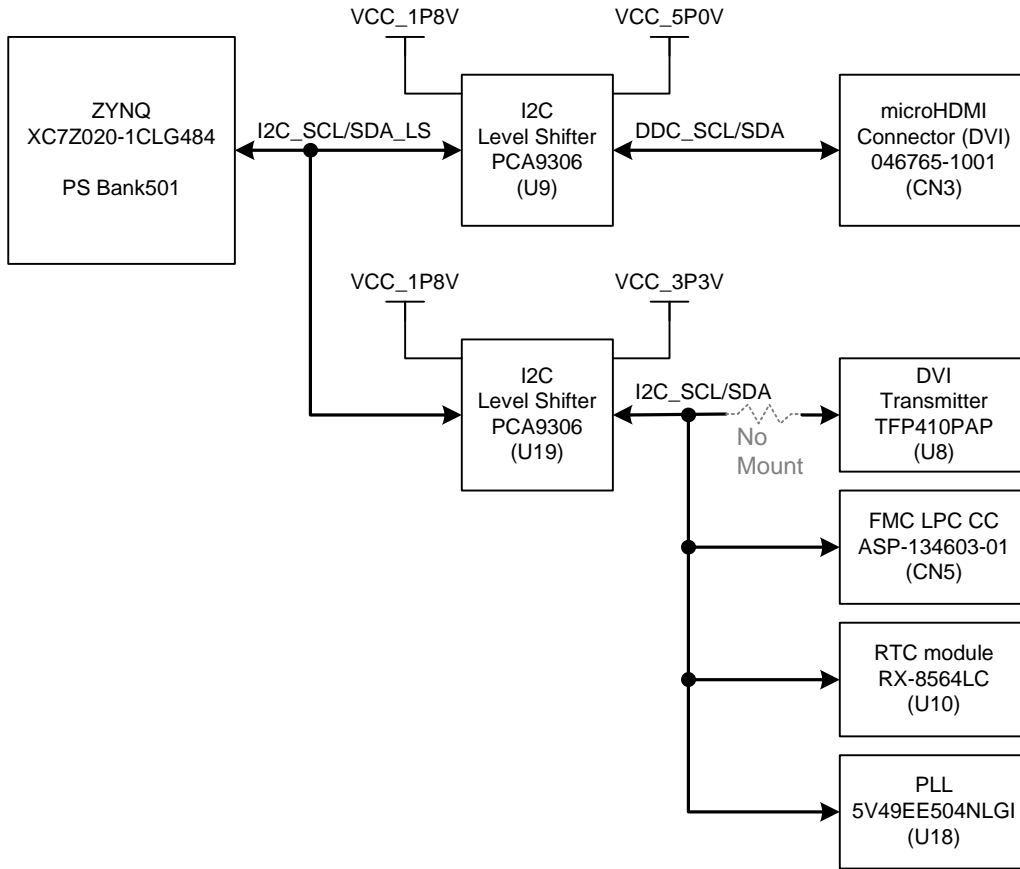


Figure 7-7 I2C Bus Topology

Table 7-4 I2C Address Map

No.	Device	Write Address	Read Address	Note
1	microHDMI Connector	Custom	Custom	Interface is DVI DDC_SCL, DDC_SDA
2	TFP410PAP (DVI PHY)	01110000	01110001	It is not connected. R44 and R45 need to mount 0 ohm register.
3	FMC LPC CC (CN5)	Custom	Custom	It is related FMC mezzanine board. Please refer to section 7.16.2
4	RX-8564LC (RTC)	1010001	1010001	Please refer to section 7.10 and datasheet
5	5V49EE504NLGI (PLL)	1101010	1101010	Please refer to section 7.3 and datasheet

## 7.5. Memory

Zynq AP SoC contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules.

### 7.5.1. DDR3

The board includes two DDR3 SDRAM memory components creating a 32-bit interface. The DDR3 is connected to the hard memory controller in the PS.

The PS incorporates both the DDR controller and the associated PHY, including its own set of dedicated I/Os. The PS DDR3 memory interface speeds up to 533MHz (1066Mbps) are supported.

Device: MT41J256M16RE-15E IT:D (Micron) 32 Meg x 16 x 8 banks (or compatible device)

Device Data Rate: 667MHz (1333Mbps)

The DDR3 interface is shown in Figure 7-8.

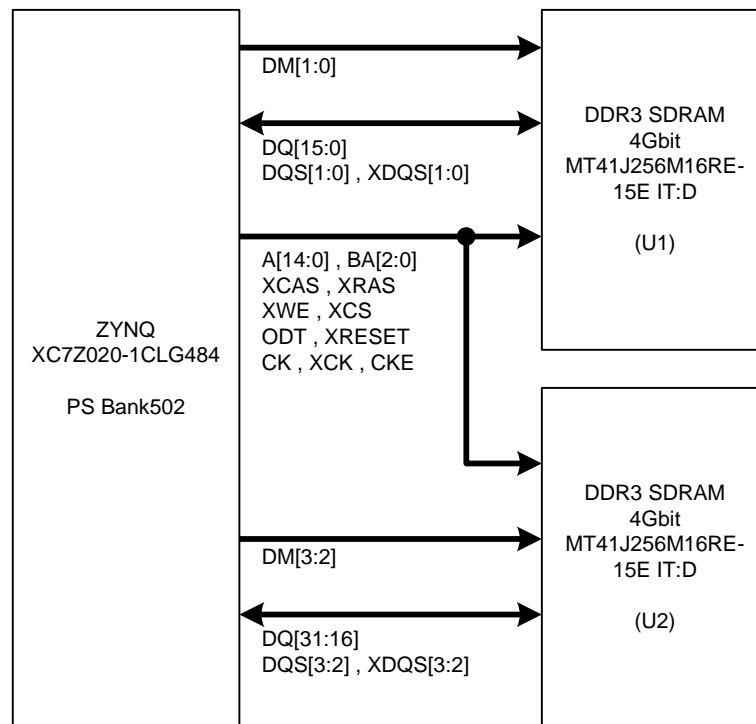


Figure 7-8 DDR3 Memory Connection

### 7.5.2. QSPI Flash

The Board includes a 4-bit QSPI (quad-SPI) 128Mbit NOR flash. The Micron N25Q128A13BSF40F is used on this board. The Multi-I/O SPI Flash memory is used to provide non-volatile code, and data storage. It can be used to initialize the PS as well as configure the PL (bitstream).

Device: N25Q128A13BSF40F (Micron) 128Mbit , x1/x2/x4 support (or compatible device)

Device Data Rate: 108 MHz (maximum) clock frequency

The QSPI interface is shown in Figure 7-9.

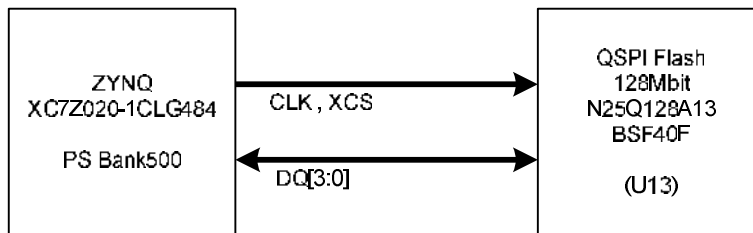


Figure 7-9 QSPI Connection

### 7.5.3. SD Card Interface

The Zynq AP SoC PS SD/SDIO peripheral controls communication with the SD card. The SD card can be used for non-volatile external memory storage as well as booting the Zynq AP SoC.

Device Features: microSD Card Slot ST1W 008S4ER1500 (JAE Electronics)

Media is 4GB uSD card support

The microSD Card interface is shown in Figure 7-10.

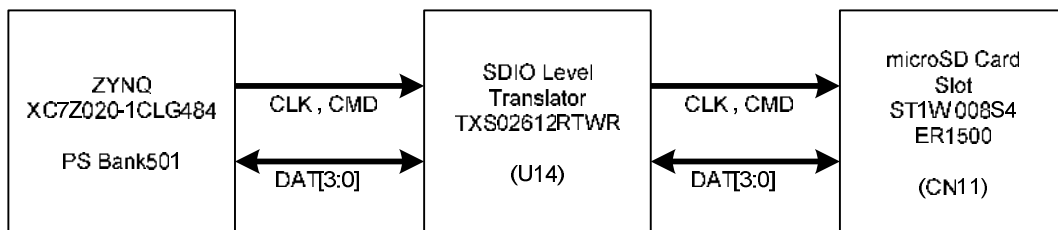


Figure 7-10 SD Card Slot Connection

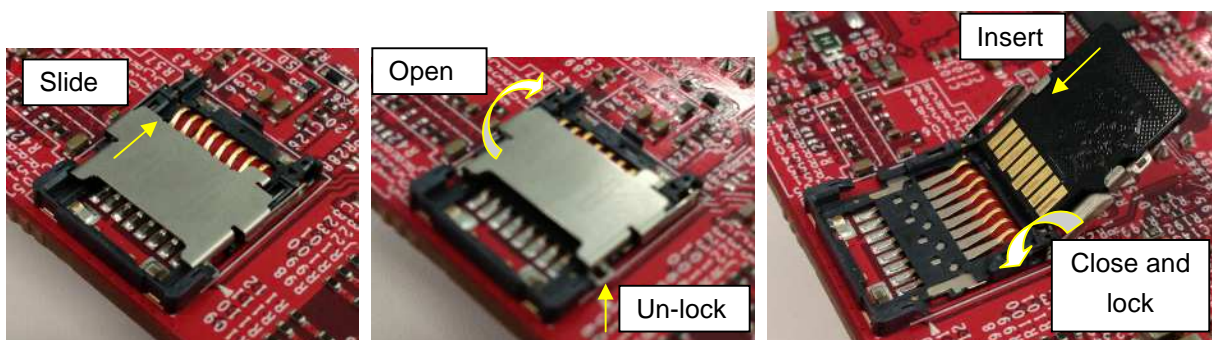


Figure 7-11 micro SD CARD Socket

### 7.6. 10/100/1000 Ethernet PHY

TB-7Z-020-EMC has 10/100/1000 Base Ethernet PHY connected to the PS Ethernet MAC by RGMII. PHY chip is Marvell's 88E1518. The bit[0] of PHY address is 0.

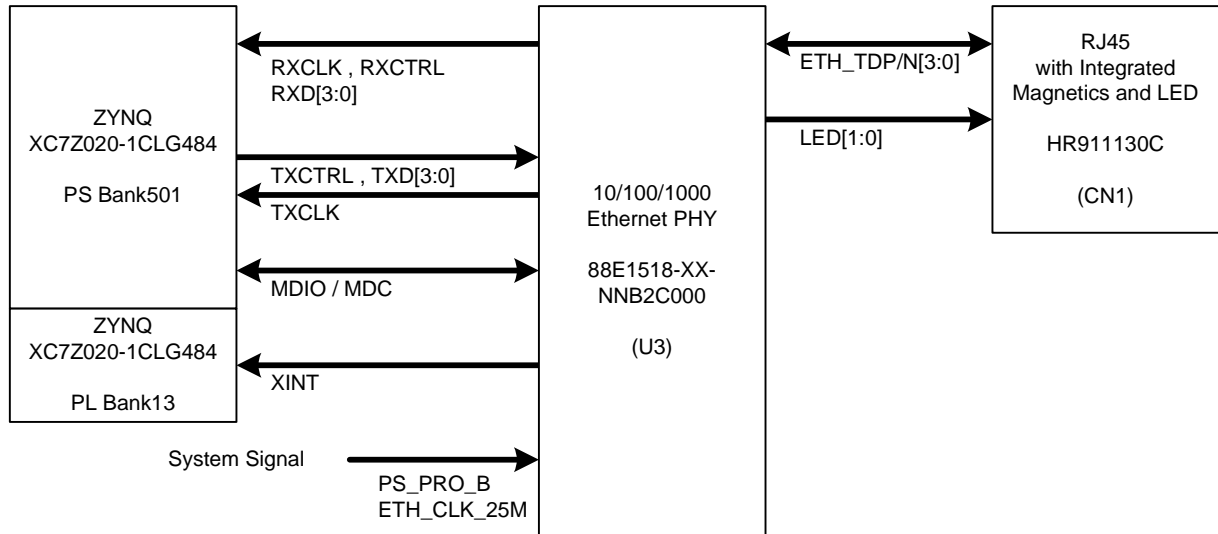


Figure 7-12 RGMII Connection

RJ-45 connector (HanRun's HY911130C) has internal LEDs. To indicate the statuses of Ethernet PHY, LEDs are connected to PHY's signal LED0 and LED1 respectively.

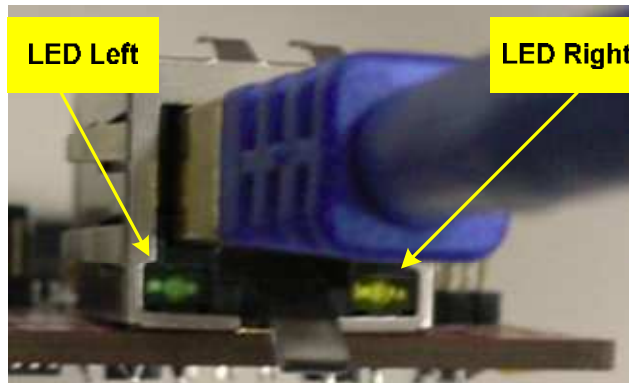


Figure 7-13 RJ-45 internal LED

Table 7-5 RJ-45 internal LED Function Table

LED#	Color	Function	Target IC		
			IC#	Pin#	Pin Name
LED Left	Green	LED for 1000BASE-TX link/speed or link indicator.	U3	10	LED0
LED Right	Yellow	LED for Transmit Activity or RX/TX Activity/Link modes.	U3	9	LED1

### 7.7. UART Interface

The TB-7Z-020-EMC board includes the TI MAX3232CPW RS-232 Line Driver/Receiver.

Device Features : MAX3232CPW (TI)

The UART interface is shown in Figure 7-14.

PinHeader to D-sub 9 pin conversion cable is included in TB-7Z-020-EMC. Please refer to connection in Figure 7-15.

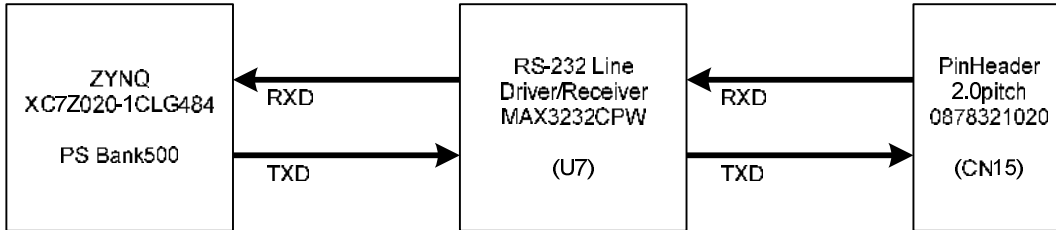


Figure 7-14 UART Connection

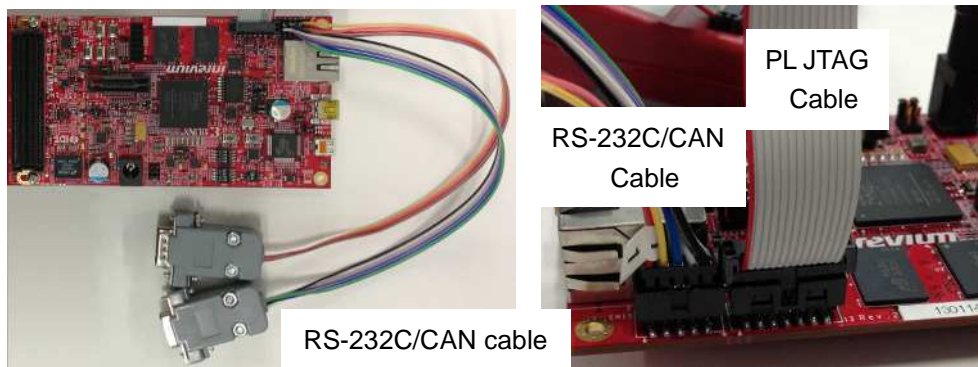


Figure 7-15 RS-232C/CAN Cable connection

#### 7.7.1. RS-232C Cable pin assign

Cable end is Dsub 9pin male connector and header is connecting to CN15.

Table 7-6 RS-232C Cable pin assign

Dsub Pin#	Signal Name	Header Pin#	Zynq Pin#	Dsub Pin#	Signal Name	Header Pin#	Zynq Pin#
1	NC	-	-	6	NC	-	-
2	RXD	2	B6	7	NC	-	-
3	TXD	1	E6	8	NC	-	-
4	NC	-	-	9	NC	-	-
5	GND	3 and 4	-				

### 7.8. CAN BUS

The TB-7Z-020-EMC board includes the PHILIPS TJA1040T\_VM\_118. The TJA1040 is an advanced high speed Controller Area Network (CAN) transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation described in the international standard for in-vehicle high speed CAN applications (ISO 11898).

Device Features : TJA1040T\_VM\_118 (PHILIPS)

The CAN interface is shown in Figure 7-16.

RXD signal connected to Zynq D12. TXD signal connected to Zynq B10.

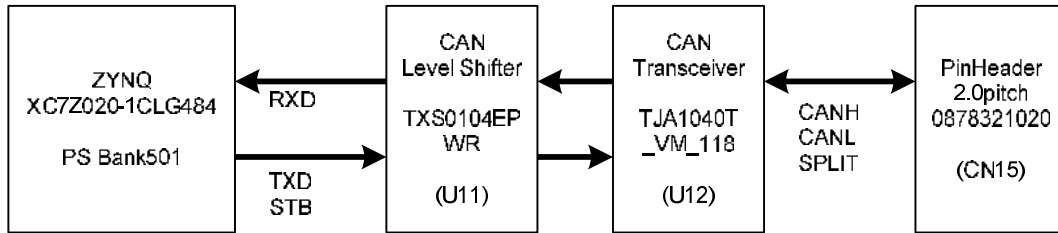


Figure 7-16 CAN Connection

#### 7.8.1. Termination of CAN Bus

TB-7Z-020-EMC has termination registers R290 and R291. To connecting CAN Bus, Please check that registers

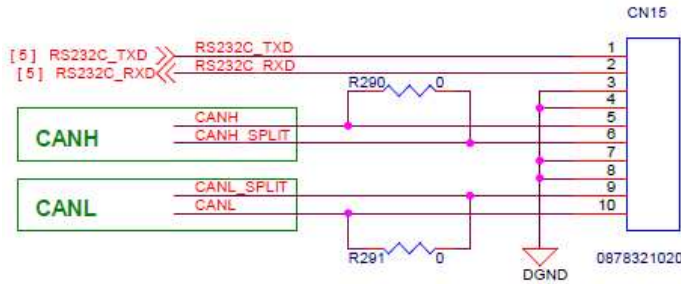


Figure 7-17 CN15 and CAN Termination

#### 7.8.2. CAN Cable pin assign

Cable end is Dsub 9pin female connector and header is connecting to CN15.

Table 7-7 CAN BUS Cable pin assign

Dsub Pin#	Signal Name	Header Pin#	Dsub Pin#	Signal Name	Header Pin#
1	NC	-	6	NC	-
2	CANL	10	7	CANH	5
3	GND	7 and 8	8	NC	-
4	NC	-	9	NC	-
5	NC	-			

CANH\_SPLIT and CANL\_SPLIT signals are not connected.



### 7.9. USB OTG

The TB-7Z-020-EMC board includes the TI TUSB1210 Standalone USB Transceiver Chip. It is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbps.

Device Features : TUSB1210BRHB (TI)

**Caution: TUSB1210BRHB and Zynq-7000 has a timing incompatibility at hot temperature.  
Please use TB-7Z-020-MEC in room temperature.**

The USB interface is shown in Figure 7-18.

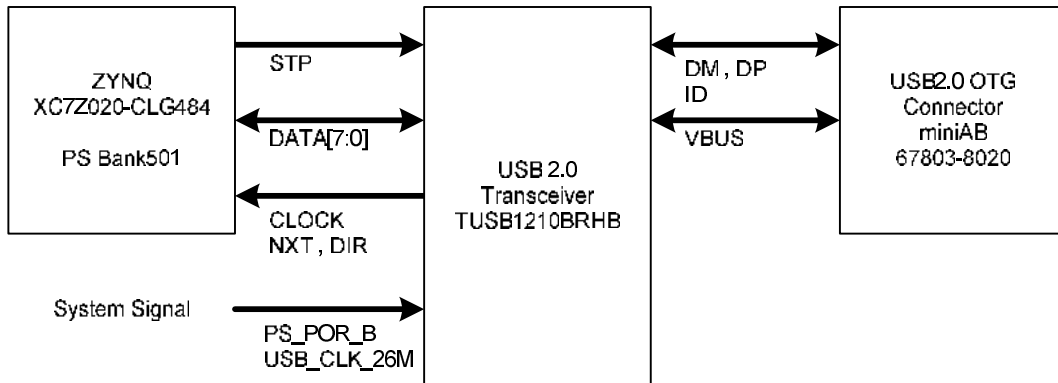


Figure 7-18 USB Connection

#### 7.9.1. USB VBUS Power Supply SEL Jumper

There is a 2 pin jumper (J1) for USB VBUS power Supply selection.

**Caution: Do not connect USB Host(as PC) when J1 is shorted.**

**J1 - VBUS 5V Enable (Default : Disconnect) ; J2 Short to enable 5V output to USB OTG Connector .**

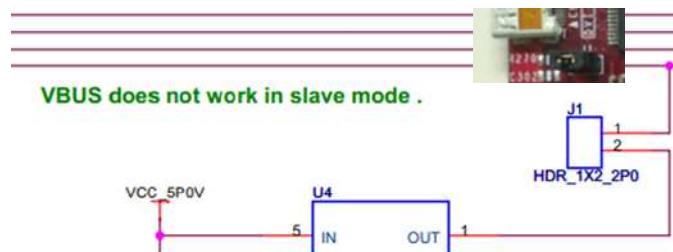


Figure 7-19 USB VBUS Power Supply SEL Jumper

Table 7-8 USB Settings

Jumper #	Description	Status	Function
J1	VBUS 5V Power Supply Enable	Short	Enable 5V output to USB Connector, while USB Transceiver is working in Host Mode.
		Open	Disable 5V output to USB Connector, while USB Transceiver is working in Slave Mode.
J2	USB VBUS Capacitor Setting	Short	For Host Mode (Cvbus > 120uF)
		Open	For Device or OTG modes (Cvbus=2.2uF)

## 7.10. RTC

The TB-7Z-020-EMC board includes the Epson RX-8564LC RS-232. It is an I2C bus interface real-time clock that has a built-in 32.768 KHz oscillator with these features:

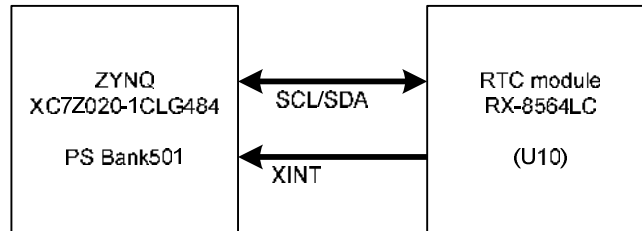
Frequency output options: 32.768 KHz, 1024 Hz, 32 Hz or 1 Hz

Calendar output functions: Year, month, day, weekday, hour, minute and second

Clock counter, alarm and fixed-cycle timer interrupt functions

Device: RX-8564LC

The RTC interface is shown in Figure 7-20.



**Figure 7-20 RTC Connection**

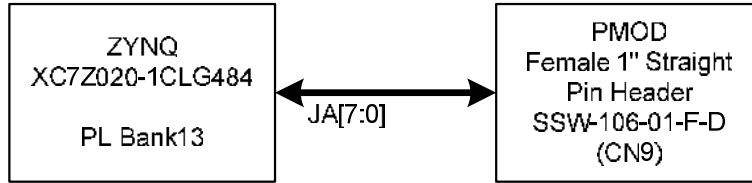
**Table 7-9 RTC I2C Address**

Device	Write Address	Read Address
RX-8564LC	1010001	1010001

**7.11. Pmod**

The TB-7Z-020-EMC board includes the Digilent Pmod compatible headers (2x6). It is straight, 0.1” female headers that include eight user I/O plus 3.3V and ground signals.

The Pmod interface is shown in Figure 7-21.



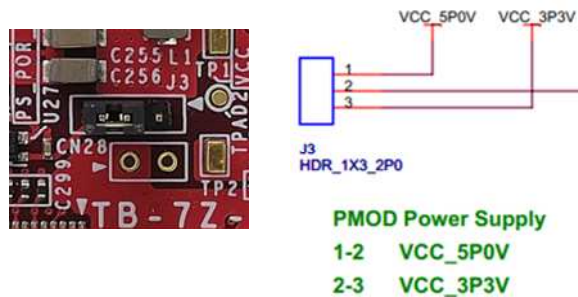
**Figure 7-21 Pmod Connection**

**Table 7-10 Pmod pin assign**

Pmod Pin#	Signal Name	Zynq Pin#	Pmod Pin#	Signal Name	Zynq Pin#
1	JA0	AA7	7	JA4	AB5
2	JA1	AA6	8	JA5	AB4
3	JA2	AB2	9	JA6	AB7
4	JA3	AB1	10	JA7	AB6
5	GND	GND	11	GND	GND
6	VCC	Refer to section 7.11.1	12	VCC	Refer to section 7.11.1

**7.11.1. Pmod Power Supply SEL Jumper**

There is a 3 pin jumper (J3) for Pmod Port’s power selection.



**Figure 7-22 Pmod Port’s Power SEL Jumper**

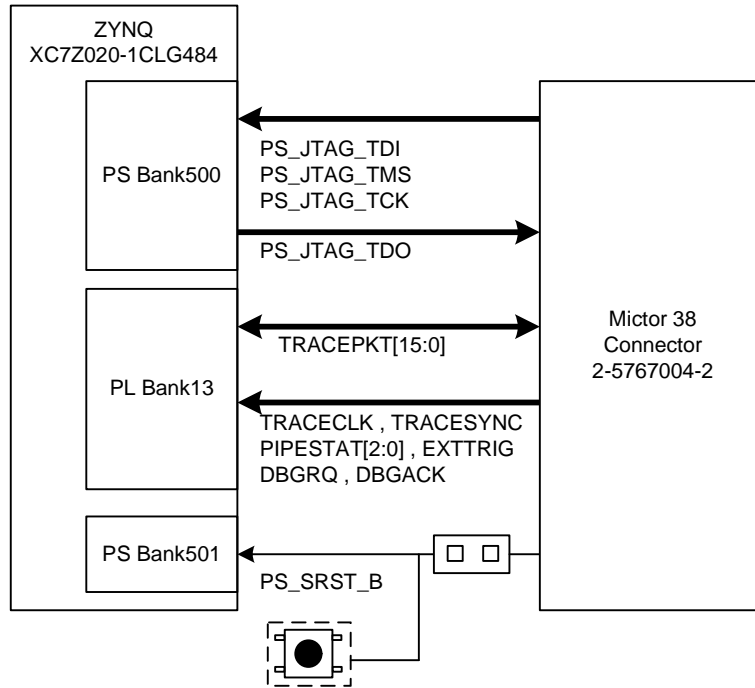
**Table 7-11 Pmod Power Setting**

Jumper No.	Description	Status	Function
J3	Pmod power supply selection	1-2 Short	Use VCC_5P0V power supply
		2-3 Short	Use VCC_3P3V power supply

**7.12. Mictor 38**

The TB-7Z-020-EMC board includes ARM Debugger Interface Connector (Mictor 38). It is intended for high-speed trace capture of up to 16 bits of trace data and status/sync signals. It can also be used to connect to the debug signals of the target.

The Mictor 38 interface is shown in Figure 7-23.



**Figure 7-23 MICTOR 38 Connection**

**Table 7-12 JTAG Mode Setting for Mictor-38**

No.	Boot Device	J7
2	Cascade	2-3

## 7.12.1. VTREF SEL Jumper

There is a 2 pin jumper (J5) for VTREF power supply.

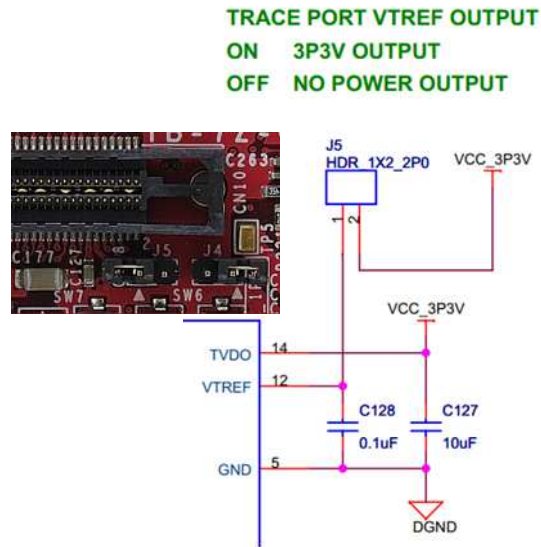


Figure 7-24 ARM PJTAG Port's VTREF SEL Jumper

Table 7-13 Jumper Function Table

Jumper #	Description	Status	Function
J4	ARM Trace Port Soft-reset enable	Short	Enable Soft-reset from ARM Trace Port
		Open	Soft-reset is only generated by SW8
J5	ARM Trace Port VTREF power Supply enable	Short	Enable 3.3V output to ARM Trace Port's VTREF pin.
		Open	Only connect a 0.1uF capacitor to ARM Trace Port's VTREF pin.

Table 7-14 MICTOR 38 pin assignment

Pin#	Pin Name	Connect to (FPGA)	Pin#	Pin Name	Connect to
1	NC	-	2	NC	-
3	NC	-	4	NC	-
5	GND	GND	6	TRACECLK	Y9(U15) via R153
7	DBGRQ	AB12(U15) via R158	8	DBGACK	AA9(U15) via R163
9	XSRST	SW8 via JP4	10	EXTTRIG	AA12(U15) via R159
11	TDO	B4(U15) via R132	12	VTREF	VCC_3P3V via J5
13	RTCK	R125 (Pull-up)	14	TVDO	VCC_3P3V
15	TCK	C5(U15) via R131	16	TRACEPKT7	U4(U15) via R147
17	TMS	A6(U15) via R127	18	TRACEPKT6	T4(U15) via R146
19	TDI	G7(U15) via R130	20	TRACEPKT5	T6(U15) via R145
21	XTRST	R122 (Pull-up)	22	TRACEPKT4	R6(U15) via R143
23	TRACEPKT15	W5(U15) via R152	24	TRACEPKT3	AA4(U15) via R144
25	TRACEPKT14	W6(U15) via R151	26	TRACEPKT2	Y4(U15) via R142
27	TRACEPKT13	W7(U15) via R150	28	TRACEPKT1	AB11(U15) via R133
29	TRACEPKT12	V7(U15) via R149	30	TRACEPKT0	AA11(U15) via R141
31	TRACEPKT11	U5(U15) via R148	32	TRACESYNC	AB10(U15) via R154
33	TRACEPKT10	U6(U15) via R136	34	PIPESTAT2	Y10(U15) via R157
35	TRACEPKT9	V4(U15) via R135	36	PIPESTAT1	Y11(U15) via R155
37	TRACEPKT8	V5(U15) via R134	38	PIPESTAT0	AB9(U15) via R156
39	GND	GND	40	GND	GND
41	GND	GND	42	GND	GND
43	GND	GND	44		

\*U15: ZYNQ ZC7020 device

### 7.13. Reset Switch

PS SRST is system reset switch. This reset signals shared with JTAG-ICE by J4.

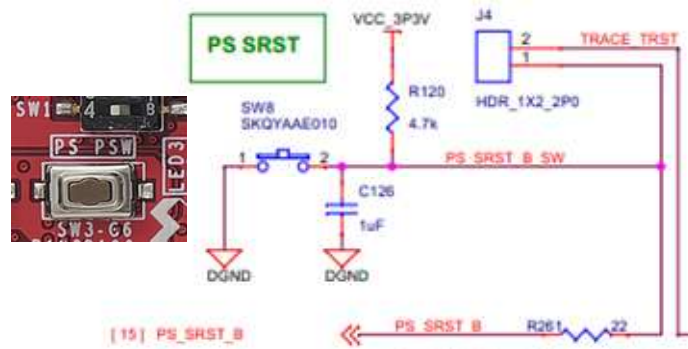


Figure 7-25 XC7Z020's System Reset Push Switch

### 7.14. JTAG

The TB-7Z-020-EMC board provides a traditional Platform Cable JTAG connector.

The JTAG Chain is constructed as follows:

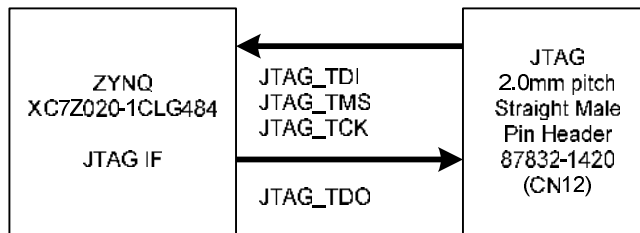


Figure 7-26 JTAG Connection

Table 7-15 JTAG(CN12) Pin assign

CN12 Pin#	Signal Name	Connect to	CN12 Pin#	Signal Name	Zynq Pin#
1	GND	GND	2	3P3V	VCC_3P3V via 100Ohm(R166)
3	GND	GND	4	TMS	G12(Pull-up by 4.7kOhm)
4	GND	GND	6	TCK	G11(Pull-up by 4.7kOhm)
7	GND	GND	8	TDO	G14(Pull-up by 4.7kOhm)
9	GND	GND	10	TDI	H13(Pull-up by 4.7kOhm)
11	GND	GND	12	NC	
13	GND	GND	14	NC	

### 7.15. DVI Output

The TB-7Z-020-EMC board includes the TI TFP410PAP DVI Transmitter. It provides a digital video interface to the TB-7Z-020-EMC board. This 165MHz transmitter is DVI 1.0-compatible supporting 1080p and WUXGA at 60Hz. DDC signals are not connected.

Device Features : TFP410PAP (TI) (Pin Compatible with Sil164 DVI Transmitter)

The DVI interface is shown in Figure 7-27.

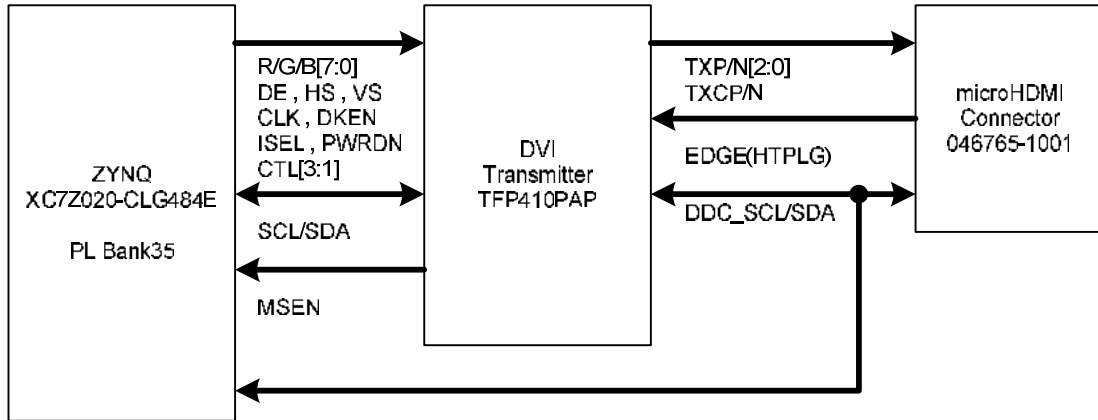


Figure 7-27 DVI Connection

Table 7-16 DVI TX pin assign

DVI (U8) Pin#	Signal Name	Zynq Pin#	DVI (U8) Pin#	Signal Name	Zynq Pin#	DVI (U8) Pin#	Signal Name	Zynq Pin#
63	DVI_B0	F16	53	DVI_G0	F18	43	DVI_R0	A16
62	DVI_B1	E16	52	DVI_G1	E18	42	DVI_R1	A17
61	DVI_B2	D16	51	DVI_G2	G17	41	DVI_R2	A18
60	DVI_B3	D17	50	DVI_G3	F17	40	DVI_R3	A19
59	DVI_B4	E15	47	DVI_G4	C15	39	DVI_R4	C17
58	DVI_B5	D15	46	DVI_G5	B15	38	DVI_R5	C18
55	DVI_B6	G15	45	DVI_G6	B16	37	DVI_R6	C19
54	DVI_B7	G16	44	DVI_G7	B17	36	DVI_R7	B19
2	DVI_DE	B20	14	DVI_R_DSEL	*1	8	DVI_CTL1	C22
5	DVI_VS	D20	15	DVI_E_BSEL	*1	7	DVI_CTL2	E21
4	DVI_HS	C20	35	DVI_DKEN	A22	6	DVI_CTL3	D21
57	DVI_CLK	A21	13	DVI_ISEL	D22	11	DVI_MSEN	B21
						10	DVI_PWRDN	B22

\*1: These signals need to mount 00hm on R45 and R44 pad for connecting Zynq I2C Controller.

Please refer to section 7.4



### 7.16. FMC Connector Interface

The board provides Samtec’s FMC Low-Pin Count Mezzanine Card (CN4) connector and Carrier Card (CN5). The VITA-57 Low-Pin Count pin list is showed in Figure 7-28 respectively.

Notice: Not all pins of LPC are connected to the Zynq-7000.

**Cation: FMC connetors are only exclusice use**

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSENT_M2C	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	G8TCLK0_M5C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	G8TCLK0_M5C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3V_AUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P1V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P1V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VAD2	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VAD2	GND	NC	NC	3P3V	GND	NC	NC

Figure 7-28 FMC LPC Pin List

## 7.16.1. FMC Low-Pin Count Mezzanine Card (CN4) connector.

Table 7-17 FMC LPC MC Connector pin assignment table (CN4)

Zynq Pin#	Signal Name	C		D	Signal Name	Zynq Pin#
	GND	GND	1	PG_C2M	-	
	-	DP0_C2M_P	2	GND	GND	
	-	DP0_C2M_N	3	GND	GND	
	GND	GND	4	GBTCLK0_M2C_P	-	
	GND	GND	5	GBTCLK0_M2C_N	-	
	-	DP0_M2C_P	6	GND	GND	
	-	DP0_M2C_N	7	GND	GND	
	GND	GND	8	LA01_P_CC	FMC_LAP29	V13
	GND	GND	9	LA01_N_CC	FMC_LAN29	W13
J16	FMC_LAP28	LA06_P	10	GND	GND	
J17	FMC_LAN28	LA06_N	11	LA05_P	FMC_LAP24	T16
	GND	GND	12	LA05_N	FMC_LAN24	T17
	GND	GND	13	GND	GND	
P20	FMC_LAP21	LA10_P	14	LA09_P	FMC_LAP25	U17
P21	FMC_LAN21	LA10_N	15	LA09_N	FMC_LAN25	V17
	GND	GND	16	GND	GND	
	GND	GND	17	LA13_P	FMC_LAP20	AB19
N22	FMC_LAP15	LA14_P	18	LA13_N	FMC_LAN20	AB20
P22	FMC_LAN15	LA14_N	19	GND	GND	
	GND	GND	20	LA17_P_CC	FMC_LAP17_CC	N19
	GND	GND	21	LA17_N_CC	FMC_LAN17_CC	N20
J21	FMC_LAP11	LA18_P_CC	22	GND	GND	
J22	FMC_LAN11	LA18_N_CC	23	LA23_P	FMC_LAP12	AA21
	GND	GND	24	LA23_N	FMC_LAN12	AB21
	GND	GND	25	GND	GND	
L21	FMC_LAP07	LA27_P	26	LA26_P	FMC_LAP08	AA22
L22	FMC_LAN07	LA27_N	27	LA26_N	FMC_LAN08	AB22
	GND	GND	28	GND	GND	
	GND	GND	29	TCK	-	
	-	SCL	30	TDI	-	
	-	SDA	31	TDO	-	
	GND	GND	32	*1 3P3VAUX	-	
	GND	GND	33	TMS	-	
	-	GA0	34	TRST_L	-	
	-	12P0V	35	GA1	-	
	GND	GND	36	3P3V	-	
	-	12P0V	37	GND	GND	
	GND	GND	38	3P3V	-	
	-	3P3V	39	GND	GND	
	GND	GND	40	3P3V	-	

Zynq Pin#	Signal Name	G		H	Signal Name	Zynq Pin#
	GND	GND	1	VREF_A_M2C	TPAD1	
Y18	FMC_CLK1P_M2C	CLK1_M2C_P	2	PRSNT_M2C_L	-	
AA18	FMC_CLK1N_M2C	CLK1_M2C_N	3	GND	GND	
	GND	GND	4	CLK0_M2C_P	FMC_CLK0P_M2C	L18
	GND	GND	5	CLK0_M2C_N	FMC_CLK0N_M2C	L19
Y14	FMC_LAP33	LA00_P_CC	6	GND	GND	
AA14	FMC_LAN33	LA00_N_CC	7	LA02_P	FMC_LAP32	N17
	GND	GND	8	LA02_N	FMC_LAN32	N18
W15	FMC_LAP31	LA03_P	9	GND	GND	
Y15	FMC_LAN31	LA03_N	10	LA04_P	FMC_LAP30	L17
	GND	GND	11	LA04_N	FMC_LAN30	M17
J15	FMC_LAP26	LA08_P	12	GND	GND	
K15	FMC_LAN26	LA08_N	13	LA07_P	FMC_LAP27	T21
	GND	GND	14	LA07_N	FMC_LAN27	U21
P17	FMC_LAP23	LA12_P	15	GND	GND	
P18	FMC_LAN23	LA12_N	16	LA11_P	FMC_LAP22	U15
	GND	GND	17	LA11_N	FMC_LAN22	U16
Y20	FMC_LAP16	LA16_P	18	GND	GND	
Y21	FMC_LAN16	LA16_N	19	LA15_P	FMC_LAP19	R20
	GND	GND	20	LA15_N	FMC_LAN19	R21
M21	FMC_LAP13	LA20_P	21	GND	GND	
M22	FMC_LAN13	LA20_N	22	LA19_P	FMC_LAP18_CC	W16
	GND	GND	23	LA19_N	FMC_LAN18_CC	Y16
Y13	FMC_LAP09	LA22_P	24	GND	GND	
AA13	FMC_LAN09	LA22_N	25	LA21_P	FMC_LAP14	W20
	GND	GND	26	LA21_N	FMC_LAN14	W21
J18	FMC_LAP05	LA25_P	27	GND	GND	
K18	FMC_LAN05	LA25_N	28	LA24_P	FMC_LAP10	V22
	GND	GND	29	LA24_N	FMC_LAN10	W22
M19	FMC_LAP01_CC	LA29_P	30	GND	GND	
M20	FMC_LAN01_CC	LA29_N	31	LA28_P	FMC_LAP06	T22
	GND	GND	32	LA28_N	FMC_LAN06	U22
U20	FMC_LAP03	LA31_P	33	GND	GND	
V20	FMC_LAN03	LA31_N	34	LA30_P	FMC_LAP04	K19
	GND	GND	35	LA30_N	FMC_LAN04	K20
Y19	FMC_LAP00_CC	LA33_P	36	GND	GND	
AA19	FMC_LAN00_CC	LA33_N	37	LA32_P	FMC_LAP02	J20
	GND	GND	38	LA32_N	FMC_LAN02	K21
-	FMC_ADJ	VADJ	39	GND	GND	
	GND	GND	40	VADJ	FMC_ADJ	-

## 7.16.2. FMC Low-Pin Count Carrier Card (CN5) connector.

**Table 7-18 FMC LPC CC Connector pin assignment table (CN5)**

Zynq Pin#	Connection	C		D	Connection	Zynq Pin#
	GND	GND	1	PG_C2M	-	
	-	DP0_C2M_P	2	GND	GND	
	-	DP0_C2M_N	3	GND	GND	
	GND	GND	4	GBTCLK0_M2C_P	-	
	GND	GND	5	GBTCLK0_M2C_N	-	
	-	DP0_M2C_P	6	GND	GND	
	-	DP0_M2C_N	7	GND	GND	
	GND	GND	8	LA01_P_CC	FMC_LAP01_CC	M19
	GND	GND	9	LA01_N_CC	FMC_LAN01_CC	M20
T22	FMC_LAP06	LA06_P	10	GND	GND	
U22	FMC_LAN06	LA06_N	11	LA05_P	FMC_LAP05	J18
	GND	GND	12	LA05_N	FMC_LAN05	K18
	GND	GND	13	GND	GND	
V22	FMC_LAP10	LA10_P	14	LA09_P	FMC_LAP09	Y13
W22	FMC_LAN10	LA10_N	15	LA09_N	FMC_LAN09	AA13
	GND	GND	16	GND	GND	
	GND	GND	17	LA13_P	FMC_LAP13	M21
W20	FMC_LAP14	LA14_P	18	LA13_N	FMC_LAN13	M22
W21	FMC_LAN14	LA14_N	19	GND	GND	
	GND	GND	20	LA17_P_CC	FMC_LAP17_CC	N19
	GND	GND	21	LA17_N_CC	FMC_LAN17_CC	N20
W16	FMC_LAP18_CC	LA18_P_CC	22	GND	GND	
Y16	FMC_LAN18_CC	LA18_N_CC	23	LA23_P	FMC_LAP23	P17
	GND	GND	24	LA23_N	FMC_LAN23	P18
	GND	GND	25	GND	GND	
T21	FMC_LAP27	LA27_P	26	LA26_P	FMC_LAP26	J15
U21	FMC_LAN27	LA27_N	27	LA26_N	FMC_LAN26	K15
	GND	GND	28	GND	GND	
	GND	GND	29	TCK	-	
D13	FMC_SCL	SCL	30	TDI	-	
C10	FMC_SDA	SDA	31	TDO	-	
	GND	GND	32	*1 3P3VAUX	-	
	GND	GND	33	TMS	-	
-	FMC_I2C_A0	GA0	34	TRST_L	-	
-	VCC_12P0V	12P0V	35	GA1	FMC_I2C_A1	-
	GND	GND	36	3P3V	VCC_3P3V	-
-	VCC_12P0V	12P0V	37	GND	GND	
	GND	GND	38	3P3V	VCC_3P3V	-
-	VCC_3P3V	3P3V	39	GND	GND	
	GND	GND	40	3P3V	VCC_3P3V	-

Zynq Pin#	Connection	G		H	Connection	Zynq Pin#
	GND	GND	1	VREF_A_M2C	FMC_VREF	
Y18	FMC_CLK1P_M2C	CLK1_M2C_P	2	PRSNT_M2C_L	-	
AA18	FMC_CLK1N_M2C	CLK1_M2C_N	3	GND	GND	
	GND	GND	4	CLK0_M2C_P	FMC_CLK0P_M2C	L18
	GND	GND	5	CLK0_M2C_N	FMC_CLK0N_M2C	L19
Y19	FMC_LAP00_CC	LA00_P_CC	6	GND	GND	
AA19	FMC_LAN00_CC	LA00_N_CC	7	LA02_P	FMC_LAP02	J20
	GND	GND	8	LA02_N	FMC_LAN02	K21
U20	FMC_LAP03	LA03_P	9	GND	GND	
V20	FMC_LAN03	LA03_N	10	LA04_P	FMC_LAP04	K19
	GND	GND	11	LA04_N	FMC_LAN04	K20
AA22	FMC_LAP08	LA08_P	12	GND	GND	
AB22	FMC_LAN08	LA08_N	13	LA07_P	FMC_LAP07	L21
	GND	GND	14	LA07_N	FMC_LAN07	L22
AA21	FMC_LAP12	LA12_P	15	GND	GND	
AB21	FMC_LAN12	LA12_N	16	LA11_P	FMC_LAP11	J21
	GND	GND	17	LA11_N	FMC_LAN11	J22
Y20	FMC_LAP16	LA16_P	18	GND	GND	
Y21	FMC_LAN16	LA16_N	19	LA15_P	FMC_LAP15	N22
	GND	GND	20	LA15_N	FMC_LAN15	P22
AB19	FMC_LAP20	LA20_P	21	GND	GND	
AB20	FMC_LAN20	LA20_N	22	LA19_P	FMC_LAP19	R20
	GND	GND	23	LA19_N	FMC_LAN19	R21
U15	FMC_LAP22	LA22_P	24	GND	GND	
U16	FMC_LAN22	LA22_N	25	LA21_P	FMC_LAP21	P20
	GND	GND	26	LA21_N	FMC_LAN21	P21
U17	FMC_LAP25	LA25_P	27	GND	GND	
V17	FMC_LAN25	LA25_N	28	LA24_P	FMC_LAP24	T16
	GND	GND	29	LA24_N	FMC_LAN24	T17
V13	FMC_LAP29	LA29_P	30	GND	GND	
W13	FMC_LAN29	LA29_N	31	LA28_P	FMC_LAP28	J16
	GND	GND	32	LA28_N	FMC_LAN28	J17
W15	FMC_LAP31	LA31_P	33	GND	GND	
Y15	FMC_LAN31	LA31_N	34	LA30_P	FMC_LAP30	L17
	GND	GND	35	LA30_N	FMC_LAN30	M17
Y14	FMC_LAP33	LA33_P	36	GND	GND	
AA14	FMC_LAN33	LA33_N	37	LA32_P	FMC_LAP32	N17
	GND	GND	38	LA32_N	FMC_LAN32	N18
-	FMC_VCCO_ADJ	VADJ	39	GND	GND	
	GND	GND	40	VADJ	FMC_VCCO_ADJ	-

## 7.17. Jumper

The function description of Jumper is in the following table.

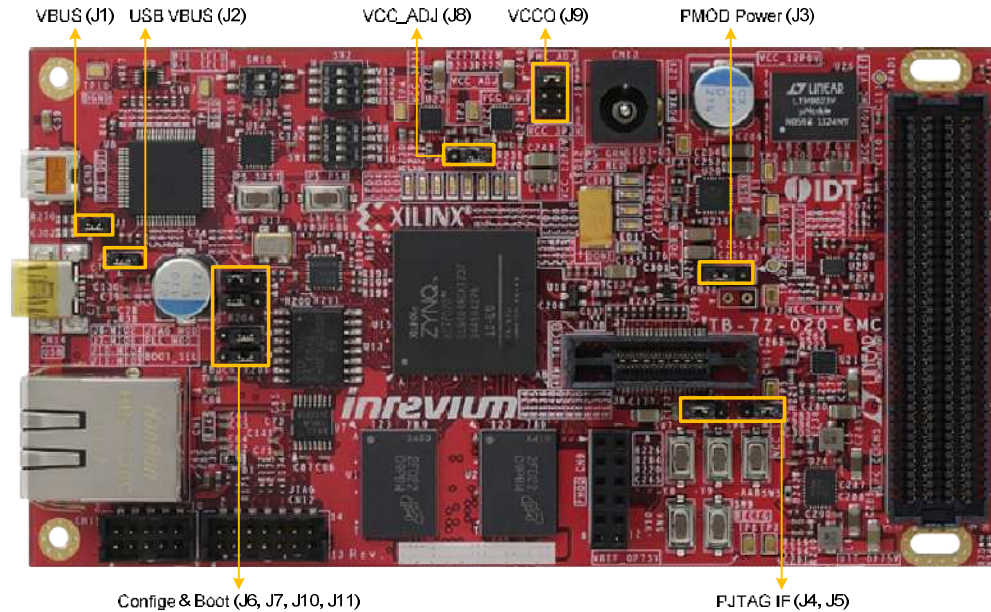


Figure 7-29 Jumpers Position

Table 7-19 All Jumpers Function Table

Jumper#	Description	Status	Function
J1	USB VBUS 5V Power Supply Enable	Short	Enable 5V output.(Host Mode)
		Open	Disable 5V output(Slave Mode)
J2	USB VBUS Capacitor Setting	Short	For Host Mode (Cvbus > 129uF)
		Open	For Device or OTG modes (Cvbus=4.7uF)
J3	Pmod power supply selection	1-2 Short	Use VCC_5P0V power supply
		2-3 Short	Use VCC_3P3V power supply
J4	ARM Trace Port Soft-reset enable	Short	Enable Soft-reset from ARM Trace Port
		Open	Soft-reset is only generated by SW8
J5	ARM Trace Port VTREF power Supply enable	Short	Enable 3.3V output to VTREF pin.
		Open	Connect a 0.1uF capacitor to VTREF pin.
J6	Boot_Mode[3] / MIO[2]	1-2	VCC makes JTAG chains independent.
		2-3	GND cascades PS and PL JTAG chains.
J7	Boot_Mode[4] / MIO[6]	1-2	VCC bypasses internal PS PLLs.
		2-3	GND uses PS PLLs.
J8	VCC_ADJ select	Short	1.8V
		Open	2.5V
J9	FP_VCCO_ADJ select	2-4	FMC_ADJ
		3-4	VCC_ADJ
		6-4	VCC_3P3V
J10	Boot_Mode[1] / MIO[4]	1-2	Boot Device : SD Mode
		3-2	Boot Device : Quad-SPI / JTAG Mode
J11	Boot_Mode[2] / MIO[5]	1-2	Boot Mode : SD / Quad-SPI Mode
		3-2	Boot Mode : JTAG Mode



## 7.17.1. Boot Mode Settings

**Table 7-20 Boot Mode Settings**

No.	Boot Device	J10	J11	J7
1	JTAG	2-3	2-3	2-3
2	SD Card	1-2	1-2	2-3
3	QSPI	2-3	1-2	2-3

Note: Usually, J6 is fixed setting.

## 7.17.2. JTAG Mode Setting

Debugging ARM software via Mictor-38 connector, J6 should be Cascade Mode (2-3).

**Table 7-21 JTAG Mode Setting**

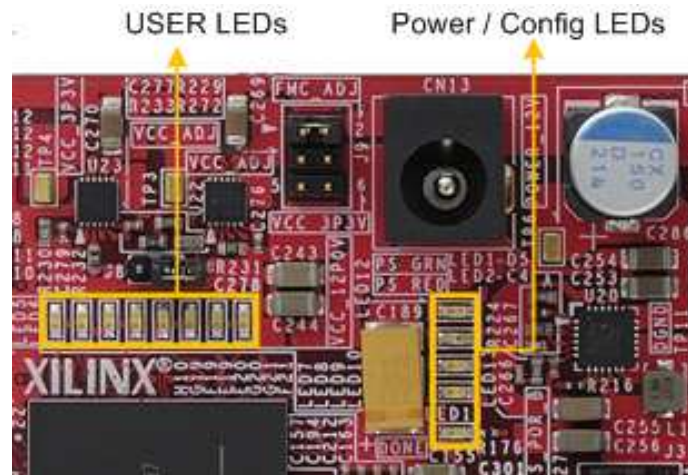
No.	Boot Device	J6
1	Independent	1-2
2	Cascade	2-3

### 7.18. LED

There are 13 LEDs on the board. Some of These LEDs are used to indicate the statuses of XC7Z020, while the others provide user and general purpose I/O capabilities. The function description of LEDs is in the following table.

**Table 7-22 LED Function Table**

LED#	Color	Function	Target IC		
			IC#	Pin#	Pin Name
LED1	Green	PS User LED. High Active(On)	U15	D5	PS_LED_GRN
LED2	Red	PS User LED. Low Active(On)	U15	C4	PS_LED_RED
LED3	Green	PL User LED. Low Active(On)	U15	H20	FP_LED0
LED4	Green	PL User LED. Low Active(On)	U15	G19	FP_LED1
LED5	Green	PL User LED. Low Active(On)	U15	F19	FP_LED2
LED6	Green	PL User LED. Low Active(On)	U15	E19	FP_LED3
LED7	Green	PL User LED. Low Active(On)	U15	E20	FP_LED4
LED8	Green	PL User LED. Low Active(On)	U15	G20	FP_LED5
LED9	Green	PL User LED. Low Active(On)	U15	G21	FP_LED6
LED10	Green	PL User LED. Low Active(On)	U15	F21	FP_LED7
LED11	Green	PL configuration is Done.	U15	T12	DONE
LED12	Green	VCC_12P0V Power ON	TP6	-	VCC_12P0V
LED13	Green	External power-on reset is released.	U15	B5	PS_POR_B



**Figure 7-30 LED Position**

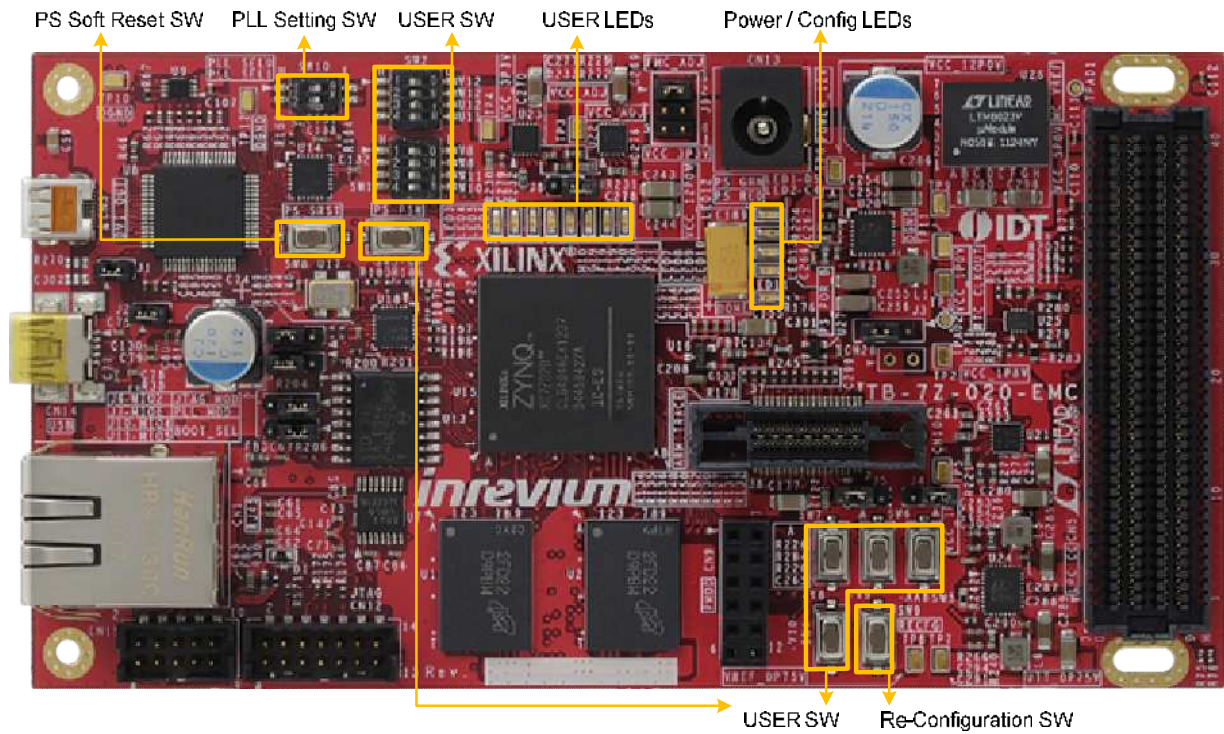


### 7.19. Push Switch

There are 3 switches on the board. The following table shows the details of the Push switches.

**Table 7-23 Push Switch Function Table**

Switch#	Description	Target IC		
		IC#	Pin#	Net Name
SW3	PS User Push Switch. Active High(Push)	U15	G6	PS_PUSHSW
SW4	PL User Push Switch. Active Low(Push)	U15	V10	FP_PUSHSW0
SW5	PL User Push Switch. Active Low(Push)	U15	AA8	FP_PUSHSW1
SW6	PL User Push Switch. Active Low(Push)	U15	V9	FP_PUSHSW2
SW7	PL User Push Switch. Active Low(Push)	U15	Y8	FP_PUSHSW3
SW8	Toggles XC7Z020's PS_SRST_B	U15	C9	PS_SRST_B
SW9	Toggles XC7Z020's PROG_B	U15	T11	PROG_B Only erase PL Design



**Figure 7-31 Push Switches**

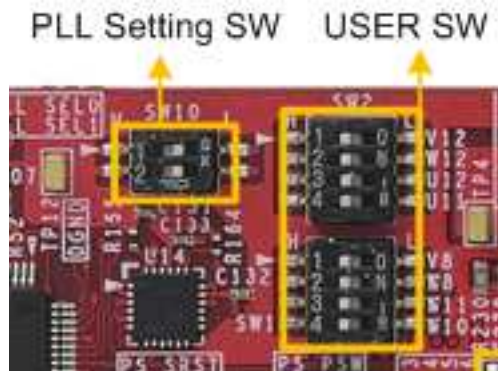
## 7.20. Dip Switches

There are 3 switches on the board.

The following table shows the details of the Dip switches.

**Table 7-24 Dip Switch Function Table**

Switch#	Description	bits	Target IC		
			IC#	Pin#	Net Name
SW1	For PL User Dip Switch Active Low(ON)	1	U15	V8	FP_DIPSW0
		2	U15	W8	FP_DIPSW1
		3	U15	W11	FP_DIPSW2
		4	U15	W10	FP_DIPSW3
SW2		1	U15	V12	FP_DIPSW4
		2	U15	W12	FP_DIPSW5
		3	U15	U12	FP_DIPSW6
		4	U15	U11	FP_DIPSW7
SW10	For PLL Mode Setting	1	U18	21	PLL_SEL0
		2	U18	20	PLL_SEL1



**Figure 7-32 DIP Switch Position**

## 8. Default Settings

The following two tables show default settings of Jumpers and Dip Switches.

**Table 8-1 Default Jumper Settings**

No.	Jumper No.	Default Setting	Note
1	J1	Short	Enable 5V output to USB Connector
2	J2	Short	For Host Mode
3	J3	<2-3>Short	Pmod power 3.3V
4	J4	Open	Soft-reset is only generated by SW8
5	J5	Short	Enable 3.3V output to ARM Trace Port's VTREF pin.
6	J6	<2-3> Short	Boot mode: QSPI
7	J7	<2-3> Short	JTAG: Cascade mode
8	J8	Open	VCC_ADJ select: 2.5V
9	J9	<3-4> Short	VCC_ADJ
10	J10	<2-3> Short	Boot mode: QSPI
11	J11	<1-2> Short	

**Table 8-2 Default Switch Settings**

No.	Jumper No.	bit	Default Setting	Note
1	SW10	1	ON	Please refer to 7.3
2		2	ON	
3	SW1	1	OFF	
4		2	OFF	
5		3	OFF	
6		4	OFF	
7	SW2	1	OFF	
8		2	OFF	
9		3	ON	
10		4	ON	



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