TB100

NPN power transistor

19 December 2013 Product data sheet

1. General description

High voltage, high speed, planar passivated NPN power switching transistor in a SOT54 (TO92) plastic package intended for use in low power SMPS emitter switching circuits.

2. Features and benefits

- Fast switching
- High base current drive capability
- High voltage capability
- Very low switching and conduction losses

3. Applications

- Emitter-switched low power SMPS circuits
- Self Oscillating Power Supplies
- AC-DC converters
- DC-AC inverters

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_C	collector current	DC		-	-	1	A
P_{tot}	total power dissipation	$T_{lead} \leq 25$ °C; Fig. 1		-	-	2	W
T_j	junction temperature			-	-	150	°C
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	-	700	V
Static characteristics							
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA; T_{lead} = 25 °C; Fig. 5; Fig. 6		12	22	32	
		V_{CE} = 5 V; I_C = 100 mA; T_{lead} = 25 °C; Fig. 5; Fig. 6		14	24	34	
		V_{CE} = 5 V; I_C = 0.75 A; T_{lead} = 25 °C; Fig. 5; Fig. 6		12	15.5	20	

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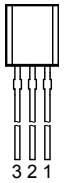
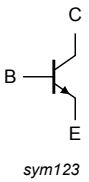
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E	emitter	 TO-92 (SOT54)	 sym123
2	C	collector		
3	B	base		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TB100	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Marking

Table 4. Marking codes

Type number	Marking code
TB100	TB100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	700	V
V_{CBO}	collector-base voltage	I_E = 0 A		-	700	V
I_C	collector current	DC		-	1	A
I_{CM}	peak collector current			-	2	A
I_B	base current			-	0.5	A
I_{BM}	peak base current			-	3	A
P_{tot}	total power dissipation	T_{lead} ≤ 25 °C; Fig. 1		-	2	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C

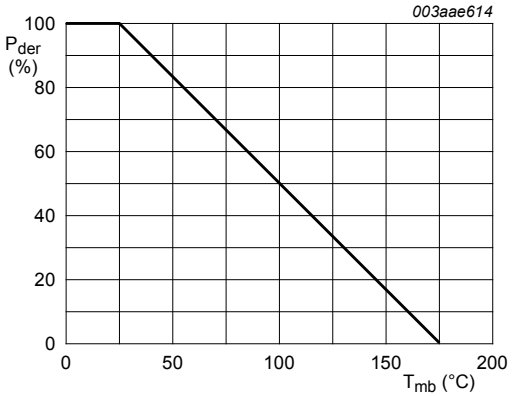


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead			-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	printed circuit board mounted; lead length = 4 mm; Fig. 2		-	150	-	K/W

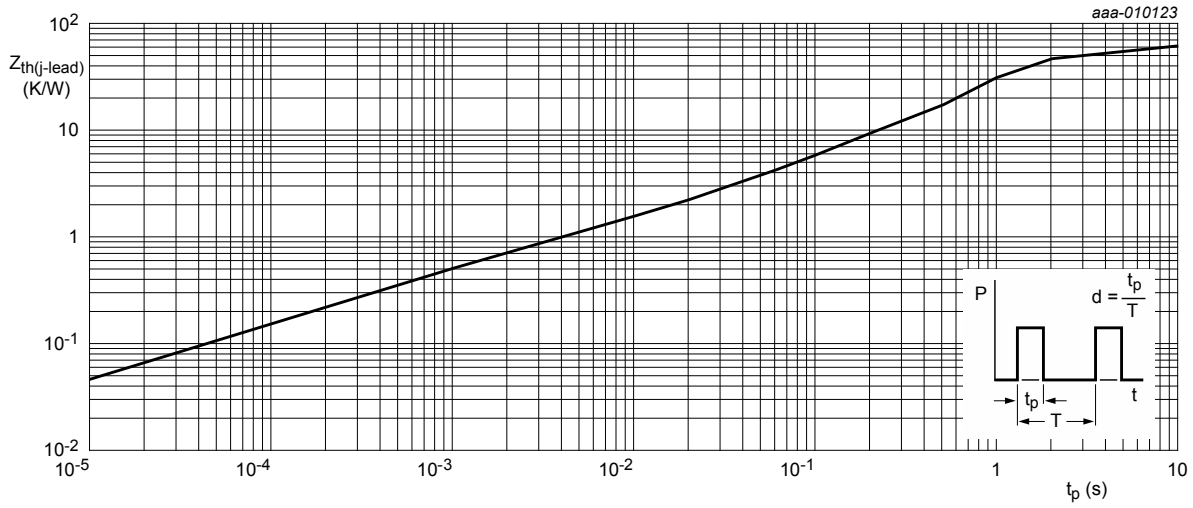


Fig. 2. Transient thermal impedance from junction to lead as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = 700 V; T_{lead} = 25 °C		-	0.8	100	µA
		V_{BE} = 0 V; V_{CE} = 700 V; T_j = 125 °C		-	2	500	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 9 V; I_C = 0 A; T_{lead} = 25 °C		-	0.05	100	µA
V_{CEsat}	collector-emitter saturation voltage	I_C = 0.75 A; I_B = 0.15 A; T_{lead} = 25 °C; Fig. 3		-	0.24	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 0.75 A; I_B = 0.15 A; T_{lead} = 25 °C; Fig. 4		-	0.93	1.3	V
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 5 V; T_{lead} = 25 °C; Fig. 5; Fig. 6		12	22	32	
		I_C = 100 mA; V_{CE} = 5 V; T_{lead} = 25 °C; Fig. 5; Fig. 6		14	24	34	
		I_C = 0.75 A; V_{CE} = 5 V; T_{lead} = 25 °C; Fig. 5; Fig. 6		12	15.5	20	
Dynamic characteristics (resistive load)							
t_s	storage time	I_C = 1 A; I_{Bon} = 0.2 A; I_{Boff} = -0.2 A; R_L = 75 Ω; V_{BB} = -4 V; T_{lead} = 25 °C; Fig. 7; Fig. 8		-	2	-	µs
t_f	fall time			-	320	-	ns

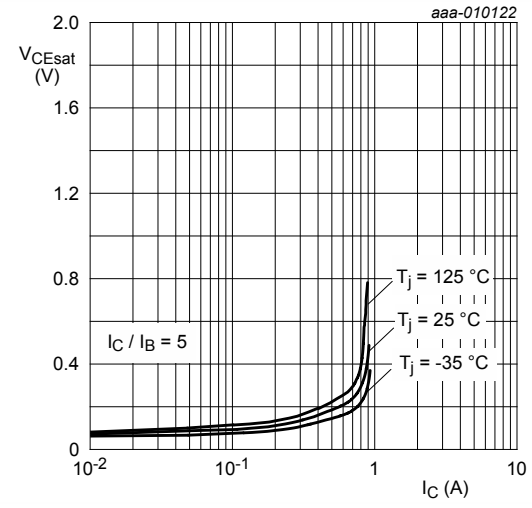


Fig. 3. Collector-emitter saturation voltage as a function of collector current; typical values

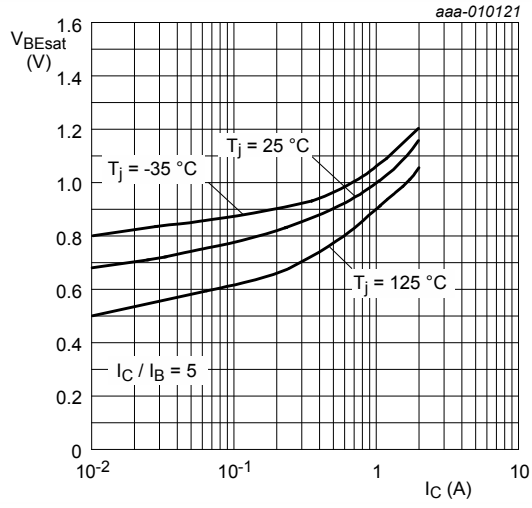


Fig. 4. Base-emitter saturation voltage as a function of collector current; typical values

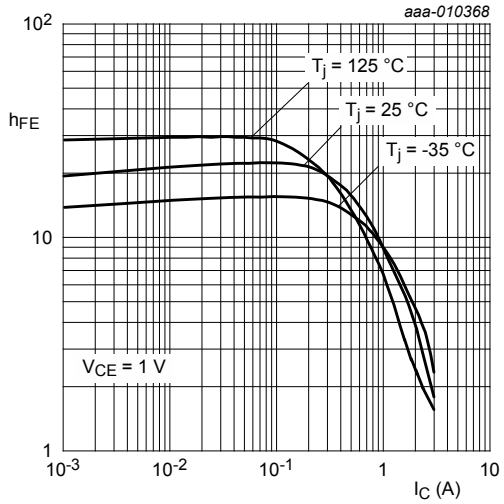


Fig. 5. DC current gain as a function of collector current; typical values

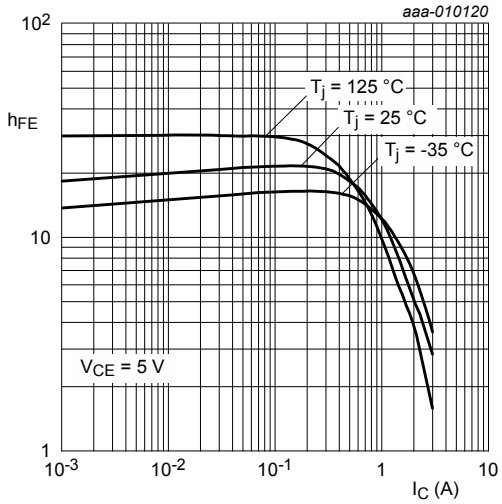


Fig. 6. DC current gain as a function of collector current; typical values

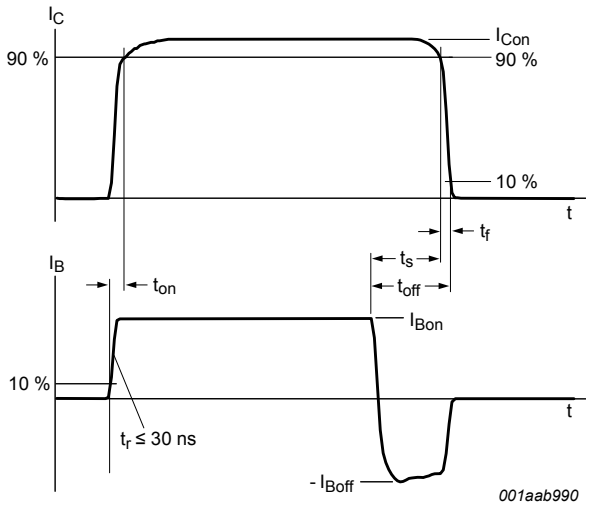


Fig. 7. Switching times waveforms for resistive load

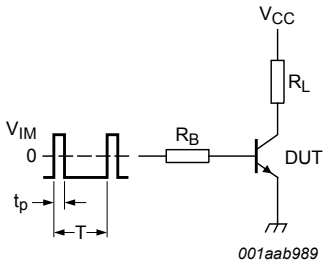


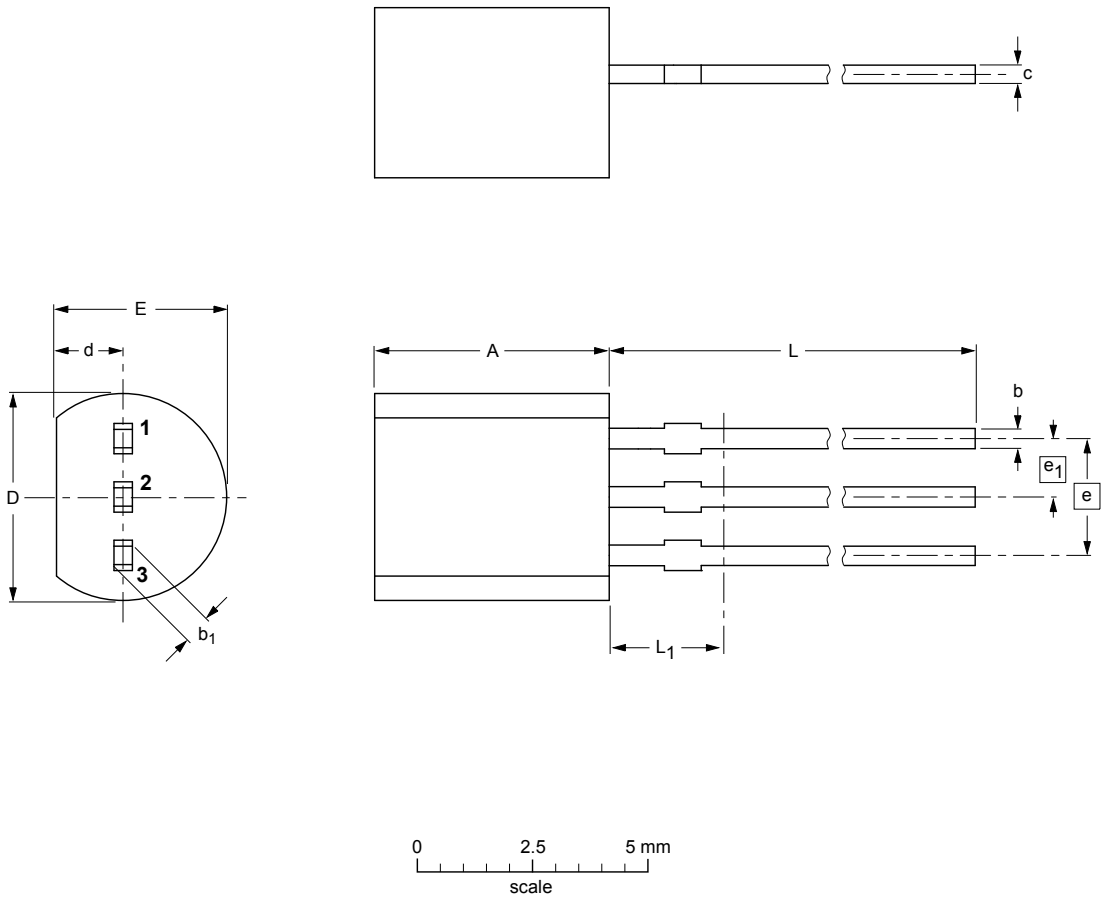
Fig. 8. Test circuit for resistive load switching

$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20\ \mu s$; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

11. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig. 9. Package outline TO-92 (SOT54)

12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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