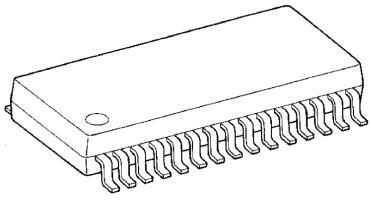
TOSHIBA Bi−CMOS Integrated Circuit Silicon Monolithic

TB2104F

VFD Driver

The TB2104F is a VFD (fluorescent display tube) driver IC implemented by the Bi−CMOS process.
The logic section is configured with CMOS transistors, and the high voltage tolerant output driver section is configured with bipolar transistors.



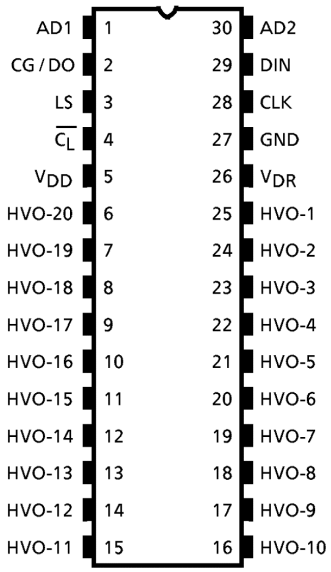
SSOP30-P-375-1.00

Weight: 0.7g (typ.)

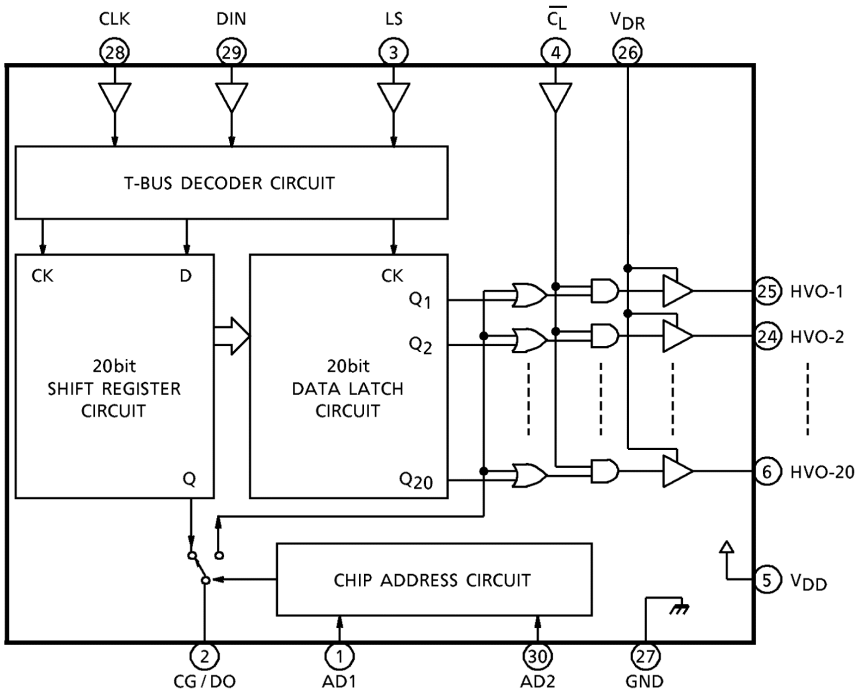
Features

- Incorporates a shift register, latch, and driver capable of handling 20 bits of data.
- The output driver comes with an active pull−down, so it can function as a VFD grid, anode driver.
- Three serial data lines are used to input display data.
- The data receiver section can also accept general−purpose serial data and T−BUS (TOSHIBA semiconductor bus).
- In serial data mode, multiple drivers can be cascaded to expand the handling capacity in 20bit increments.

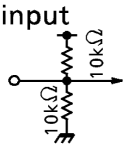
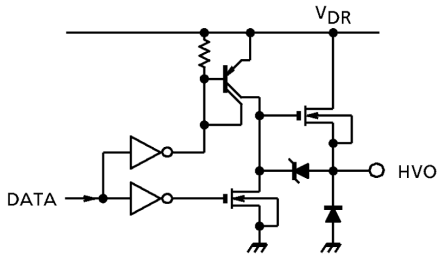
Pin Connection



Block Diagram



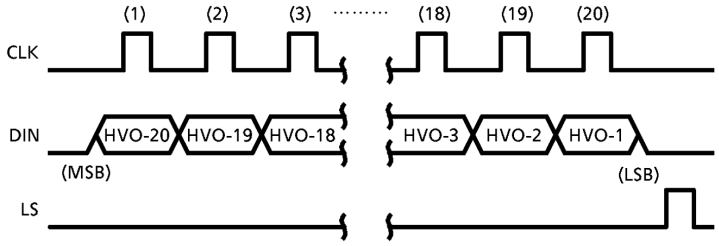
Pin Function

Pin No.	Symbol	Pin Name	Function And Operation	Remarks
1 30	AD1 AD2	Address setting input	・Chip select / address setting inputs ・When using in serial mode, keep AD1 and AD2 “open”. ・In other settings than “open”, it becomes T−BUS mode and addresses up to 8 kinds can be set.	3-value input 
3	LS	Strobe input	・Serial data input terminals ・Inputs display data through the DIN terminal synchronizing with rise of CLK input. ・Display data are updated when inputting “H” level into LS terminal after completing data input. ・In T−BUS mode, LS terminal becomes “period” input.	CMOS input
28	CLK	Clock input		
29	DIN	Data input		
2	CG / DO	Lamp test input and data output	・Lamp test input terminal and data output terminal ・In serial mode (AD1 = AD2 = open), this terminal serves as the serial data output terminal and enables cascade connection of driver IC. ・In T−BUS mode, this terminal serves as the lamp test input and is able to use all the driver outputs (HVO−1~−20) at “H” level by inputting “H” level signal. ・During the normal operation in T−BUS mode, use this terminal by fixing at “L” level.	CMOS input / CMOS output built in pull−down resistor 20kΩ
4	$\overline{C_L}$	Clear input	・Driver off (blanking) input terminal ・All the driver outputs are fixed at “L” level when “L” level signal is input. ・When “H” level signal is input, it becomes the normal mode.	CMOS input built in pull−up resistor 20kΩ
5	V_{DD}	Logic unit power supply	・Power supply and GND terminals	—
26	V_{DR}	Drive unit power supply		
27	GND	Ground		
25 24 23 ⋮ ⋮ 8 7 6	HVO−1 HVO−2 HVO−3 ⋮ ⋮ HVO−18 HVO−19 HVO−20	Driver output	・High−tension driver output terminal ・Equivalent circuit 	—

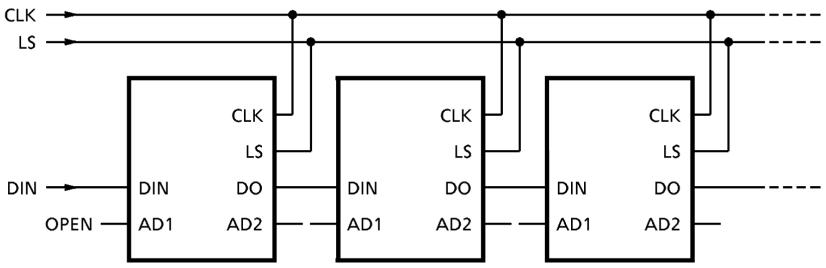
Explanation Of Operation

1. Serial data receiver circuit
   - The serial data receiver circuit can be changed over to operate in the serial mode or the T–BUS mode by switching, the AD1 / AD2 terminals.
   - In T–BUS mode, the AD1 / AD2 terminals become the chip select code inputs and it becomes possible to connect up to 8 drivers on the same bus line.

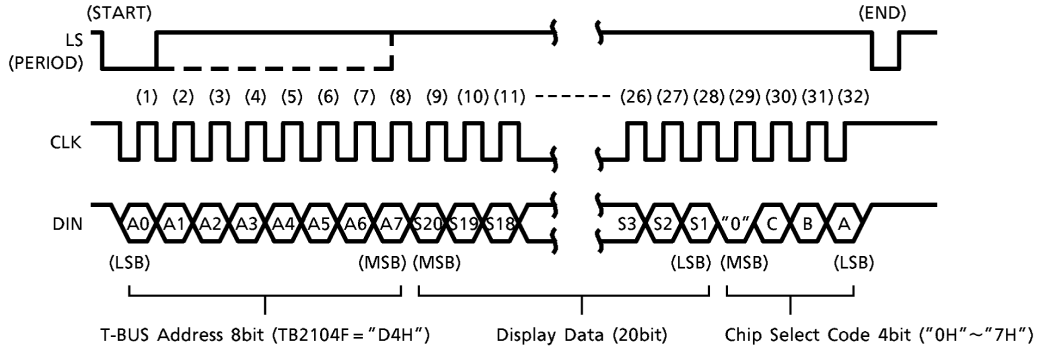
   1) Input data format in serial data mode (AD1 = AD2 = "open")



   - Display data are updated when data for 20 bits are input from MSB side (HVO–20), synchronizing with rise of CLK signal and LS input is set to "H" level after inputting data.
   - When increasing driver ICs, connect them through cascade connection as shown below:



2. Input data format in T–BUS mode

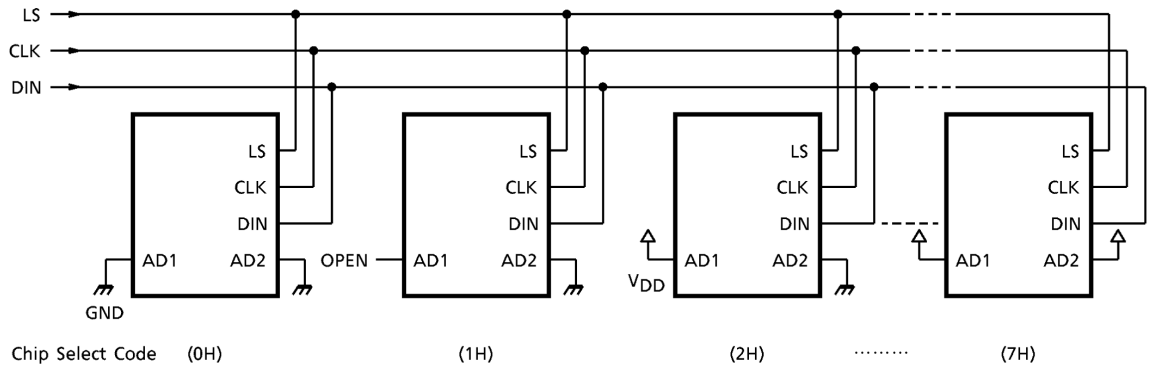


- In T–BUS mode, start data transmission with the LS terminal (period) set at "L" level.
  Thereafter, send address data 8 bits, display data 20 bits, and chip select code 4 bits, synchronizing with rise of CLK signal.
- After sending data, set the LS terminal to "L" level again and terminate the data sending.
- On a driver IC when chip select code agrees with chip select code by AD1 / AD2, display data are updated at fall of LS signal.
- When increasing driver ICs, it is possible to connect up to 8 ICs on the same bus line in combination with AD1 / AD2.
- T–BUS address of the TB2104F is "D4H".
- When data are transferred using T–BUS address "00H", the data can be input to all the driver ICs on the bus line independently of chip select codes ("0H"~"7H"). (This function can be used for power on reset.)

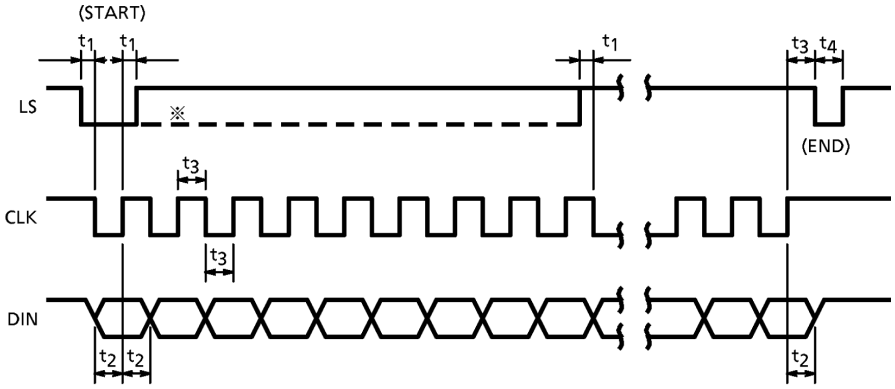
3. AD1 / AD2 input and chip select codes
   AD1 / AD2 input are 3–value level inputs and 9 kinds (3×3) of codes can be set.

AD1	AD2	A	B	C	Chip Select Code	Mode
V_{IH}	V_{IH}	1	1	1	"7H"	T–BUS
V_{IM}		0	1	1	"6H"	
V_{IL}		1	0	1	"5H"	
V_{IH}	V_{IM}	0	0	1	"4H"	
V_{IM}		—	—	—	—	Serial
V_{IL}		1	1	0	"3H"	T–BUS
V_{IH}	V_{IL}	0	1	0	"2H"	
V_{IM}		1	0	0	"1H"	
V_{IL}		0	0	0	"0H"	

4. Example of extension of driver ICs in T–BUS mode chip select code



5. T–BUS mode timing chart



- $f_{CLK} \leq 500kHz$
- $t_1 \geq 0.2\mu s$, $t_2 \geq 0.2\mu s$
- $t_3 \geq 1.0\mu s$, $t_4 \geq 1.0\mu s$

Cautions for use

- Therefore, multiple driver outputs may possibly become “H” level simultaneously after the power is turned on.
  (In this case, the allowable power dissipation of a device using this IC may possible be exceeded, destroying the device.)
- In order to avoid this, while keeping the clear terminal ($\overline{C_L}$) at “L” level, rise the power supply for the logic unit (V_{DD}) and then, that for the drivers (V_{DR}), reset all the contents of the data latch (“L” level) by serial data, and initialize the driver outputs.

Maximum Ratings (Ta = 25°C)

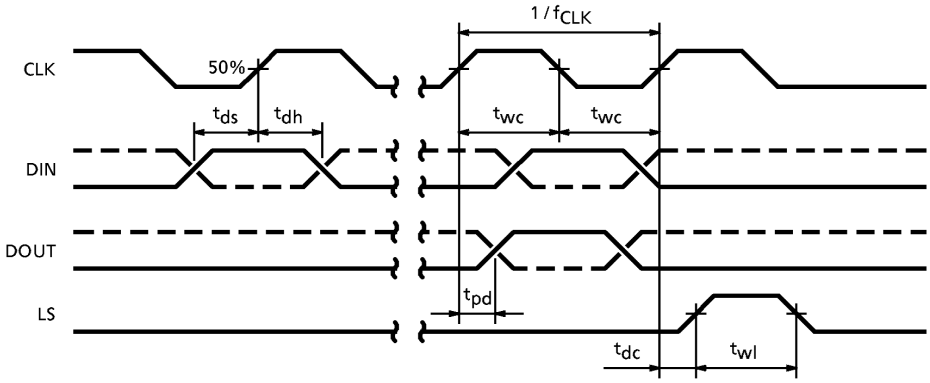
Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~7.0	V
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Driver voltage	V_{DR}	V_{DD}~60	V
Driver current	I_{DR}	50	mA
Power dissipation	P_D (Note)	800	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−55~150	°C

(Note) In case it is used at more than Ta = 25°C, it is considered by reducing 6.4mW each 1°C.

Electrical Characteristics (unless otherwise specified, V_{DD} = 5V, V_{DR} = 50V, Ta = 25°C)

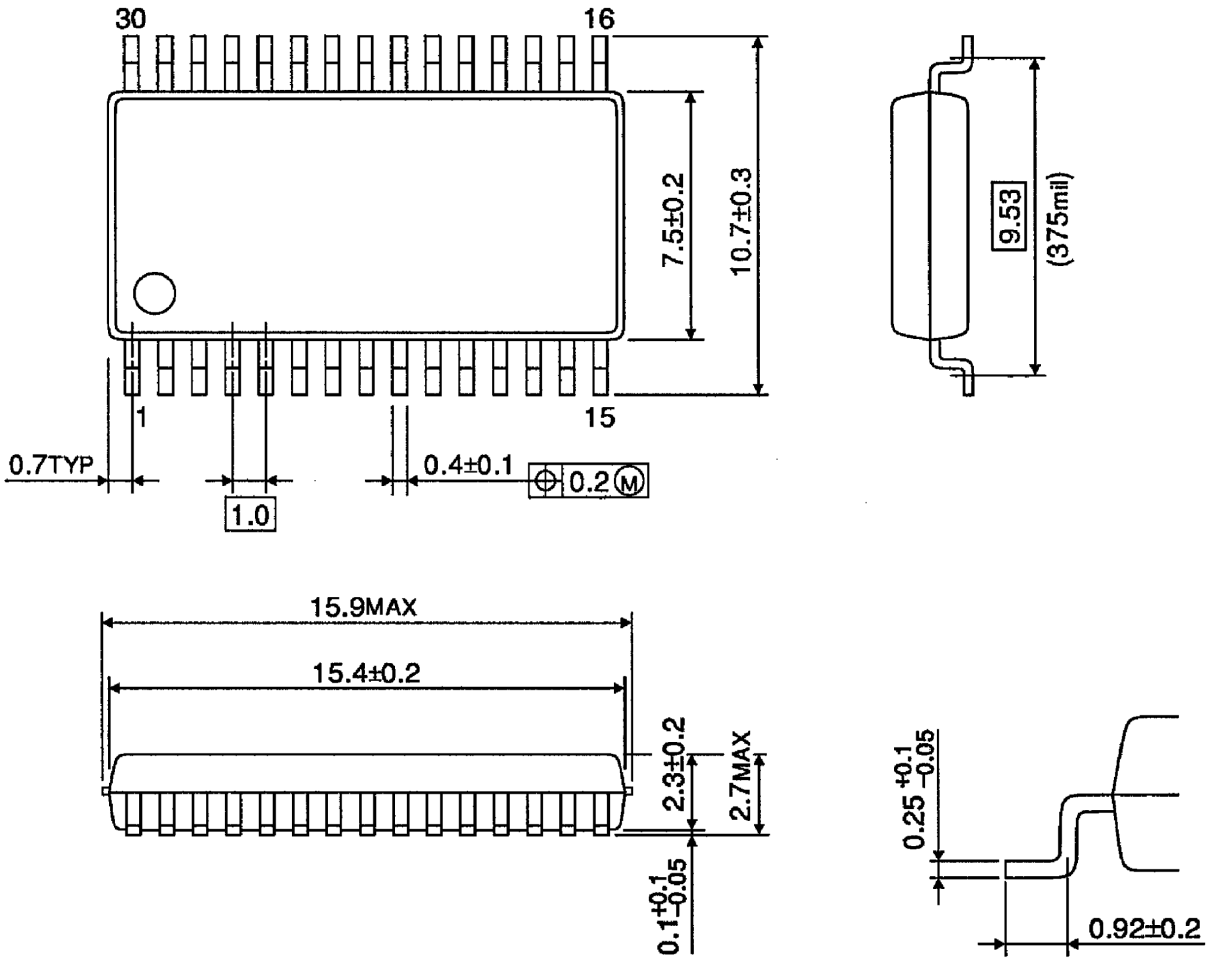
Characteristic		Symbol	Test Cir− cuit	Test Condition		Min.	Typ.	Max.	Unit
Operating supply voltage (1)		V_{DD}	—	Logic unit		4.5	5.0	5.5	V
Operating supply voltage (2)		V_{DR}	—	Driver unit		10	~	50	V
Operating supply current (1)		I_{DD}	—	No load, no input		—	0.3	1.5	mA
Operating supply current (2)		I_{DR}	—	No load, output V_{OL} level		—	2.3	3.5	mA
Input voltage	"H" level	$V_{IH\ (1)}$	—	CMOS input terminal DIN, CLK, LS, CG, $\overline{CL}$		V_{DD} ×0.7	~	V_{DD}	V
	"L" level	$V_{IL\ (1)}$				GND	~	V_{DD} ×0.3	
Input voltage	"H" level	$V_{IH\ (2)}$	—	3−value input terminal AD1, AD2		V_{DD} −0.5	~	V_{DD}	V
	Open	V_{IM}				—	V_{DD} ×0.5	—	
	"L" level	$V_{IL\ (2)}$				GND	~	GND +0.5	
Input current	"H" level	I_{IH}	—	CMOS input terminal	V_{IH} = 5V	−1.0	~	1.0	μA
	"L" level	I_{IL}			V_{IL} = 0V	−1.0	~	1.0	
Input resistance		R_{IN}	—	3−value input terminal		80	100	120	kΩ
Output current	"H" level	$I_{OH\ (1)}$	—	HVO−1~−20 output terminal	V_{OH} = 45V	—	−8.4	−5	mA
	"L" level	$I_{OL\ (1)}$			V_{OL} = 3V	2.0	2.7	—	
Output current	"H" level	$I_{OH\ (2)}$	—	DO output terminal	V_{OH} = 4V	—	−0.3	−0.1	mA
	"L" level	$I_{OL\ (2)}$			V_{OL} = 1V	0.1	0.3	—	
Clock frequency		f_{CLK}	Fig. 1	CLK max. operating		—	5.0	4.0	MHz
Clock pulse width		t_{wc}		CLK min. operating		75	60	—	ns
Data setup time		t_{ds}		DIN min. operating pulse width		50	40	—	ns
Data hold time		t_{dh}				50	40	—	ns
LS pulse width		t_{wl}		LS min. operating		80	60	—	ns
CLK−LS delay time		t_{dc}		CLK→LS delay time		50	40	—	ns
CLK−DOUT delay time		t_{pd}		CLK→DOUT delay time CL = 30pF		—	120	160	ns

Fig. 1: Serial data timing chart



Package Dimensions

SSOP30-P-375-1.00 Unit : mm



Weight: 0.7g (typ.)

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