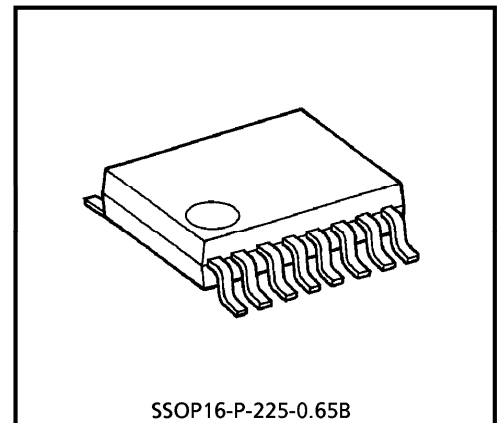


# TB31206FN, TB31206AFN

## PLL FREQUENCY SYNTHESIZER

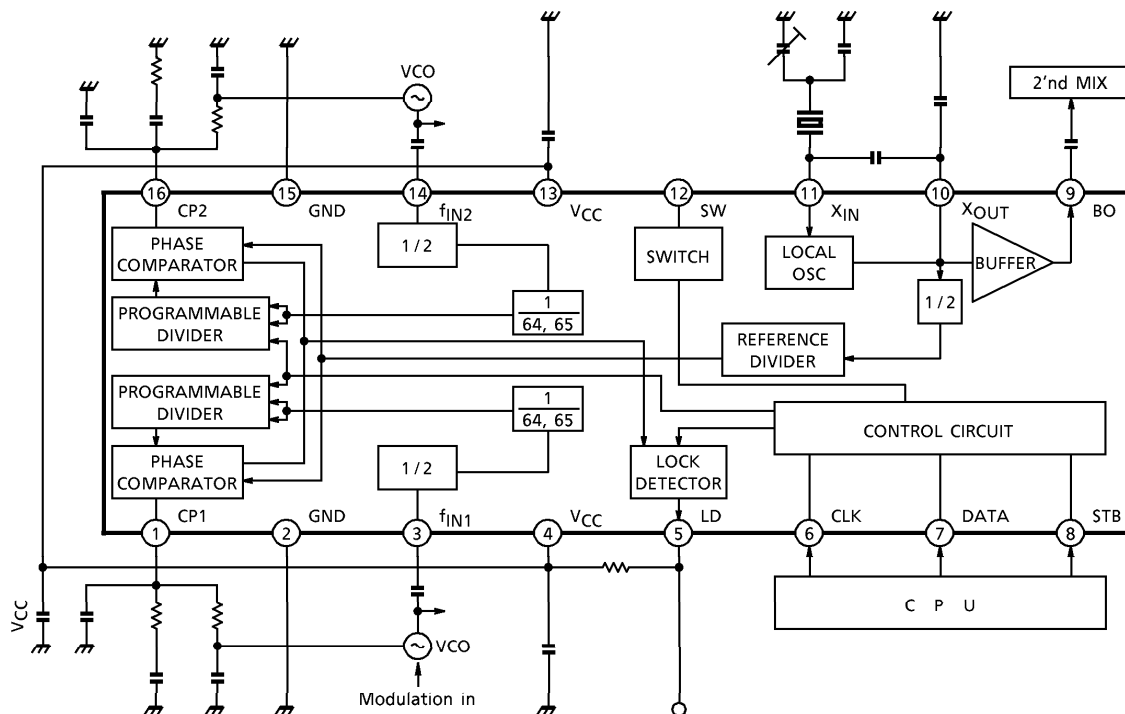
### FEATURES

- One packaging CH1/CH2 two systems prescaler and PLL.
- Low operating power supply voltage  
:  $V_{CC} = 2.7 \sim 5.5 \text{ V}$
- Low current consumption FN :  $I_{CC} = 16.5 \text{ mA (Typ.)}$   
AFN :  $I_{CC} = 14.5 \text{ mA (Typ.)}$
- Input frequency :  $f_{IN} = 520 \sim 1100 \text{ MHz}$
- High input sensitivity :  $V_{IN} = 92 \sim 107 \text{ dB}\mu\text{V}$
- Charge pump is constant current type, and is able to change output current by serial data
- Reference oscillation circuit is adopted circuit of bipolar, so getting the stable X'tal oscillation circuit
- Available standby control in CH1 and CH2 independent of each other
- The very small package : SSOP16pin (0.65 mm pitch)



Weight : 0.07 g (Typ.)

### BLOCK DIAGRAM



**PIN FUNCTION** (The values of resistor and capacitor are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	CP1	Output terminal of charge pump. Charge pump is constant current output circuit, and output current is varied by input serial data.	
16	CP2		
2	GND	GND Terminal.	—
15	GND		
3	f <sub>IN1</sub>	Input terminal of RF oscillation signal.	
14	f <sub>IN2</sub>		
4	V <sub>CC</sub>	Power Supply Terminal.	—
13	V <sub>CC</sub>		
5	LD	Output terminal of lock detector. It is the open drain output.	
12	SW	Switchover terminal for constant of loop filter. It is the open drain output. When don't switch constant of loop filter, available general output.	
6	CLK	Input terminal of clock.	
7	DATA	Input terminal of serial data.	
8	STB	Input terminal of strobe signal.	
9	BO	Output terminal of buffer amplifier. The signal of local oscillation is output through the buffer amplifier.	
10	X <sub>OUT</sub>	Output terminal of local oscillation signal.	
11	X <sub>IN</sub>	Input terminal of local oscillation signal. In case of external input, connecting it to this terminal.	

**DESCRIPTION OF FUNCTION AND OPERATION**

1. Entry of serial data

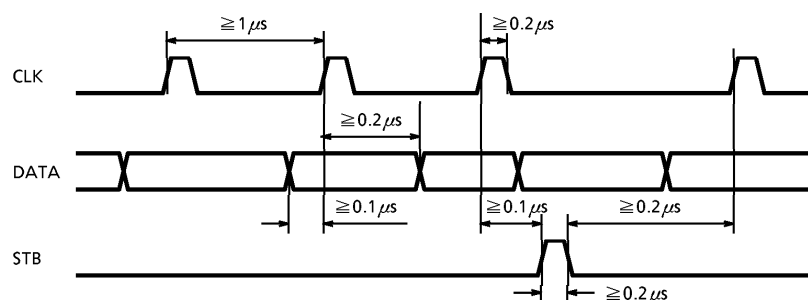
- Serial data used to control the IC is input through three terminals, CLK, DATA and STB.
  - ① During the rise of a clock pulse, data is fed to the shift register in the IC in order from the LSB.
  - ② Upon the reception of all data, the strobe signal (STB) is made "H".
  - ③ After the situation of ②, the data stored in the shift register is transferred to the latch in the block selected by the group code, whereby the IC is controlled.
- The three terminals, CLK, DATA and STB, contains Schmitt trigger circuits to prevent the data errors by noise, etc.

○ Serial data group and group code

- The IC has control divided into four groups so that they may be controlled independent of one another. Each group is identified by a two-bit group code attached at the data end.

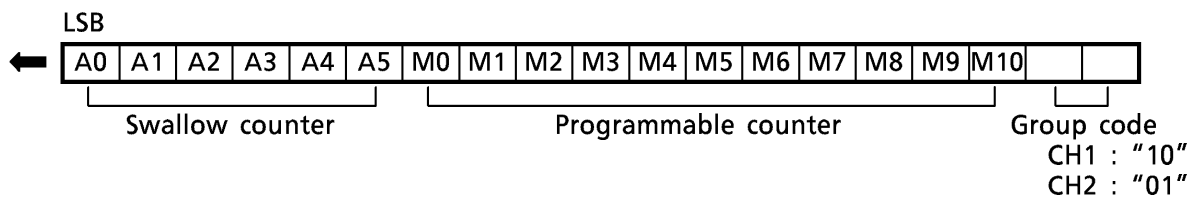
CODE	ITEM
10	Number of divisions by CH1 programmable divider ( $f_{IN1}$ )
01	Number of divisions by CH2 programmable divider ( $f_{IN2}$ )
11	Number of divisions by reference divider ( $X_{IN}$ )
00	Optional control

○ Serial data input timing



2. CHANNEL dividers (CH1, CH2)

- These programmable dividers are composed of a half fixed divider, a 6bit swallow counter (6bit programmable divider), a 11bit programmable counter, and a two-modular prescaler providing 64 and 65 divisions.
- The strategy of a swallow counter is used to set high reference frequency.
- Sending certain data to the swallow counter and the programmable counter allows the setting of any of 8064 to 262142 divisions (multiple of two).
- The programmable counter and swallow counter are set by each channel. Each channel is specified by a group code.



$$A = A_0 + A_1 \times 2^1 + \dots + A_5 \times 2^5$$

$$M = M_0 + M_1 \times 2^1 + \dots + M_{10} \times 2^{10}$$

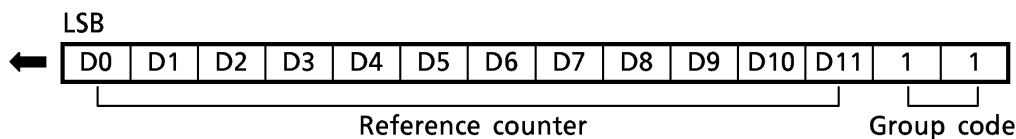
$$\text{Number of divisions} = 2(64N + A)$$

$$8064 \leq \text{Number of divisions} \leq 262142$$

(EX) A Signal of 900MHz is entered into  $f_{IN1}$ , being divided into 25.0kHz step.  
 (Reference frequency is 12.5kHz)  
 $900 \times 10^6 \div (25.0 \times 10^3 \div 2) = 72000$   
 $72000 = 2(64N + A)$   
 $\therefore N = 562, A = 32$

3. Reference divider

- This block generates the reference frequency for the PLL.
- This reference divider is composed of a 12bit reference counter and a half fixed divider.
- Sending certain data to the reference divider allows the setting of any of 6 to 8190 divisions (multiple of two).



$$D = D_0 + D_1 \times 2^1 + \dots + D_{10} \times 2^{10} + D_{11} \times 2^{11}$$

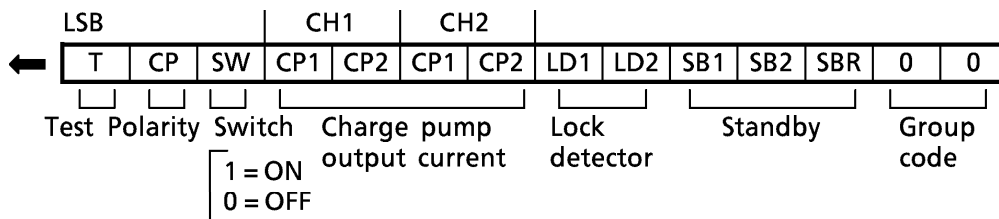
$$\text{Number of divisions} = 2D$$

$$6 \leq \text{Number of divisions} \leq 8190$$

(EX) With a 12.8MHz X'tal oscillator connected, being divided into 25.0kHz step.  
 (Reference frequency is 12.5kHz)  
 $12.8 \times 10^6 \div (25.0 \times 10^3 \div 2) = 1024$   
 $2D = 1024$   
 $\therefore D = 512$

4. Optional control

- The optional control below is available.
  - ① Test mode (Usually set up T = "0").
  - ② Control and polarity control of the charge pump output current for each channel.
  - ③ Output terminal for lock detector.
  - ④ Standby control of CH1, CH2 and reference divider.
  - ⑤ Control of filter switch.



- T : Bit for test mode
- CP : Switchover bit for charge pump output polarity
- SW : Control bit for filter switch
- CP1, 2 : Switchover bit for charge pump output current
- LD1, 2 : Control bit for lock detector output
- SB1, 2 : Standby control bit for CH1, CH2
- SRB : Standby control bit for reference divider

- Description of options including their control

① Test mode (T)

Bit "T" is for test mode. In other than the test mode, set this bit at "0".

② Control of charge pump output current (CP1, CP2)

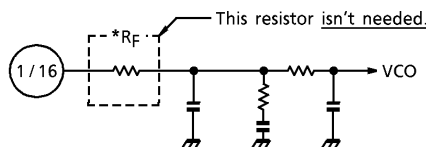
This IC uses a constant current output type charge pump circuit. Output current is varied by serial data "CP1" and "CP2".

**CHARGE PUMP OUTPUT CURRENT**

CONTROL BIT		CHARGE PUMP OUTPUT CURRENT
CP1	CP2	
0	0	± 100 μA
0	1	± 200 μA
1	0	± 400 μA
1	1	± 800 μA

High speed lock up is possible by switching charge pump output current.

(Note)



Charge pump output polarity (CP)

Bit "CP" can be reversed charge pump output polarity.

**CHARGE PUMP OUTPUT POLARITY**

CP	OUTPUT POLARITY
0	Normal
1	Reverse

③ Lock detector output

When phase comparator detects phase difference, LD terminal (pin 5) outputs "L". When phase comparator locks, LD terminal outputs "H". On standby, outputs "H".

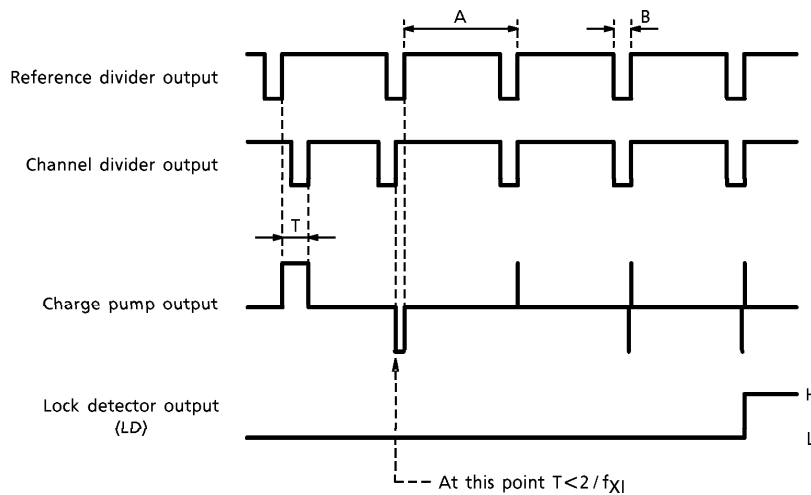
LD terminal output is controlled by "SB1", "SB2", "LD1" and "LD2".

CONTROL BIT				5PIN OUTPUT
SB1	SB2	LD1	LD2	
0	0	0	0	L
		0	1	CH2 only detect
		1	0	CH1 only detect
		1	1	CH1 * CH2
0	1	0	0	L
		0	1	H
		1	0	CH1 only detect
		1	1	CH1 only detect
1	0	0	0	L
		0	1	CH2 only detect
		1	0	H
		1	1	CH2 only detect
1	1	0	0	L
		0	1	H
		1	0	H
		1	1	H

→ Logical multiplication (AND) of CH1, CH2

About SB1, SB2 bit

0 : Normal operation  
1 : Standby



$f_{X1}$  ..  $X_{1N}$  operating frequency (X'tal OSC)

T .... The time difference of the pulse between reference divider output and channel divider output. (Phase difference)

$f_{PC}$  .. Phase comparison frequency

$$A = \frac{\text{Number of divisions by reference divider}}{f_{X1}} \text{ (s)} = \frac{1}{f_{PC}} \text{ (s)}$$

$$B = 2 / f_{X1} \text{ (s)}$$

When the situation that T is less than B ( $T < B$ ) continues more than  $3 / f_{PC}$  (s), lock detector outputs "H".

④ Standby control (SB1, SB2, SBR)

Standby control by three bits (SB1, SB2, SBR).

Bits "SB1" and "SB2" do standby control of CH1, CH2. Bit "SBR" does standby control of reference divider.

CONTROL BIT			STATE		
SB1	SB2	SBR	CH1	CH2	REFERENCE DIVIDER
0	0	*	ON	ON	ON
0	1	*	ON	OFF	ON
1	0	*	OFF	ON	ON
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF

Interlocking mode

REFERENCE DIVIDER ON mode

Note : \* is don't care.

## ⑤ Filter switch control (SW)

Control of SW terminal by bit "SW".

This terminal is for switching constant of loop filter.

Output type of this terminal is open drain output. Switching the resistor of loop filter by this terminal with switching charge pump output current, high mode and normal mode can operate PLL by ideal braking factor.

When constant of loop filter don't change switch, available general output.

FILTER SWITCH CONTROL

SW	OUTPUT
0	OFF
1	ON

## 5. X'tal oscillation circuit and buffer amplifier

This IC has a stable oscillation circuit composed of bipolar.

In case of the external input of reference frequency directly, use X<sub>IN</sub> terminal (pin 11).

For the common use of X'tal of the X'tal oscillation circuit for the PLL and X'tal of the local oscillation to 2'nd MIX, output terminal of local oscillation signal with buffer amplifier (pin 9) may be used.

This terminal (pin 9) is provided with a buffer amplifier.



**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>CC</sub>	6	V
Power Dissipation	P <sub>D</sub>	560	mW
Operating Temperature	T <sub>opr</sub>	-30~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

**ELECTRICAL CHARACTERISTICS**

(Unless otherwise specified, V<sub>CC</sub> = 3.0V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V <sub>CC</sub>	1	—	2.7	3.0	5.5	V
Operating Current Consumption : FN	I <sub>CCQ</sub>	1	CH1, CH2 operating	—	16.5	21.5	mA
Operating Current Consumption : AFN				—	14.5	19.5	
f <sub>IN</sub> Operating Frequency	f <sub>IN1</sub>	1	V <sub>IN1</sub> = 92~107dB <sub>μ</sub> V *1	520	—	1100	MHz
	f <sub>IN2</sub>	1	V <sub>IN2</sub> = 92~107dB <sub>μ</sub> V *1	520	—	1100	
f <sub>IN</sub> Input Sensitivity	V <sub>IN1</sub>	1	f <sub>IN1</sub> = 520~1100MHz *1	92	—	107	dB <sub>μ</sub> V
	V <sub>IN2</sub>	1	f <sub>IN2</sub> = 520~1100MHz *1	92	—	107	
X <sub>IN</sub> Operating Frequency	f <sub>XI</sub>	1	V <sub>XI</sub> = 102~112dB <sub>μ</sub> V Sin-wave*1	5	—	25	MHz
X <sub>IN</sub> Input Voltage	V <sub>XI</sub>	1	f <sub>XI</sub> = 5~25MHz	102	107	112	dB <sub>μ</sub> V
Input Voltage	V <sub>IH</sub>	—	STB, DATA, CLK	V <sub>CC</sub> × 0.8	V <sub>CC</sub>	5.7	V
	V <sub>IL</sub>	—	STB, DATA, CLK	-0.2	0	V <sub>CC</sub> + 0.2	
CLK Input Frequency	f <sub>CLK</sub>	—	CLK	—	—	1.0	MHz
Charge Pump Output Current	I <sub>CP1</sub>	1	"CP1" = 0, "CP2" = 0, V <sub>CP</sub> = 1.5V	—	± 100	—	μA
	I <sub>CP2</sub>	1	"CP1" = 0, "CP2" = 1, V <sub>CP</sub> = 1.5V	—	± 200	—	
	I <sub>CP3</sub>	1	"CP1" = 1, "CP2" = 0, V <sub>CP</sub> = 1.5V	—	± 400	—	
	I <sub>CP4</sub>	1	"CP1" = 1, "CP2" = 1, V <sub>CP</sub> = 1.5V	—	± 800	—	
Charge Pump OFF Leak Current	CPOFF	1	Standby mode, V <sub>CP</sub> = 1.5V	-1.0	—	1.0	μA

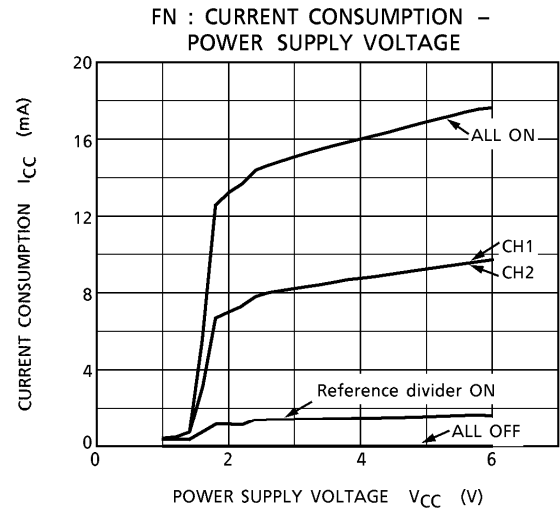
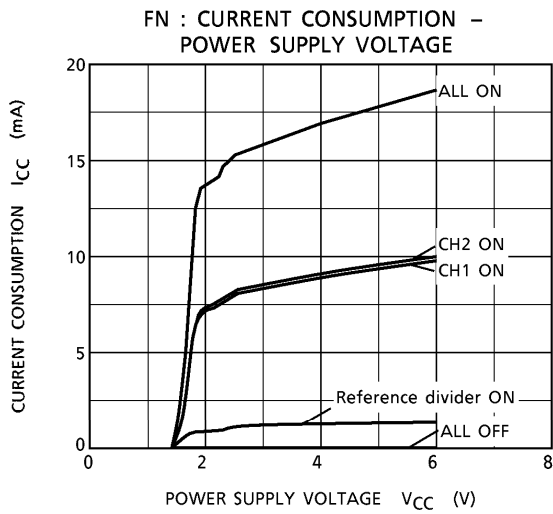
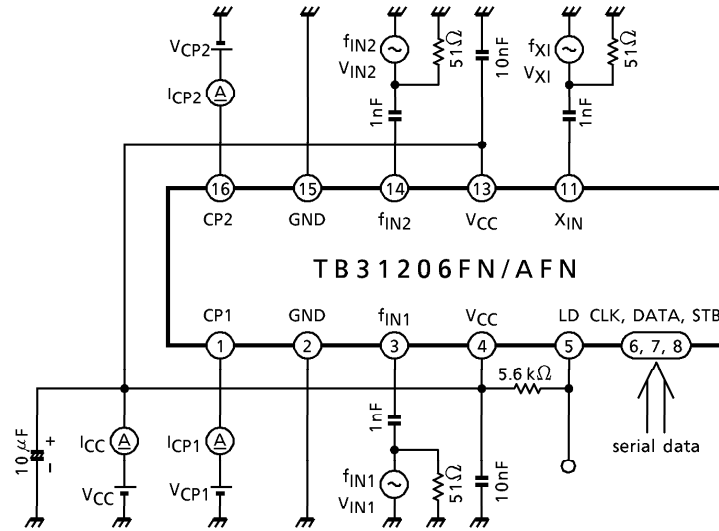
\*1 : When input is terminated with 50Ω.

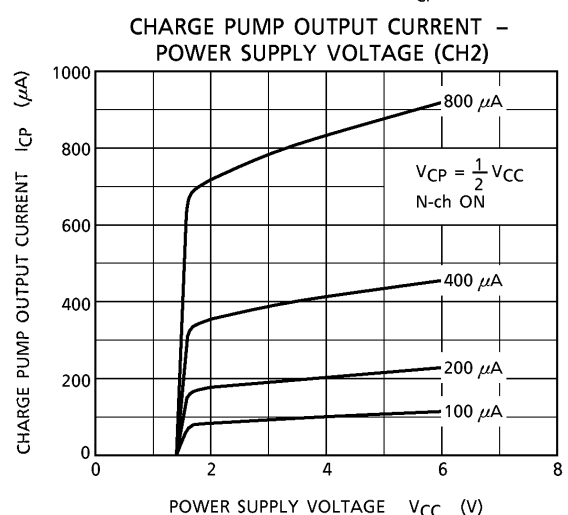
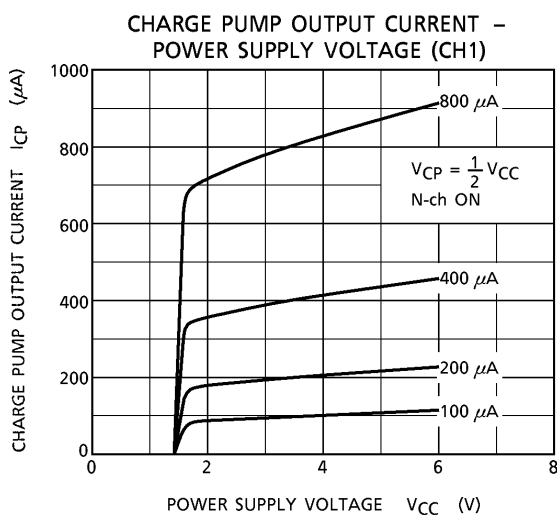
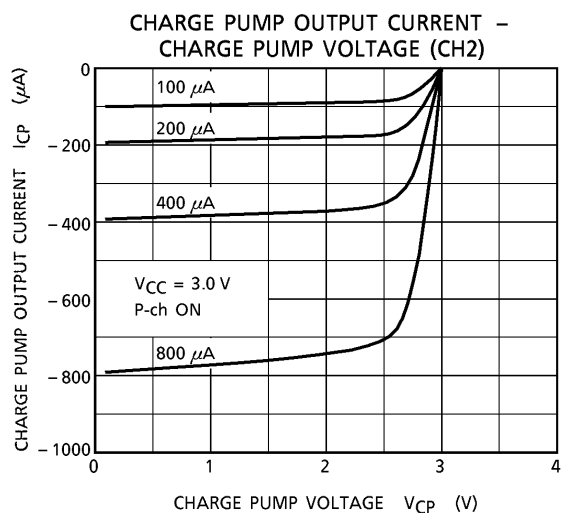
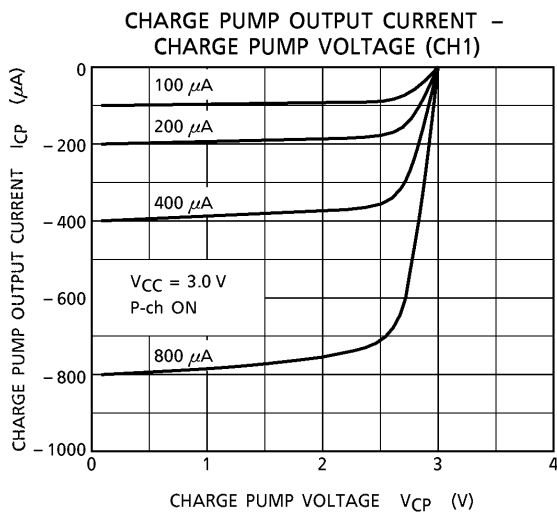
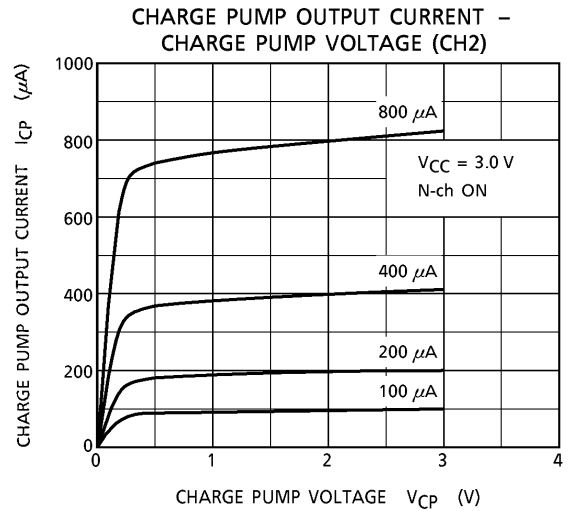
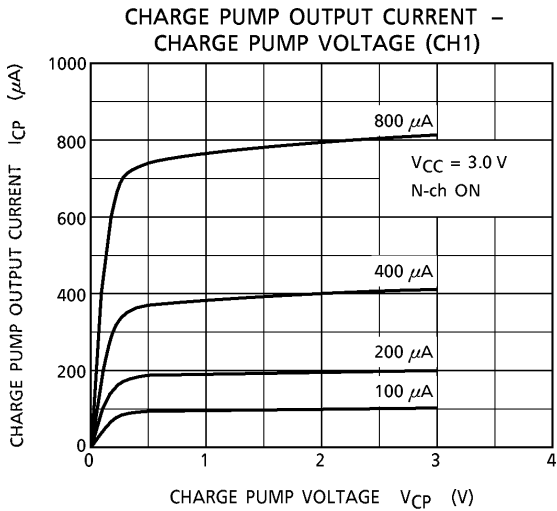
**REFERENCE DATA (Typ.)**

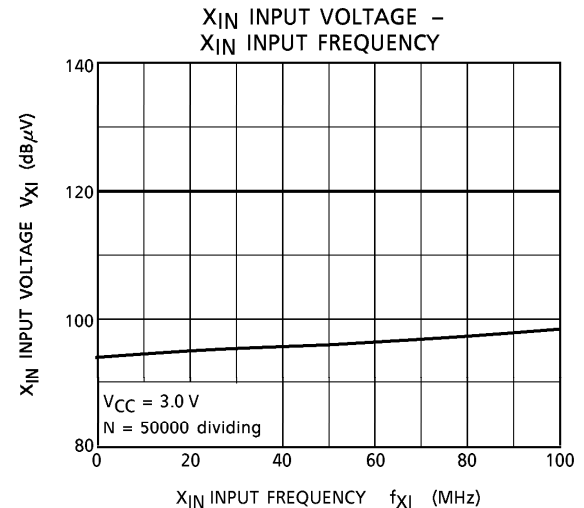
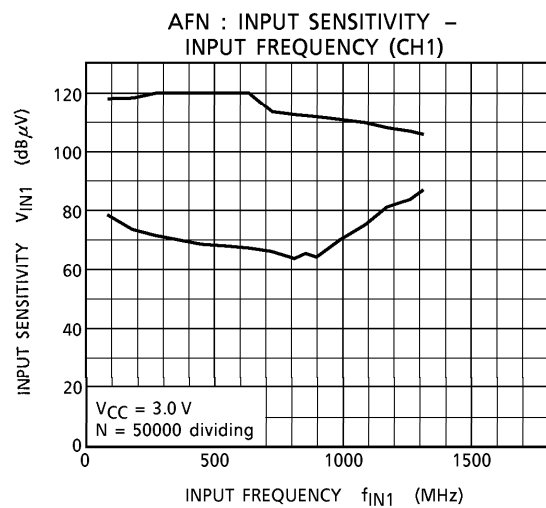
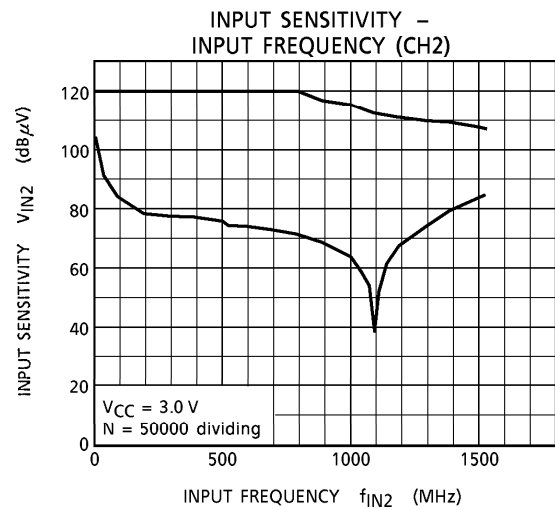
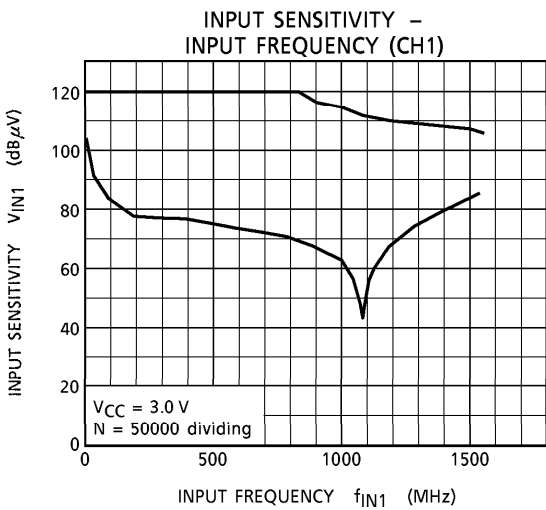
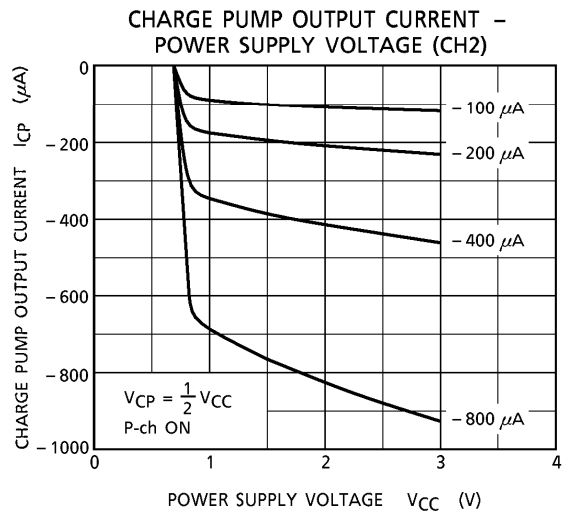
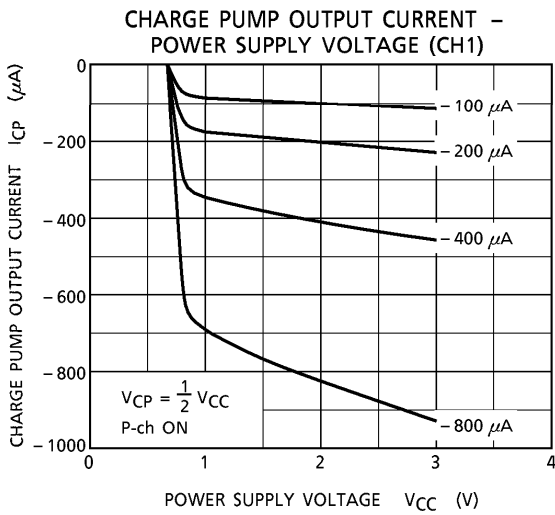
CH1	CH2	REFERENCE DIVIDER	CURRENT CONSUMPTION		UNIT
			FN	AFN	
N	N	ON	16.5	14.5	mA
N	S	ON	9.0	8.0	mA
S	N	ON	9.0	8.0	mA
S	S	ON	1.4	1.4	mA
S	S	OFF	0	0	μA

N : Normal operating  
S : Standby mode

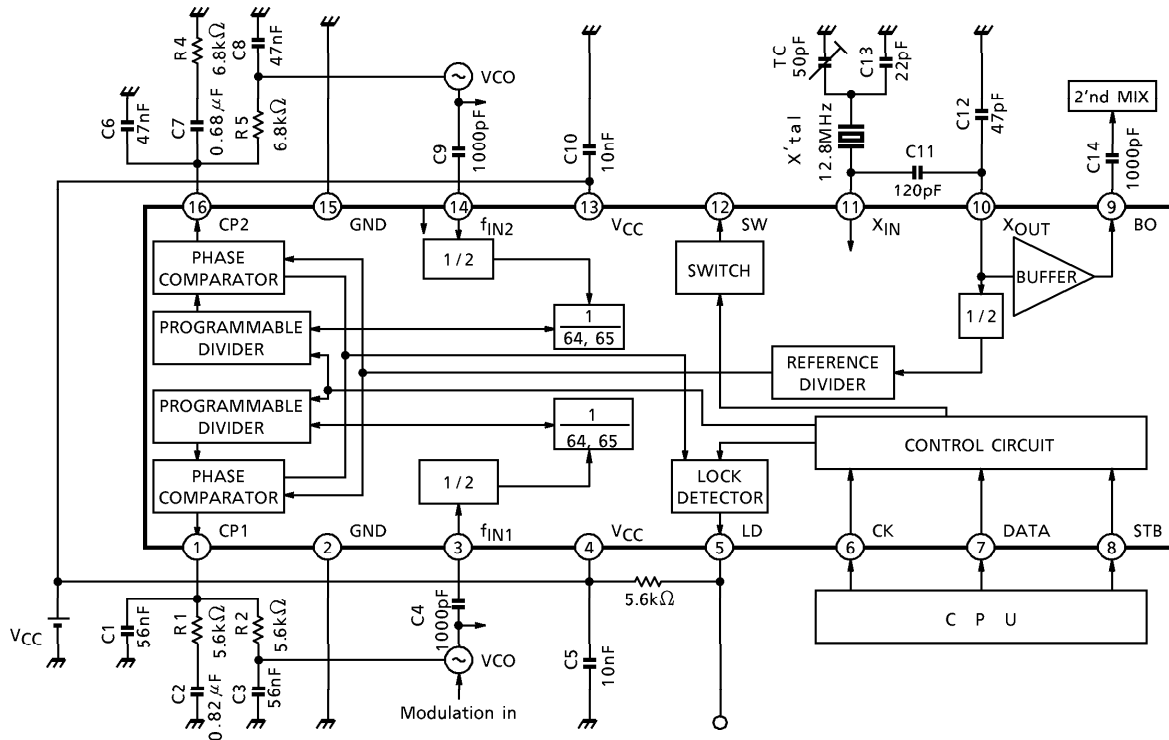
TEST CIRCUIT







APPLICATION CIRCUIT



Set up conditions (E-TACS)

- 1. Frequency bandwidth ; 32.975MHz
- 2. Frequency probability error ; ± 1kHz
- 3. Lock up time ; 30ms (calculated value)
- 4. X'tal frequency ( $f_{X1}$ ) ; 12.8MHz
- 5. Phase comparison frequency ( $f_{pC}$ ) ; 12.5kHz
- 6. Charge pump current ( $I_{CP}$ ) ; 800 $\mu$ A

TX (CH1)

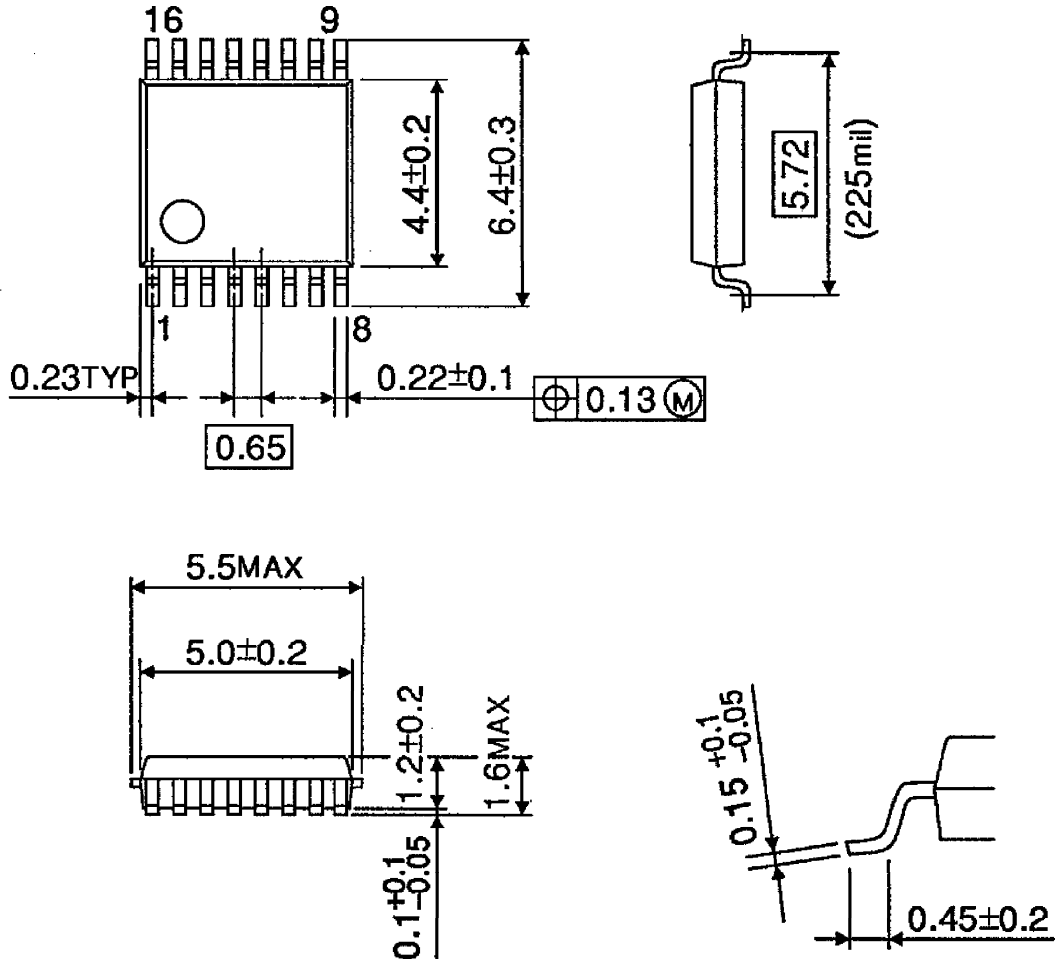
- VCO frequency ; 888.5MHz (center)
- VCO conversion sensitivity ; 14MHz / V

RX (CH2)

- VCO frequency ; 978.5MHz (center)
- VCO conversion sensitivity ; 13MHz / V

**PACKAGE DIMENSIONS**  
SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07 g (Typ.)

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000707EBA

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