

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

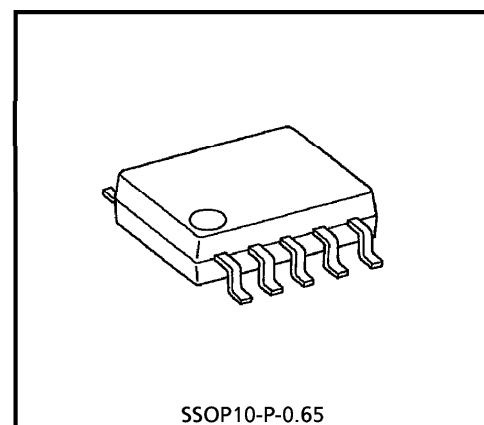
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PLL Frequency Synthesizer for PHS

TB31245FN is a PLL frequency synthesizer used for application of the digital mobile communication.

FEATURES

- Operating frequency : 1610.5 MHz to 1699.5 MHz
- Current consumption : 4.8 mA (Typ.)
- Operating voltage range : 2.4 V to 5.5 V
- Power-down mode (Battery save) available
- Compact package : SSOP10 (10 pin, 0.65 mm pitch)



SSOP10-P-0.65

Weight : 0.04 g (Typ.)
Abbreviated marked on product :B14

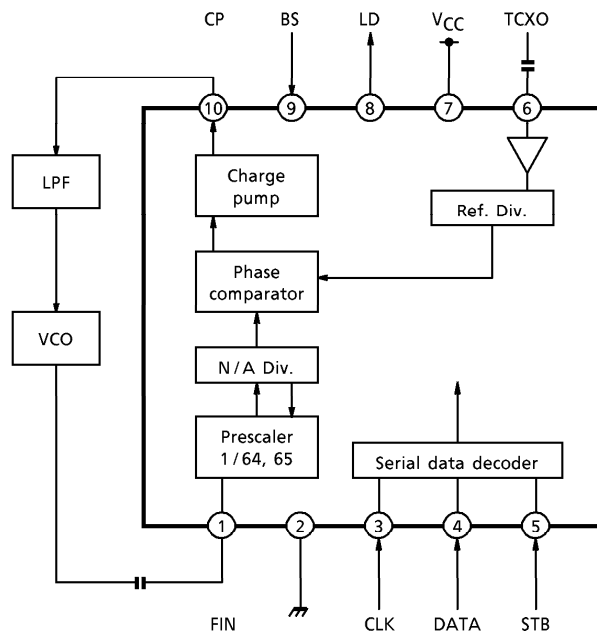
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BLOCK DIAGRAM



Handle with care to prevent devices from deterioration by static electricity.

PIN FUNCTION (All resistance and capacitance values in the table below are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT (around pins)
1	FIN	Prescaler input terminal. Inputs frequency from VCO.	
2	GND	Ground terminal	—
3	CLK	Clock input terminal	
4	DATA	Data input terminal	
5	STB	Strobe input terminal	
9	BS	Battery save terminal	
6	XIN	Reference oscillator input terminal	
7	VCC	Supply voltage terminal	—
8	LD	Lock detect output terminal. Open drain output. Locked : Open Unlocked : Low Power down : Open	
10	CP	Charge pump output terminal. Constant current output.	

- Lock detection

When the phase difference (time converted) is within one count of the TCXO, the lock detect output timer starts. After seven counts of phase comparing, LD output becomes high (lock signal). When the phase difference (time converted) exceeds one count of the TCXO, LD output becomes low (unlock signal).

- Power down mode

TB31245FN can be switched between power down mode and operating status by SB bit. This status is as listed in the table below include a relation of external battery save terminal and this IC.

External pin	Serial data	Operating mode
BS	SB	PLL
L	*	OFF
H	0	OFF
H	1	ON

ON : In operation, OFF : Power down (No operation)
External battery save terminal H = High, L = Low

(5) Reference divider data

- Reference divider is fixed to 1 / 64.
- Reference frequency (phase comparing frequency) is 300 kHz. (at reference signal (XO input) is 19.2 MHz)

DESCRIPTION OF FUNCTIONS AND OPERATION

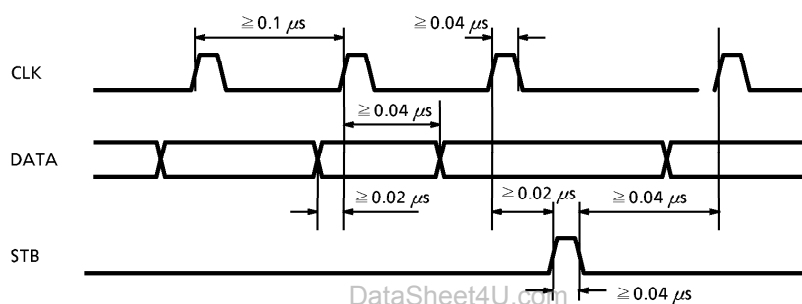
(1) Serial data input

TB31245FN operates according to the serial data program. Serial data is input from the clock terminal (CLK), data terminal (DATA), and strobe terminal (STB).

(2) Entry of serial data

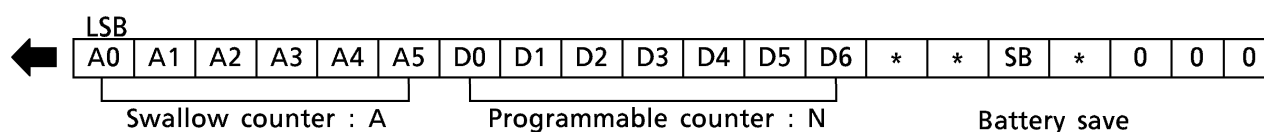
- At the rising edge of the clock pulse, data is sent to the internal shift register from the LSB sequentially. When all the data is sent, set the strobe terminal to high. At this rising edge, data is stored in latches depending on the control contents. At the same time as data is stored, control starts. Phase comparing starts with the falling edge of the strobe terminal. The clock, data, and strobe terminal contain the Schmitt trigger circuit to prevent the data errors by noise, etc.

(3) Serial data input timing



(4) Programmable divider data

- Consist of a 6-bit swallow counter (programmable counter), an 7-bit programmable counter, a 1/64, 1/65 two modulus prescaler.
- By sending any data to the swallow counter and programmable counter, number of division can be set from 4032 to 8191.



$$\text{Number of division} = 64N + A$$

$$A = A_0 + A_1 \times 2^1 + \dots + A_5 \times 2^5$$

$$N = D_0 + D_1 \times 2^1 + \dots + D_6 \times 2^6$$

$$4032 \leq \text{number of division} \leq 8191$$

A : Value of A counter (remainder)

N : Value of N counter (quotient)

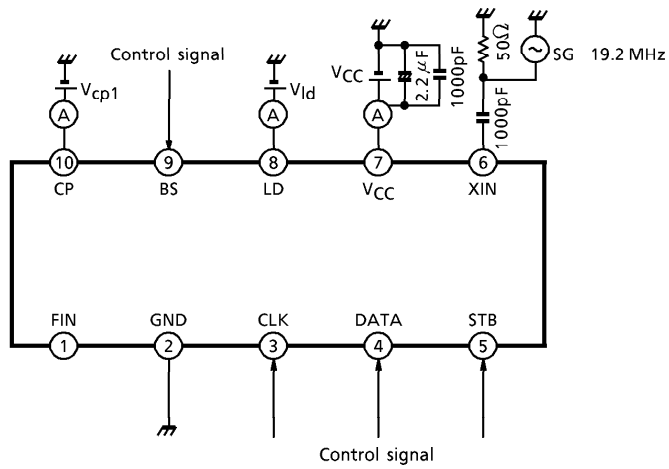
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power supply voltage	V _{CC}	6.0	V
Power dissipation	P _D	240	mW
Input terminal voltage	V _{IN}	-0.5~6.0	V
Operating temperature range	T _{opr}	-40~85	°C
Storage temperature range	T _{stg}	-55~150	°C

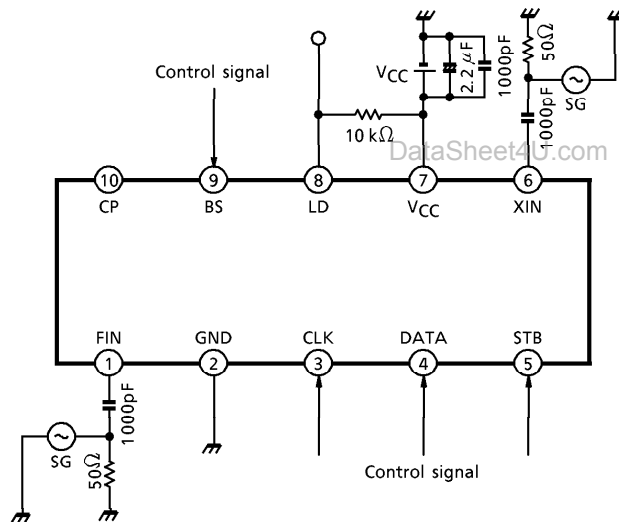
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, V_{CC} = 3.0 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIRC UIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating power supply voltage	V _{CC}	—	—	2.4	3.0	5.5	V
Current consumption at operation	I _{cco}	1	All circuits in operation	—	4.8	6.5	mA
Current consumption at BS	I _{ccq}	1	Power down mode	—	0	10	μA
Operating frequency	F _{IN}	2	V _{FIN} = 97dBμV	1610.5	—	1699.5	MHz
FIN input level	V _{FIN}	2	F _{IN} = 1610.5~1699.5 MHz	92	—	107	dBμV
Reference operating frequency	X _{IN}	2	V _{XIN} = 97~112dBμV	—	19.2	—	MHz
Reference input level	V _{XIN}	2	X _{IN} = 19.2 MHz	97	—	112	dBμV
CLK input frequency	F _{CLK}	—	—	0.1	0.5	10	MHz
Charge pump output current	I _{CP}	1	V _{CP} = 1/2V _{CC}	1.2	1.8	2.4	mA
Charge pump output off leak	I _{CP (OFF)}	1	V _{CP} = 0~V _{CC}	-0.1	0	0.1	μA
"H" level input voltage	V _{IH}	—	BS, CLK, DATA, STB	0.8 × V _{CC}	V _{CC}	5.5	V
"L" level input voltage	V _{IL}	—	BS, CLK, DATA, STB	-0.2	0	0.2 × V _{CC}	V
LD terminal off leak	I _{LD}	1	V _{LD} = 5.5 V	-1	0	1	μA
LD terminal on resistance	R _{LD}	1	V _{LD} = 0.4 V	800	1100	2000	Ω

TEST CIRCUIT DIAGRAM 1



TEST CIRCUIT DIAGRAM 2



Notes : ← and → in the circuits indicate control signals.

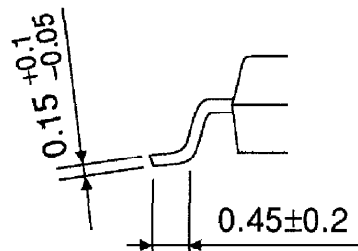
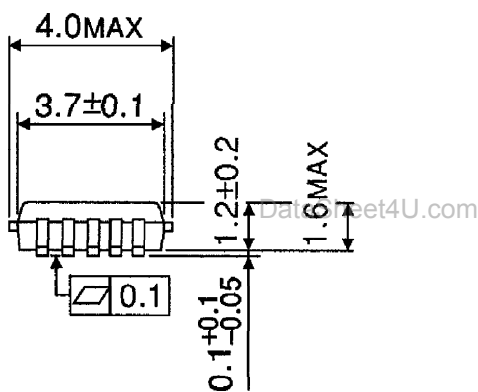
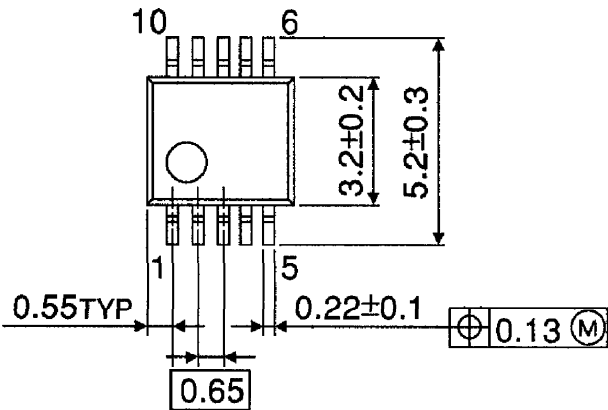
○ indicates a test pin.

In test circuit diagram 1, unless measuring the current consumption, pin 6 is open.

PACKAGE DIMENSIONS

SSOP10-P-0.65

Unit : mm



Weight : 0.04 g (Typ.)