TOSHIBA BiCD Process Integrated Circuit - Silicon Monolithic

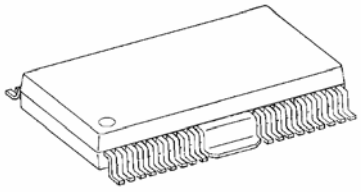
TB62207BF･TB62207BFG

Stepping Motor Driver/DC Motor Driver Select, DC-DC Converter and Reset Driven by Chopper Microstep Pseudo Sine Wave

The TB62207BF/BFG is a dual stepping motor driver./DC motor driver switching enabled, DC-DC converter and reset driven by chopper microstep pseudo sine wave.

To drive a two-phase bipolar-type stepping motor, a 16-bit latch and a 16-bit shift register are built in the IC. The IC is suitable for driving stepping motors with low-torque ripple in a highly efficient manner. In addition, a signal axis can be switched to serve as a PWM driver for two DC motors.

By equipping the stepping motor driver with Selectable Mixed Decay Mode for switching the attenuation ratio during chopping and also equipping it with a DC/DC converter, it is possible for the IC to supply external voltage.



HSOP36-P-450-0.65

Weight: 0.79 g (typ.)

Features

●The following motor combinations can be used (see p. 16-20 for pin locations)

	Stepper	DC Large DC (L)	DC Small DC (S)
1	dual axis	---	---
2	single axis	single axis	---
3	single axis	---	dual axis
4	---	single axis	dual axis
5	---	dual axis	---

Note: Hereafter, DC Large will be referenced as DC (L) and DC Small will be referenced as DC (S).

● Output Current：Stepping Motor 1.0A (MAX) (single axis drive)

DC Motor	DC Large	DC Small
Varistor peak	8A (500ns)	4A (500ns)
For initial torque	3A (100ms)	2.5A (100ms)
Stationary current	0.8A	0.8A

The large current standard is achieved by shorting a small current H-Bridge outside two ICs. In addition, if the thermal setting is designed to be within the proscribed thermal range, the initial torque current can be used as the normal operating current.

● It is possible to supply voltage to the outside by internalizing a step-down 1.5V to 5.0V variable DC-DC converter.

● A Reset function has been added making it possible to output a reset signal to the outside.

●Monolithic BiCD IC whose motor driver output DMOS is capable of achieving a low ON resistance of Ron = 0.6Ω (@Tj = 25℃, 0.6A: Typ.)

●Two sets of internal serial input type 16 bit shift registers and 16 bit latches.

●The motor driver is capable of driving stepping motors using a 4-bit microstep.

● Equipped protection circuits: DC-DC converter overcurrent/increased voltage protection, motor overcurrent protection and total IC overtemperature protection.

In addition, equipped with Power On Reset circuit for initializing the IC when the power is turned on and off.

● Package: 36-pin power flat package (HSOP36-P-450-0.65)

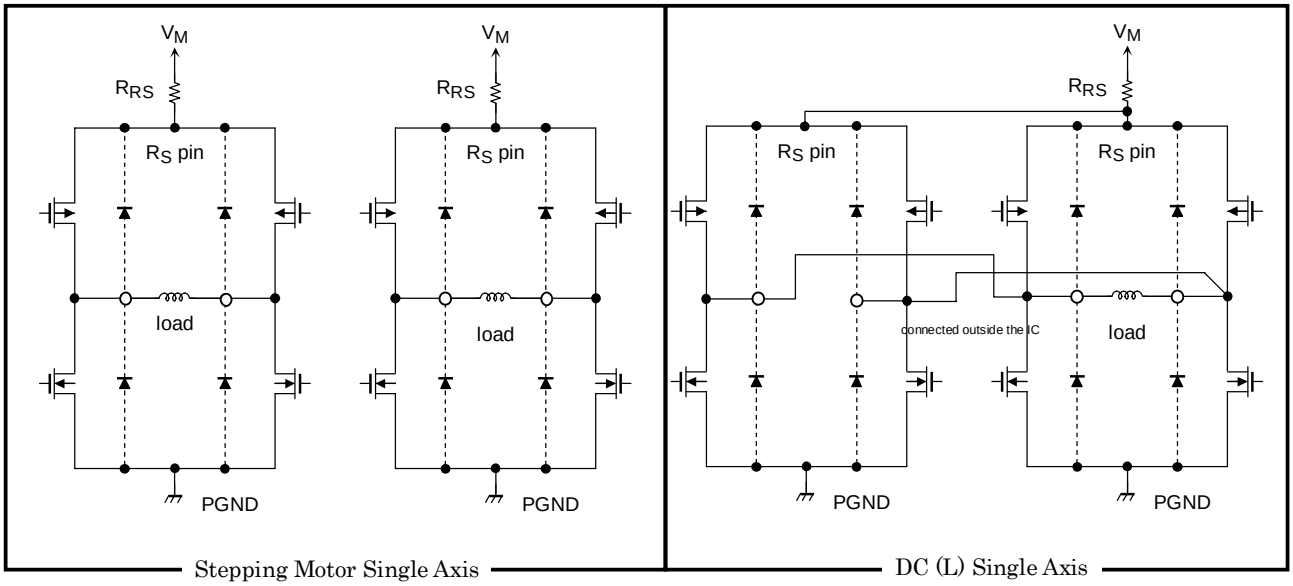
● Motor maximum output pressure: 37 V

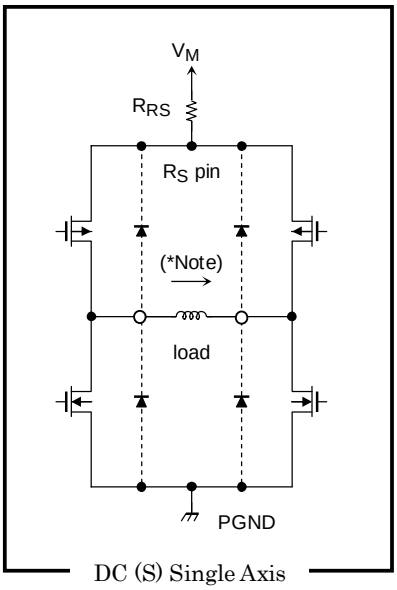
●On-chip Mixed Decay Mode enables specification of four-stage attenuation ratio.

●Chopping frequency can be set by external oscillator. High-speed chopping is possible at 100 kHz or higher.

Note: When using the IC, be very careful in regard to thermal conditions.

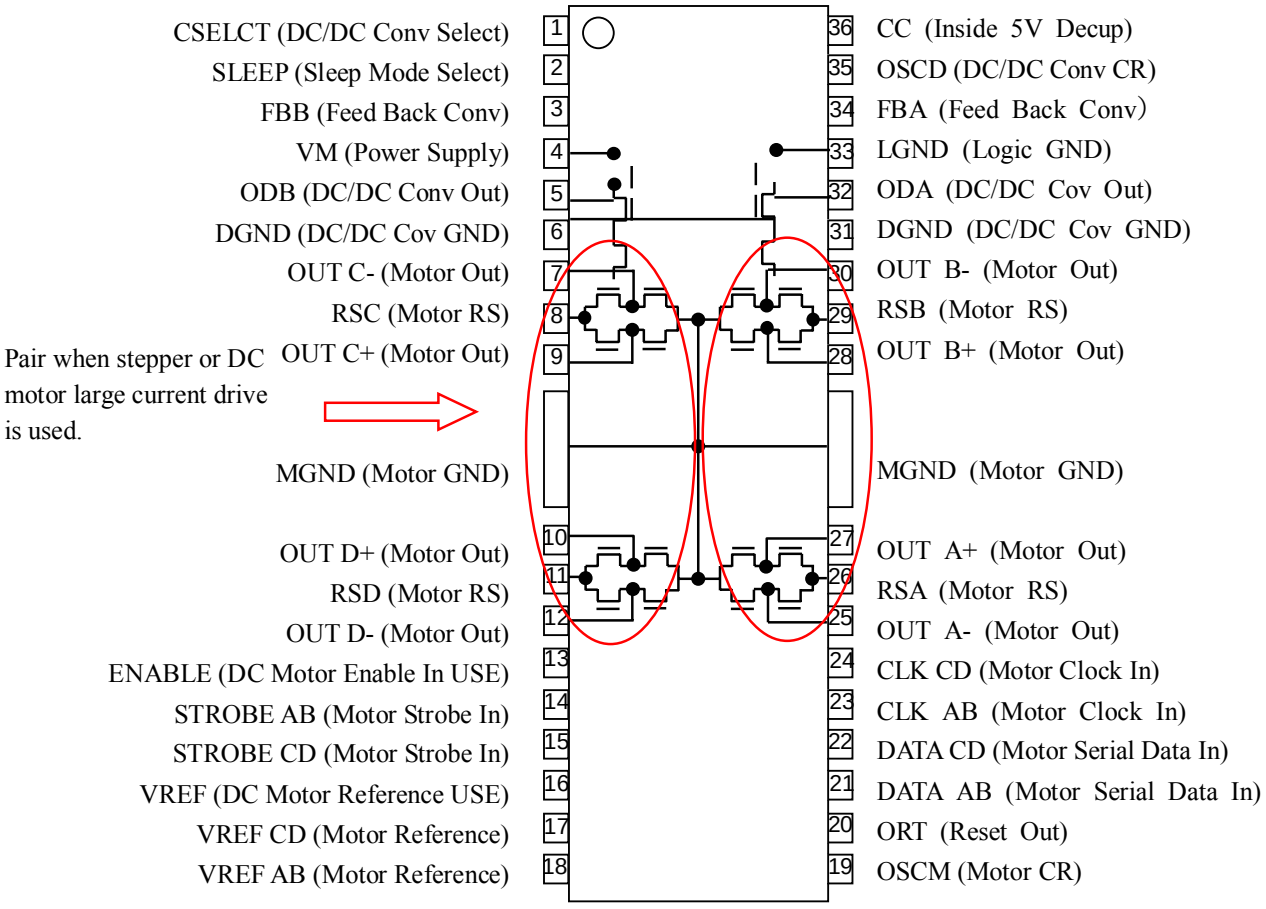
■ H-Bridge Combination (Connection Method) for Each Type of Motor Driver





○ : The white circle indicates an IC pin.

■**Pin Layout (Dual Axis Stepper Example)**



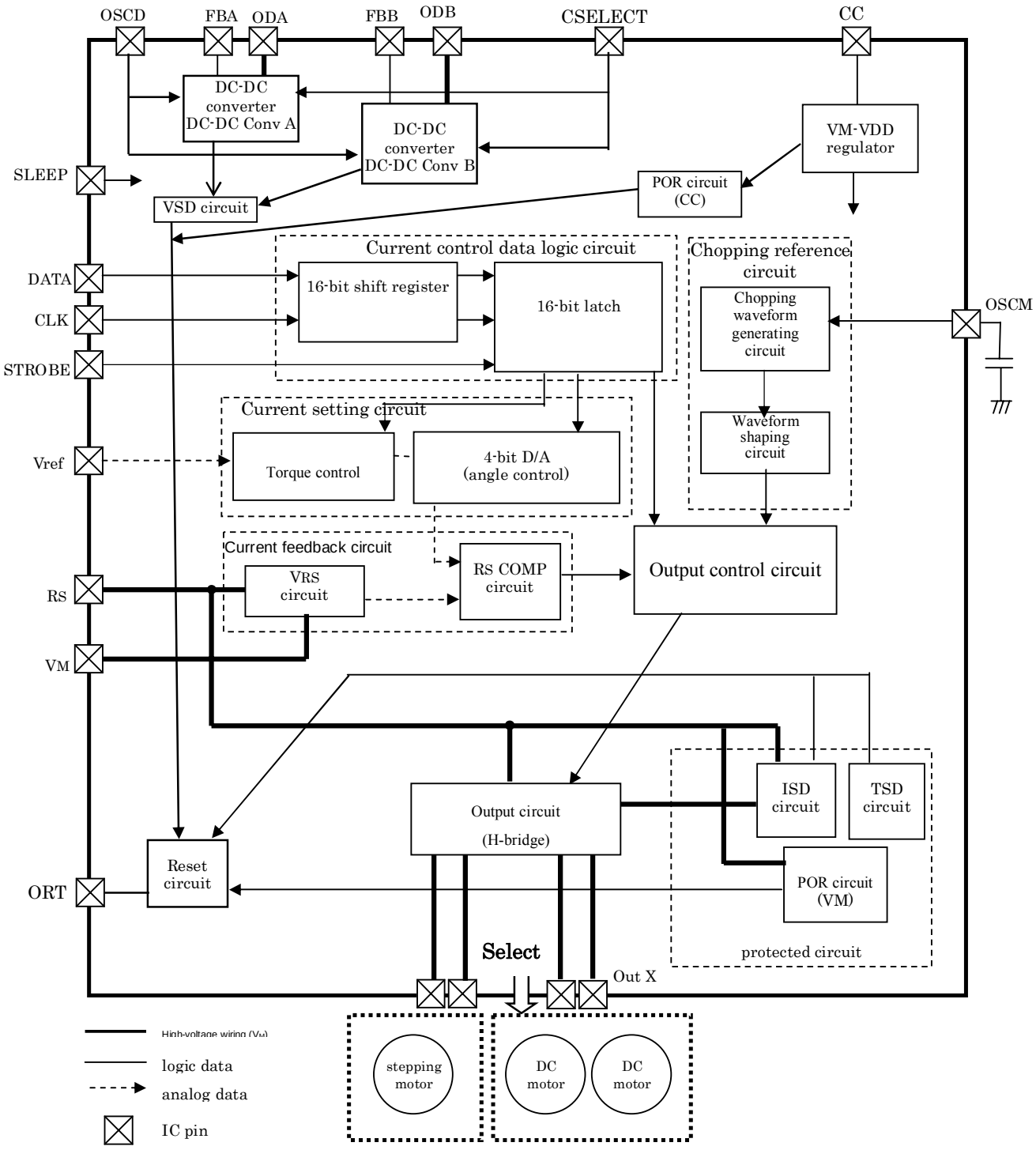
Notes

- **Connect any unused Vref pins to GND.**
- **Unused data, clock or strobe input pins are pulled down internally, so connect to Open or GND. However, please make considerations so that noise will not get mixed into the printed circuit board.**
- **Connect any unused RS pins to VM.**
- **This device dose not incorporates an over-voltage protection circuit. Thus, if an excess voltage is applied to the IC, the IC may be destroyed. Please design the IC so that an excess voltage will not be applied to the IC.**

- **When the IC is mounted in the wrong orientation, high voltage will be applied to the low-withstand-voltage block, which causes the IC to be destroyed. Please check the pin 1 positioning mark when mounting it. While the IC is powered-on, do not connect the motor to the IC or vice-versa.**

Block Diagram

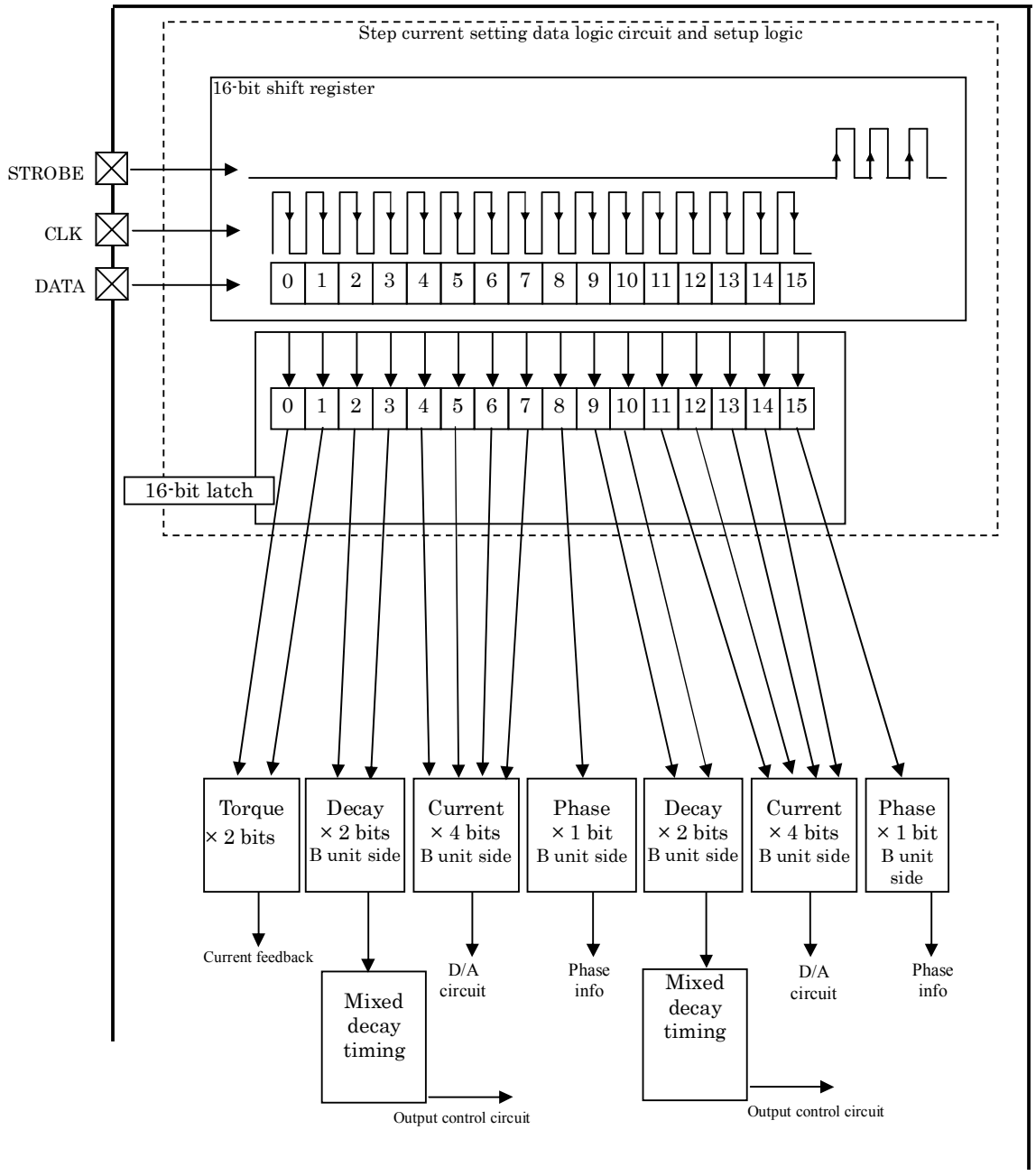
1. Overview



2. Logic unit for motor driver

Function

This circuit is used to input step current settting data from the DATA pins and then to transfer that data to the subsequent stage.



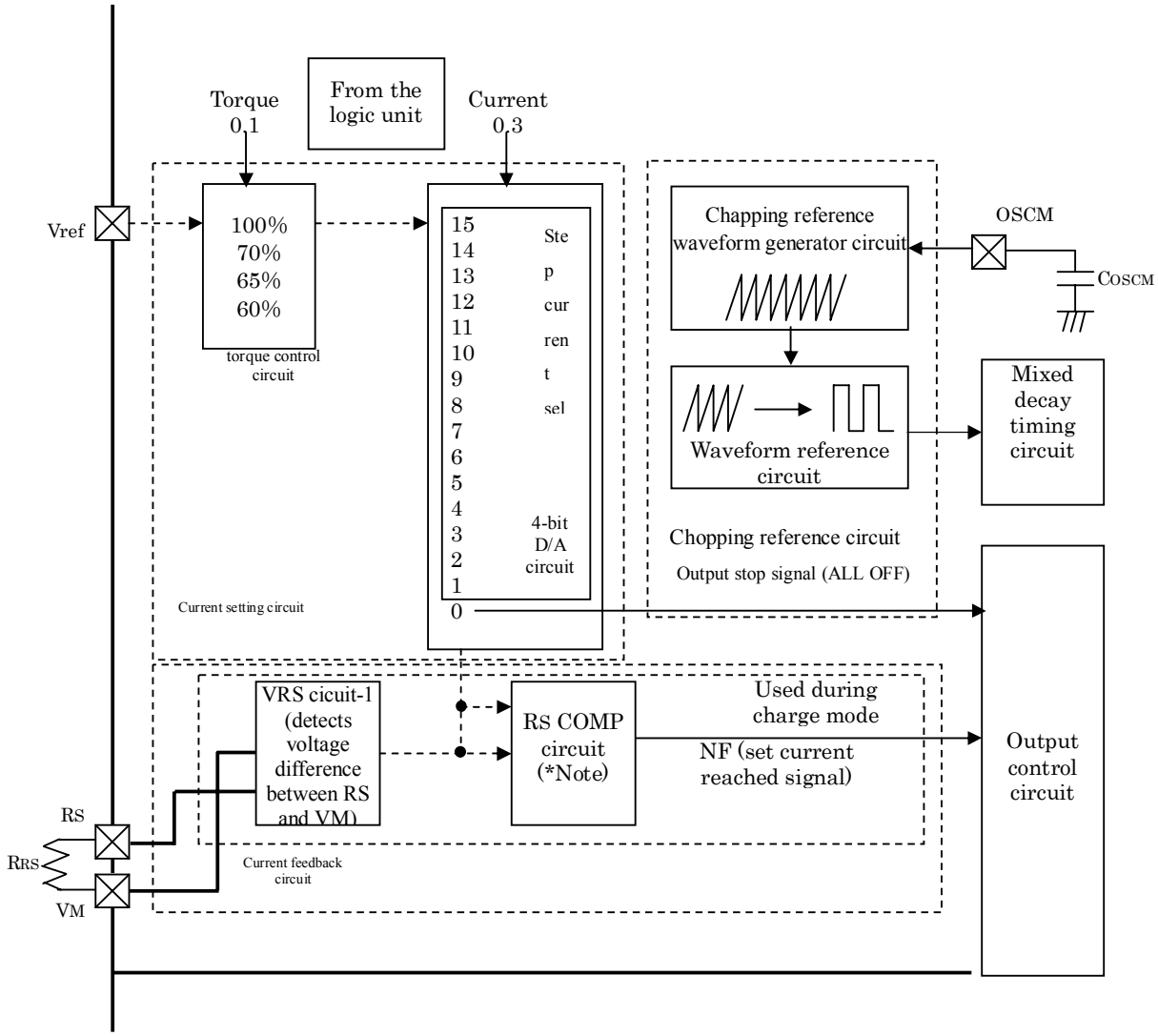
3. Current feedback circuit and current setting circuit for motor driver

Function

The current setting circuit is used to set the reference voltage of the output current using the step current setting data input from the DATA pins.

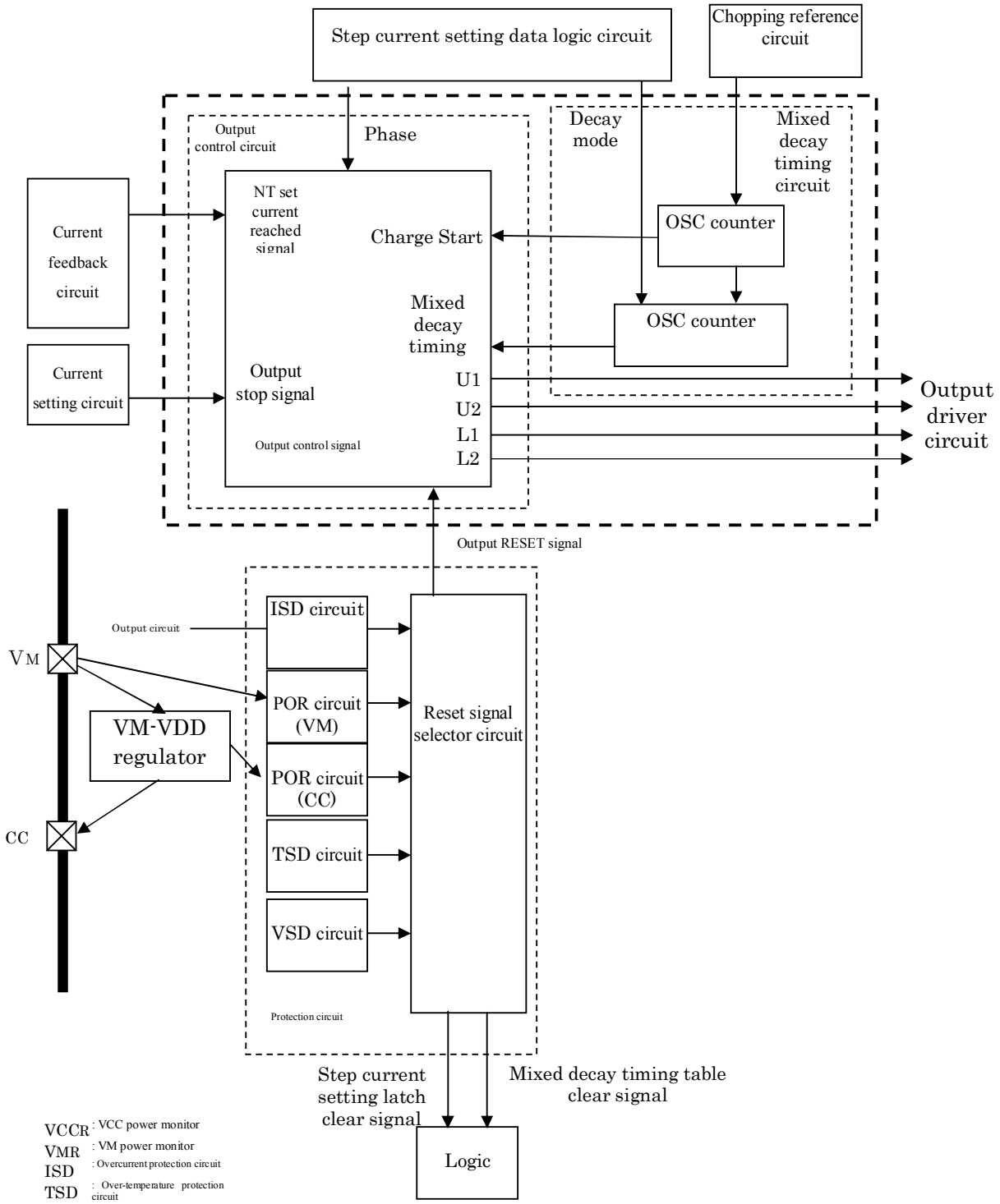
The current feedback circuit is used to output to the output control circuit the relation between the set current value and output current. This is done by comparing the reference voltage output to the current setting circuit with the potential difference generated when current flows through the current sense resistor (RRS) connected between RS and VM.

The chopping waveform generator, to which a capacitor is connected, creates the OSCM (OSC-CLK) which is used as the reference for chopping frequency.

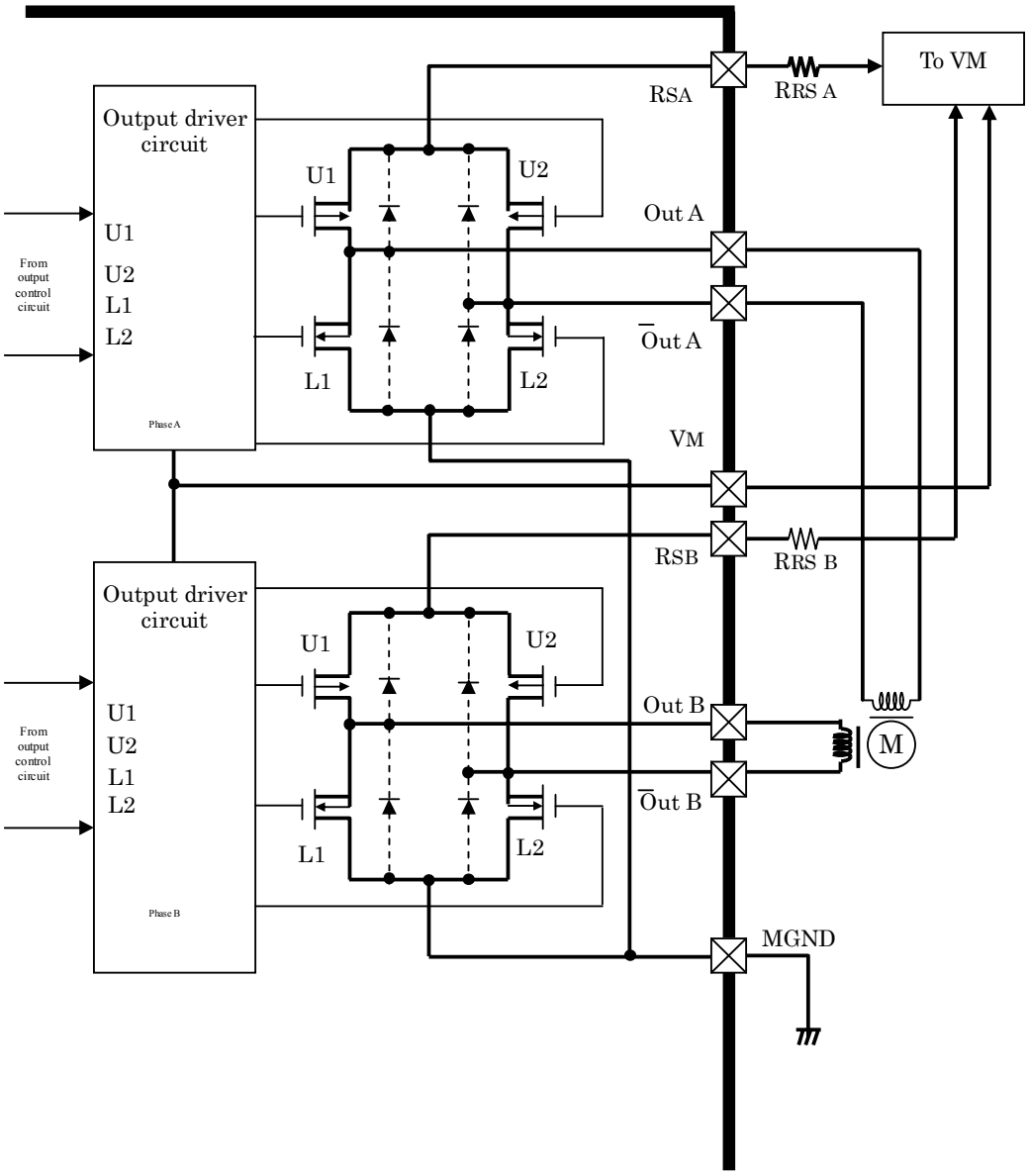


(*Note): RE COMP: Compares the set current with the output current and outputs a signal when the output current reaches the set current.

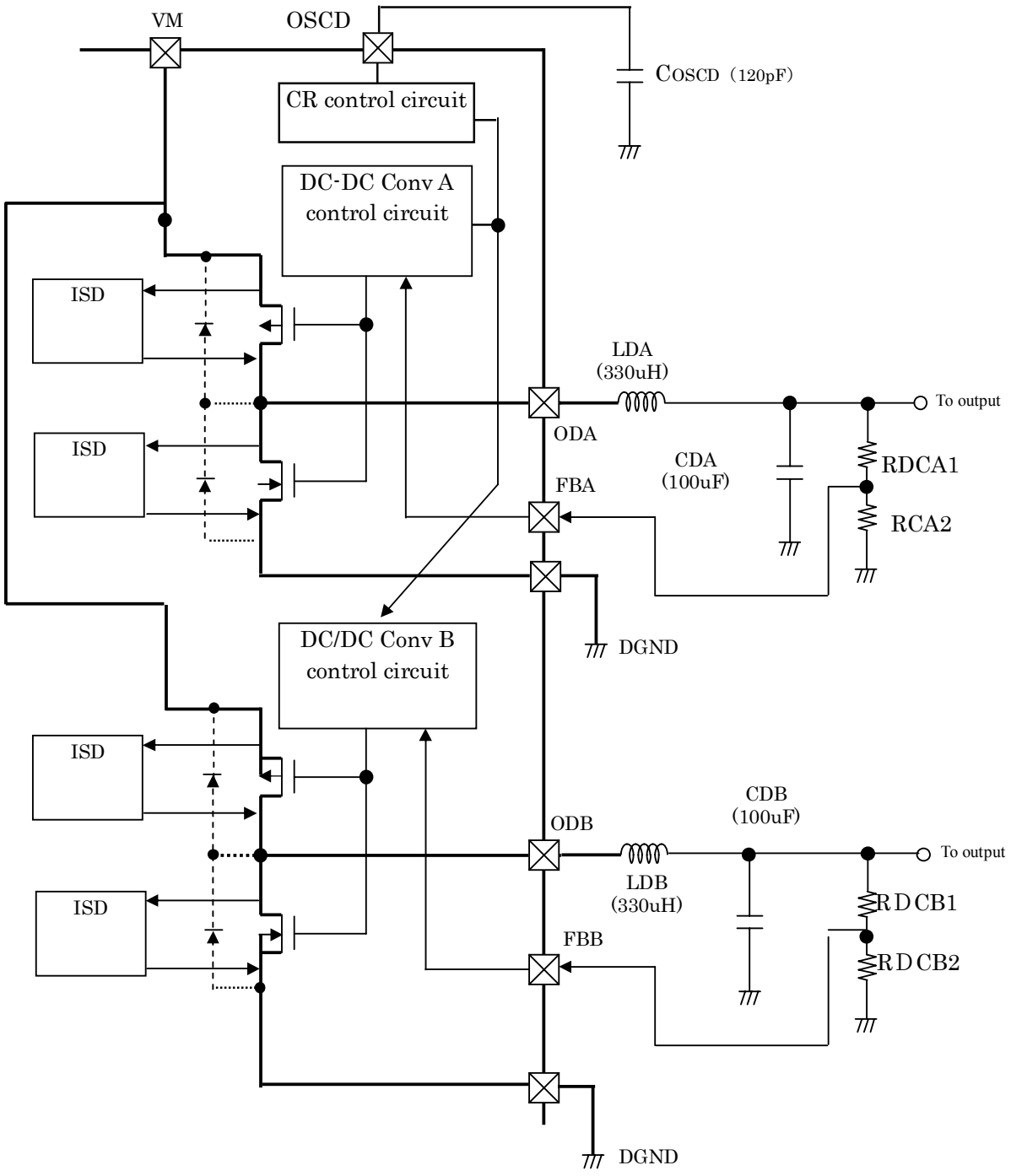
4. Output control circuit, current feedback circuit and current setting circuit for motor driver



5. Output equivalent circuit for motor driver



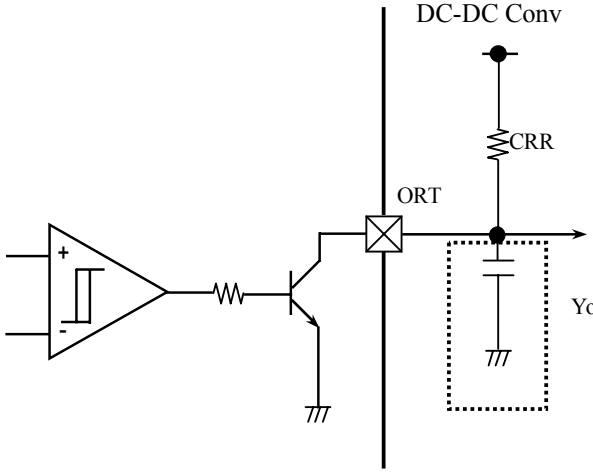
6. DC-DC converter circuit



FB recommended resistance

	RDCA1/RDCB1	RDCA2/RDCB2
3.3 V setting	1.2k	1k
5.0 V setting	5.6k	2.4k

7. Reset circuit

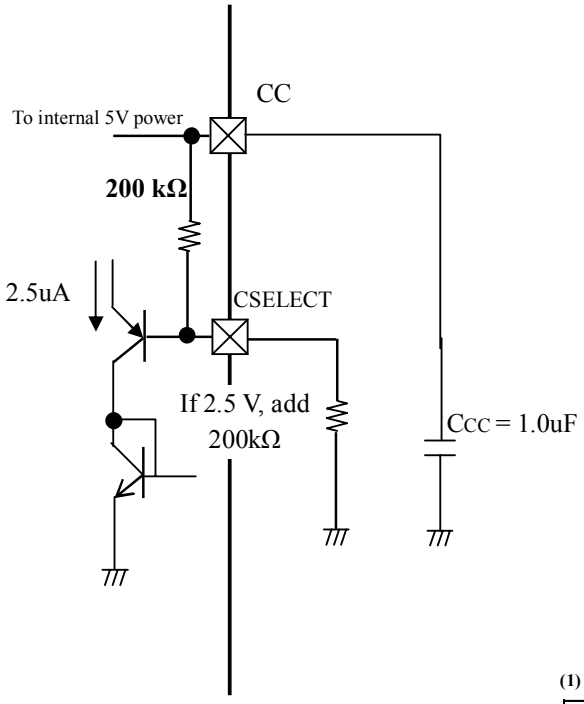


You can load capacity for delay.

Note: When the RESET pin's pullup is used not for CC pin but for DC-DC output, the OSCD's oscillation will stop and the DC-DC will go off prior to the IC's own POR, resulting in the external Reset going low prior to POR. Therefore, after AC goes OFF, if the AC goes ON during the interval between OSCD_OFF and POR then the Reset delay won't take effect. An external Reset IC is required in order to avoid this problem.

8. DC-DC converter select circuit

■



CSELECT	Serial Default Setting Data		ODA Out	ODB Out
VCSELECT	DC/DC A SW (Data bit:7)	DC/DC B SW (Data bit:8)	DC/DC A	DC/DC B
GND	0	0	ON	ON
	0	1	ON	OFF
	1	0	OFF	OFF
	1	1	OFF	OFF
2.5V	0	0	ON	OFF
	0	1	ON	OFF
	1	0	OFF	OFF
	1	1	OFF	OFF
OPEN	0	0	OFF	OFF
	0	1	OFF	OFF
	1	0	OFF	OFF
	1	1	OFF	OFF

The Reset Signal

• When using DC-DC B

The signal can be output and the proscribed amount of time can be delayed by rising DC-DC B

• When not using DC-DC B

The signal can be output and the proscribed amount of time can be delayed by rising DC-DC A

(see page 31)

(1) If the feedback pin is fixed to the following voltage from the time power is turned on

	FBA/FBB Voltage			
	0V～0.1V	0.1V～1.05V	1.05V～2.25V	2.25V～5.0V
Output logic (ODA/ODB)	"H"(=VM)	OFF	normal operation	OFF
DC/DC converter state	normal operation	shutdown	normal operation	shutdown

(2) If the feedback pin is fixed to the following voltage during normal operations

	FBA/FBB Voltage		
	0V～1.05V	1.05V～2.25V	2.25V～5.0V
Output logic (ODA/ODB)	OFF	normal operation	OFF
DC/DC converter state	shutdown	normal operation	shutdown

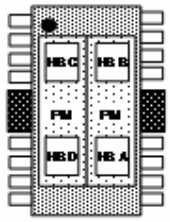
Note A: FBA/FBB pin voltage ranging from 1.05 to 2.25 volts is the normal operation state in which the FB comparative voltage is not input into the 1.5 V increase/decrease voltage (-30%/+40%).

Note B: In the above state, the FB pin only operates in the channel fixed to the listed voltage. A channel and B channel are independent.

■ **Pin Descriptions (Initial Setting Mode)**
Overwrite mode in which SLEEP = "L"

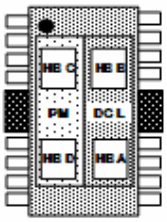
Pin No.	Initial Mote Setting	
1	_	_
2	SLEEP	Sleep mode pin (initial mode overwrite software)
3	_	_
4	VM	main power
5	_	_
6	_	_
7	_	_
8	_	_
9	_	_
10	_	_
11	_	_
12	_	_
13	_	_
14	STROBE AB	initial data latch signal
15	_	_
16	_	_
17	_	_
18	_	_
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	DATA AB	initial data input pin
22	_	_
23	CLK AB	initial data clock pin
24	_	_
25	_	_
26	_	_
27	_	_
28	_	_
29	_	_
30	_	_
31	DGND	DC-DC Conv GND
32	_	_
33	LGND	Logic GND
34	_	_
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

(1) Pin Descriptions (Stepper x 2-axis Mode)

Pin No.	Stepper x 2 	
1	CSELECT	DC-DC conv selector
2	SLEEP	Sleep mode pin
3	FBB	Bch DC-DC feedback pin
4	VM	main power
5	ODB	Bch DC-DC output pin
6	DGND	DC-DC conv GND
7	OUT C-	PM drive output (C-phase -)
8	RS C	C-phase PM current comparative resistance pin
9	OUT C+	PM drive output (C-phase +)
10	OUT D+	PM drive output (D-phase +)
11	RS D	D-phase PM motor current comparative resistance pin
12	OUT D-	PM drive output (D-phase -)
13	_	_
14	STROBE AB	AB phase strobe signal input pin
15	STROBE CD	CD phase strobe signal input pin
16	_	_
17	VREF CD	CD phase motor reference potential input pin
18	VREF AB	AB phase motor reference potential input pin
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	DATA AB	AB phase data input pin
22	DATA CD	CD phase data input/Phase single input pin
23	CLK AB	AB phase clock input pin
24	CLK CD	CD phase clock input pin
25	OUT A-	PM drive output (A-phase -)
26	RS A	A-phase PM current comparative resistance pin
27	OUT A+	PM drive output (A-phase +)
28	OUT B+	PM drive output (B-phase +)
29	RS B	B-phase PM current comparative resistance pin
30	OUT B-	PM drive output (B-phase -)
31	DGND	DC-DC Conv GND
32	ODA	A-channel DC-DC converter output pin

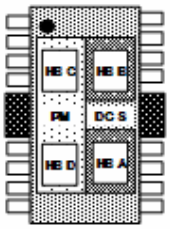
33	LGND	Logic GND
34	FBA	A-channel DC-DC converter feedback pin
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

(2) Pin Descriptions (Stepper x 1-axis and DC (L) x 1-axis Mode)

Pin No.	Stepper x 1, DC (L) x 1 	
1	CSELECT	DC-DC conv selector
2	SLEEP	Sleep mode pin
3	FBB	Bch DC-DC feedback pin
4	VM	main power
5	ODB	Bch DC-DC output pin
6	DGND	DC-DC conv GND
7	OUT LB-	DC motor drive output (-)
8	RS LB	DC motor current comparative resistance pin (short with 11-pin and add resistance between this pin and VM)
9	OUT LB+	DC motor drive output (+)
10	OUT LB-	DC motor drive output (-)
11	RS LB	DC motor current comparative resistance pin (short with 8-pin)
12	OUT LB+	DC motor drive output (+)
13	_	_
14	STROBE AB	AB phase strobe signal input pin
15	ENABLE AB	ENABLE input pin for a DC motor
16	_	_
17	VREF LB	DC motor reference potential input pin
18	VREF AB	AB phase motor reference potential input pin
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	DATA AB	AB phase data input pin
22	PHASE LB	PHASE input pin for a DC motor
23	CLK AB	AB phase clock input pin
24	_	_
25	OUT A-	PM drive output (A-phase -)
26	RS A	A-phase PM current comparative resistance pin
27	OUT A+	PM drive output (A-phase +)
28	OUT B+	PM drive output (B-phase +)
29	RS B	B-phase PM current comparative resistance pin
30	OUT B-	PM drive output (B-phase -)
31	DGND	DC-DC Conv GND
32	ODA	A-channel DC-DC converter output pin

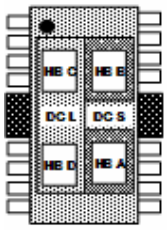
33	LGND	Logic GND
34	FBA	A-channel DC-DC converter feedback pin
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

(3) Pin Descriptions (Stepper x 1-axis and DC (S) x 2-axis Mode)

Pin No.	Stepper x 1, DC (S) x 2 	
1	CSELECT	DC-DC conv selector
2	SLEEP	Sleep mode pin
3	FBB	Bch DC-DC feedback pin
4	VM	main power
5	ODB	Bch DC-DC output pin
6	DGND	DC-DC conv GND
7	OUT SA-	A-channel DC motor drive output (-)
8	RS SA	A-channel DC motor current comparative resistance pin
9	OUT SA+	A-channel DC motor drive output (+)
10	OUT SB-	B-channel DC motor drive output (-)
11	RS DC-SB	B-channel DC motor current comparative resistance pin
12	OUT SB+	B-channel DC motor drive output (+)
13	ENABLE SB	B-channel DC motor enable input pin
14	STROBE AB	AB phase strobe signal input pin
15	ENABLE SA	A-channel DC motor enable input pin
16	VREF SB	B-channel DC motor reference potential input pin
17	VREF SA	A-channel DC motor reference potential input pin
18	VREF AB	AB phase motor reference potential input pin
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	DATA AB	AB phase data input pin for a PM
22	PHASE A	A-channel DC motor phase input pin
23	CLK AB	AB phase clock input pin
24	PHASE B	B-channel DC motor phase input pin
25	OUT A-	PM drive output (A-phase -)
26	RS A	A-phase PM current comparative resistance pin
27	OUT A+	PM drive output (A-phase +)
28	OUT B+	PM drive output (B-phase +)
29	RS B	B-phase PM current comparative resistance pin
30	OUT B-	PM drive output (B-phase -)
31	DGND	DC-DC Conv GND
32	ODA	A-channel DC-DC converter output pin

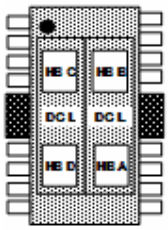
33	LGND	Logic GND
34	FBA	A-channel DC-DC converter feedback pin
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

(4) Pin Descriptions (DC (S) x 2-axis and DC (L) x 1-axis Mode)

Pin No.	DC (S) x 2, DC (L) x 1 	
1	CSELECT	DC-DC conv selector
2	SLEEP	Sleep mode pin
3	FBB	Bch DC-DC feedback pin
4	VM	main power
5	ODB	Bch DC-DC output pin
6	DGND	DC-DC conv GND
7	OUT SA-	Small A-channel DC motor drive output (-)
8	RS SA	Small A-channel DC motor current comparative resistance pin
9	OUT SA+	Small A-channel DC motor drive output (+)
10	OUT SB-	Small B-channel DC motor drive output (-)
11	RS SB	Small B-channel DC motor current comparative resistance pin
12	OUT SB+	Small B-channel DC motor drive output (+)
13	ENABLE SB	Small B-channel DC motor enable input pin
14	ENABLE LA	Large A-channel DC motor enable input pin
15	ENABLE SA	Small A-channel DC motor enable input pin
16	VREF SB	Small B-channel DC motor reference potential input pin
17	VREF SA	Small A-channel DC motor reference potential input pin
18	VREF LA	Large A-channel DC motor reference potential input pin
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	_	_
22	PHASE SA	Small A-channel DC motor phase input pin
23	PHASE LA	Large A-channel DC motor phase input pin
24	PHASE SB	Small B-channel DC motor phase input pin
25	OUT LA-	Large A-channel DC motor drive output (-)
26	RS LA	Large A-channel DC motor current comparative resistance pin(short with 29-pin and add resistance between this pin and VM)
27	OUT LA+	Large A-channel DC motor drive output (+)
28	OUT LA-	Large A-channel DC motor drive output (-)
29	RS LA	Large A-channel DC motor current comparative resistance pin(short with 26-pin)
30	OUT LA+	Large A-channel DC motor drive output (+)
31	DGND	DC-DC Conv GND

32	ODA	A-channel DC-DC converter output pin
33	LGND	Logic GND
34	FBA	A-channel DC-DC converter feedback pin
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

(5) Pin Descriptions (DC (L) x 2-axis Mode)

Pin No.	DC (L) x 2 	
1	CSELECT	DC-DC conv selector
2	SLEEP	Sleep mode pin
3	FBB	Bch DC-DC feedback pin
4	VM	main power
5	ODB	Bch DC-DC output pin
6	DGND	DC-DC conv GND
7	OUT LB-	Large B-channel DC motor drive output (-)
8	RS LB	Large B-channel DC motor current comparative resistance pin
9	OUT LB+	Large B-channel DC motor drive output (+)
10	OUT LB-	Large B-channel DC motor drive output (-)
11	RS LB	Large B-channel DC motor current comparative resistance pin
12	OUT LB+	Large B-channel DC motor drive output (+)
13	_	_
14	ENABLE LA	Large A-channel DC motor enable input pin
15	ENABLE LB	Large B-channel DC motor enable input pin
16	_	_
17	VREF LB	Large B-channel DC motor reference potential input pin
18	VREF LA	Large A-channel DC motor reference potential input pin
19	OSCM	motor reference clock generating external capacity pin (68pF typ)
20	ORT	Reset signal output pin
21	_	_
22	PHASE LB	Large B-channel DC motor phase input pin
23	PHASE LA	Large A-channel DC motor phase input pin
24	_	_
25	OUT LA-	Large A-channel DC motor drive output (-)
26	RS LA	Large A-channel DC motor current comparative resistance pin(short with 29-pin and add resistance between this pin and VM)
27	OUT LA+	Large A-channel DC motor drive output (+)
28	OUT LA-	Large A-channel DC motor drive output (-)
29	RS LA	Large A-channel DC motor current comparative resistance pin(short with 26-pin)
30	OUT LA+	Large A-channel DC motor drive output (+)
31	DGND	DC-DC Conv GND

32	ODA	A-channel DC-DC converter output pin
33	LGND	Logic GND
34	FBA	A-channel DC-DC converter feedback pin
35	OSCD	DC-DC converter oscillation capacity connection pin (120 pF typ)
36	CC	internal 5V coupling capacity connection pin (1 uF typ)
Fin	MGND	motor GND
Fin	MGND	motor GND

■ 16-bit serial input signals

(1) Initial mode select (only write during sleep during mode setting register)

Data Bit	Name	Function	Settings	Default
0	Motor Select0	Motor pairing setting (Note 1)	D2 D1 D0 0 0 0 : Stepper×2 0 0 1 : Stepper×1+DCL×1 0 1 0 : Stepper×1+DCS×2 0 1 1 : DCL×1+DCS×2 1 0 0 : DCL×2	0
1	Motor Select1			0
2	Motor Select2			0
3	TBlank A0	Noise rejection dead band time setting (Note 2)	D4 D3 D6 D5 0 0 : 1÷ƒChop÷8×0 0 1 : 1÷ƒChop÷8×0 1 0 : 1÷ƒChop÷8×0 1 1 : 1÷ƒChop÷8×0 **(Note 3)**	0 0
4	TBlank A1			
5	TBlank B0			
6	TBlank B1			
7	DC/DC A SW	DC-DC converter A-operation	0 : ON 1 : OFF	0
8	DC/DC B SW	DC-DC converter B-operation	0 : ON 1 : OFF	0
9	DC1 Motor VGain	Internal Vref attenuation ratio setting	0 : 1/10 1 : 1/20(DC) 1/10(Stepper)	0
10	DC2 Motor Vgain	Internal Vref attenuation ratio setting	0 : 1/10 1 : 1/20(DC) 1/10(Stepper)	0
11	DC3 Motor Vgain	Internal Vref attenuation ratio setting	0 : 1/10 1 : 1/20(DC) 1/10(Stepper)	0
12	Test			
13	Test			
14	Test			
15	Test			

Note 1: Please refer to the separate document regarding maximum large current in regard to motor pairing.

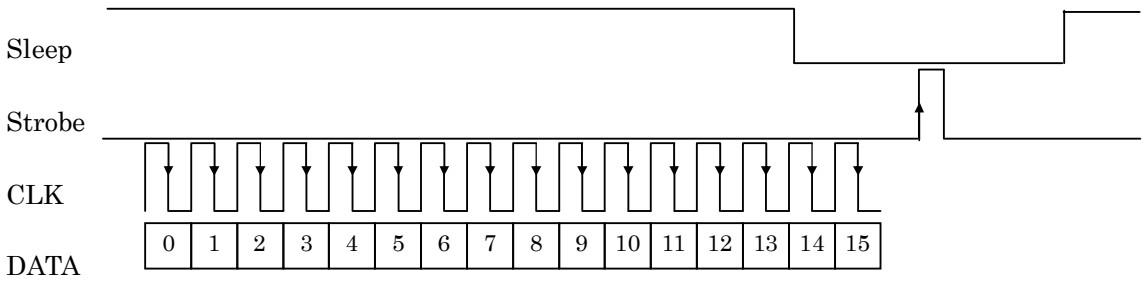
Note 2: The "noise rejection dead band time (TBlank) defined by the motor's AC characteristic, is a fixed time held internally, and is used mainly to prevent misjudgment between large recovery current during stepping motor drive operations and varistor charge/discharge current during DC motor drive operations. The above defined TBlank is the dead band time generated digitally via the chopping period. When the stepper is selected using the motor select, TBlank is set to "0 0" and is only the TBlank time (300 ns typ.) held internally is valid.

TBlank: TBlank from the register: time, TBlank: internal analog mask time

Note 3: At this Ver, tBLANK XX becomes 0 0 : 1÷ƒChop÷8×0 with any values.

(2) Normal (during normal operations)

Data Bit	Name	Function	Settings
0	Torque A0/B0	Current range setting	A1/B1 A0/B0 0 0 : 60% 0 1 : 65% 1 0 : 70% 1 1 : 100%
1	Torque A1/B1		
2	Decay Mode B0	Bch current attenuation ratio setting	B1 B0 0 0 : Slow Decay Mode 0 1 : 37.5% Decay Mode 1 0 : 75% Decay Mode 1 1 : Fast Decay Mode
3	Decay Mode B1		
4	Current B0	Bch current setting ("0000" all output OFF mode) 4-bit current data (depending on the 4-bit data, it is possible to divide the steps into 16ths)	Refer to setting chart (2)
5	Current B1		
6	Current B2		
7	Current B3		
8	Phase B	phase information	1 : OUT B+ 0 : OUT B-
9	Decay Mode A0	Ach current attenuation ratio setting	A1 A0 0 0 : Slow Decay Mode 0 1 : 37.5% Decay Mode 1 0 : 75% Decay Mode 1 1 : Fast Decay Mode
10	Decay Mode A1		
11	Current A0	Ach current setting ("0000" all output OFF mode) 4-bit current data (depending on the 4-bit data, it is possible to divide the steps into 16ths)	Refer to setting chart (2)
12	Current A1		
13	Current A2		
14	Current A3		
15	Phase A	phase information	1 : OUT A+ 0 : OUT A-



Use sleep logic and strobe edge to select the initial register or normal register for the overwrite register.
During Strobe ↑, Sleep = L: initial register, Sleep = H: normal register
During data transfer the sleep level doesn't matter.
In addition, the normal motor register can be initialized by Sleep = L. Also, POR will initialize all registers.Please input Strobe signal 3 pulse.
The pins used for overwrite during Sleep are:
No.3, the DATA AB pin, No. 5, the CLOCK AB pin, and No. 32, the STROBE AB pin. Even if the DC motor is selected, once it goes to sleep, the above pin mode will go in effect.

■**Table for Setting (1) D0, D1**

Torque setting

Data Bit	Name	Function	Torque 1	Torque 0	Setting Torque (Typ.)
0 1	Torque0 Torque1	Sets current range	0	0	60%
			0	1	65%
			1	0	70%
			1	1	100%

■**Table for Settings (2) D2, D3**

Decay Mode setting

Data Bit	Name	Function	Decay Mode 1	Decay Mode 0	Setting Decay Mode
2 3	Decay Mode A1/B1 Decay Mode A0/B0	Sets decay mode	0	0	Slow Decay Mode
			0	1	Mixed Decay Mode : 37.5%
			1	0	Mixed Decay Mode : 75%
			1	1	Fast Decay Mode

■ **Table for Settings (2) D4, D5, D6, D7**

Current setting

Data Bit	Step	B3	B2	B1	B0	Setting angle (degree)	Current (%)
4 5 6 7	16	1	1	1	1	90	100
	15	1	1	1	1	84	100
	14	1	1	1	0	79	98
	13	1	1	0	1	73	96
	12	1	1	0	0	68	92
	11	1	0	1	1	61	88
	10	1	0	1	0	56	83
	9	1	0	0	1	51	77
	8	1	0	0	0	45	71
	7	0	1	1	1	39	63
	6	0	1	1	0	34	56
	5	0	1	0	1	28	47
	4	0	1	0	0	23	38
	3	0	0	1	1	17	29
	2	0	0	1	0	11	20
	1	0	0	0	1	6	10
	0	0	0	0	0	0	0

■ **Table for Settings (2) D11, D12, D13, D14**
Current setting

Data Bit	Step	A3	A2	A1	A0	Setting angle (degree)	Current (%)
11 12 13 14	16	1	1	1	1	90	100
	15	1	1	1	1	84	100
	14	1	1	1	0	79	98
	13	1	1	0	1	73	96
	12	1	1	0	0	68	92
	11	1	0	1	1	61	88
	10	1	0	1	0	56	83
	9	1	0	0	1	51	77
	8	1	0	0	0	45	71
	7	0	1	1	1	39	63
	6	0	1	1	0	34	56
	5	0	1	0	1	28	47
	4	0	1	0	0	23	38
	3	0	0	1	1	17	29
	2	0	0	1	0	11	20
	1	0	0	0	1	6	10
	0	0	0	0	0	0	0

■ **Table for Setting (1) D8, D15**
Phase A setting

Data Bit	Name	Function	Phase	Setting Phase
8 15	Phase A Phase B	switches phase	0	OUT A **L**、OUT A- **H**
			1	OUT A **H**、OUT A- **L**

TB62207 has the internal test circuit for the factory test to shorten test time.
When the pin conditions satisfy the status in following table, TB62207 automatically enters test mode.

Pin conditions for test mode

PIN NUMBER	2	15	22	24
STATUS	Low	High	High	High

In this mode both protection mask time and ORT output time are set 1/1024 of normal mode.
Therefore, in order to keep TB62207 in normal operation, please avoid these pin conditions and pay special attention, when TB62207 starts up. Because the outputs of DC- DC converter are unstable.

■Protection operations

Error Detection Content and Detection Block						Operating State			Reset output	Reset Method
DC-DC A		DC-DC B		Motor	Entire IC	DC-DC A	DC-DC B	Motor		
overcurrent	increase/decrease voltage	overcurrent	increase/decrease voltage	overcurrent	overtemperature					
not detected	not detected	not detected	not detected	not detected	not detected	normal	normal	normal	H	---
detected	not detected	not detected	not detected	not detected	not detected	shut down	shut down	shut down	L	POR
not detected	**detected**	not detected	not detected	not detected	not detected	shut down	shut down	shut down	L	POR
not detected	not detected	**detected**	not detected	not detected	not detected	shut down	shut down	shut down	L	POR
not detected	not detected	not detected	**detected**	not detected	not detected	shut down	shut down	shut down	L	POR
not detected	not detected	not detected	not detected	**detected**	not detected	normal	normal	OFF	L pulse	SLEEP/POR
not detected	not detected	not detected	not detected	not detected	**detected**	shut down	shut down	shut down	L	POR

Notes:

Shut down = functions are ceased and can only be reset by initializing using POR.

OFF = Only the corresponding block stops to function. Reset can be performed by initializing the SLEEP from H to L

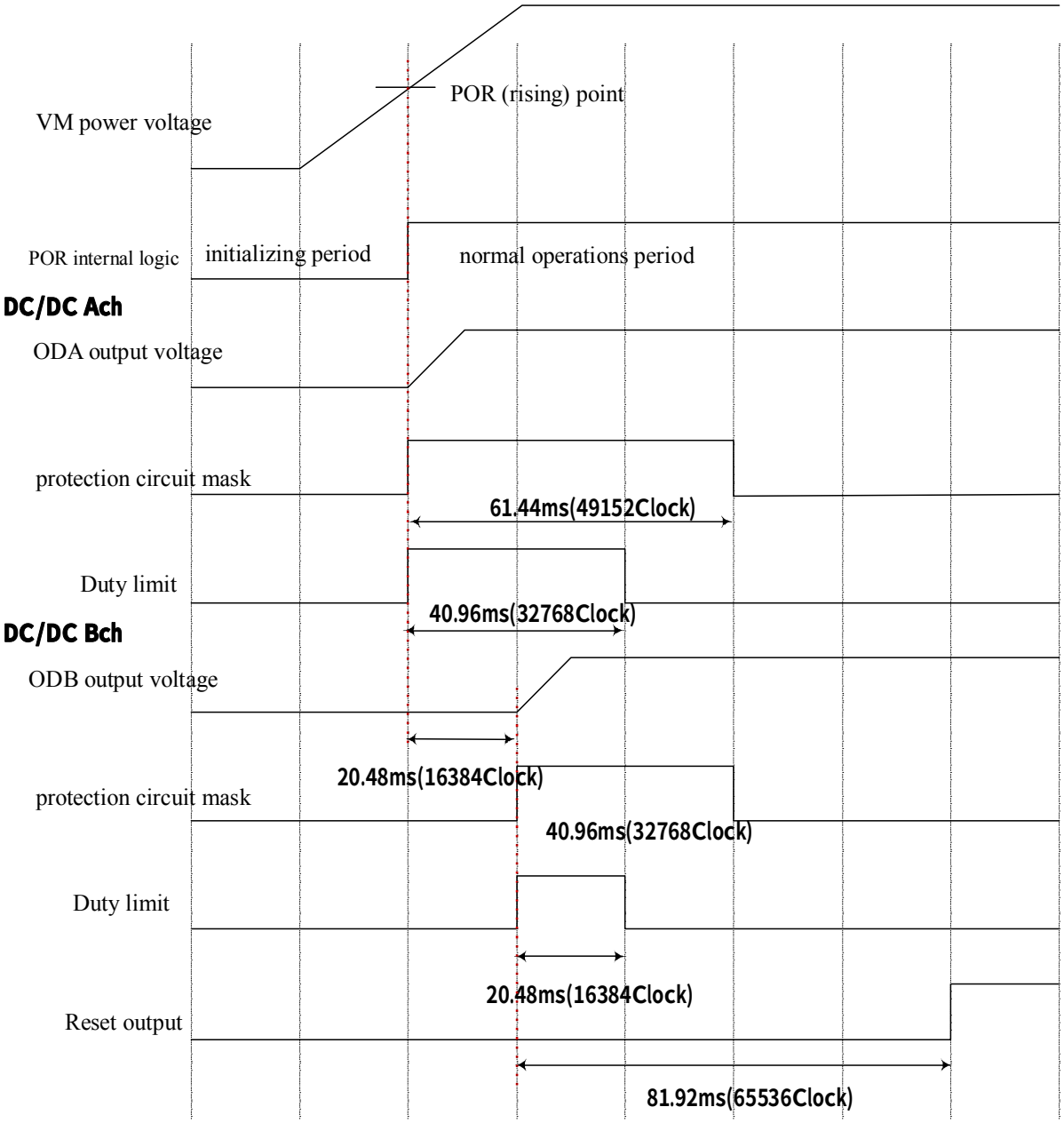
L pulse = 40ms (if reference frequency is 800kHz = 32768 clock)

■Protection Mask Period (Example: Reference Clock 800 kHz)

Protection Function	Detection Block	Protection Mask Width	Example: time when OSCM = 800 KHz	Reset Method
overtemperature protection	entire IC	16 to 20 clock	20 us	POR
overcurrent	DC-DC converter	16 to 20 clock	20 us	POR
	motor	4 to 8 clock	5 to 8 us	SLEEP/POR
increase/decrease voltage	DC-DC converter	16 to 20 clock	20 us	POR

■**Operation when DC-DC Converter Power Goes On**

(1) When both channels go on when DC-DC converter power goes on

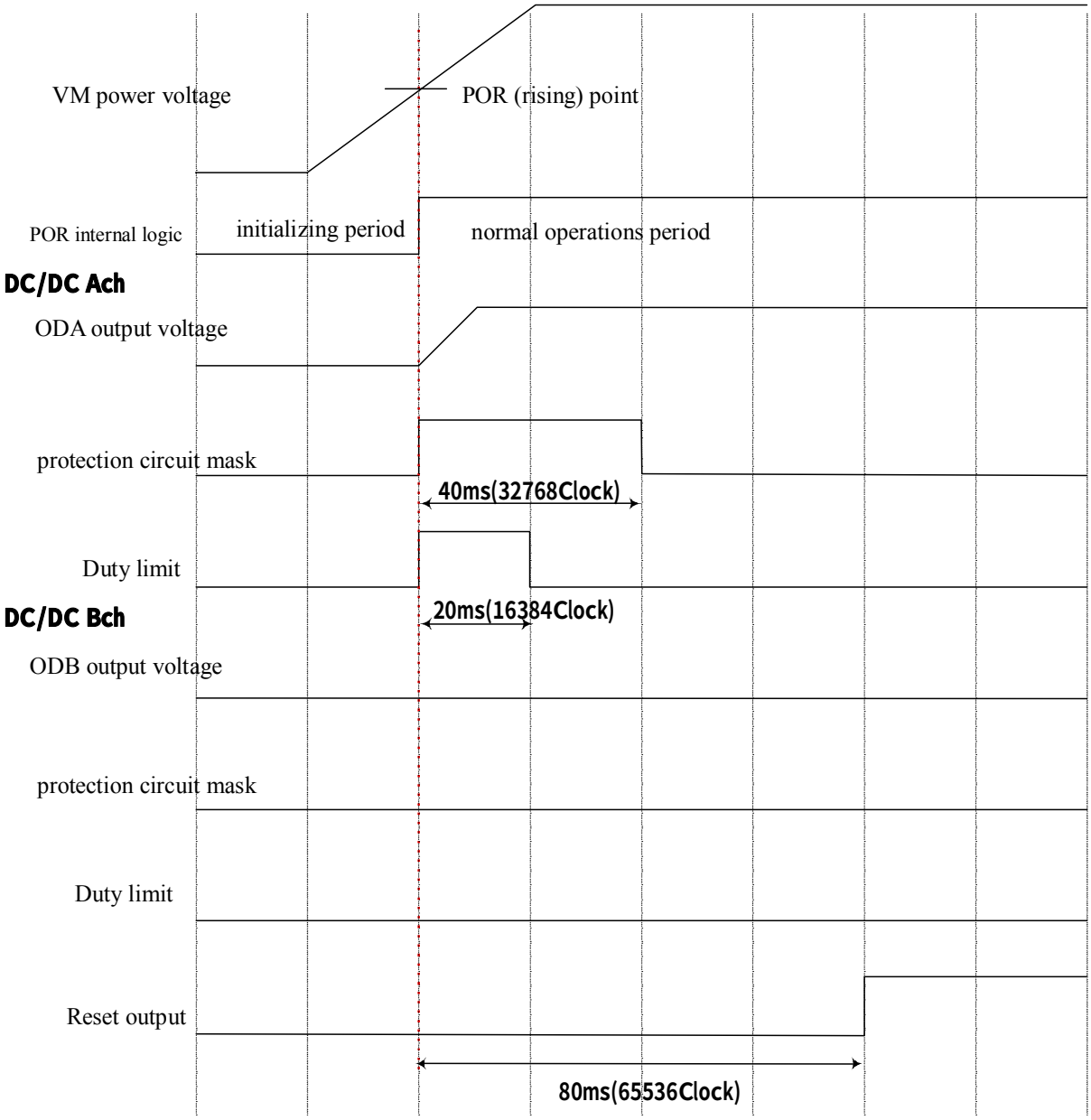


Notes: The above times are all predicated on f_{OSCDM}= 800kHZ and 1 CR_CLK = 1.25 us.

Duty limit is a function that limits the duty between 70 to 100% during the corresponding time frame.

Protection mask period is a period during which error detection is not performed.

(2) When only A-channel go on when DC-DC converter power goes on

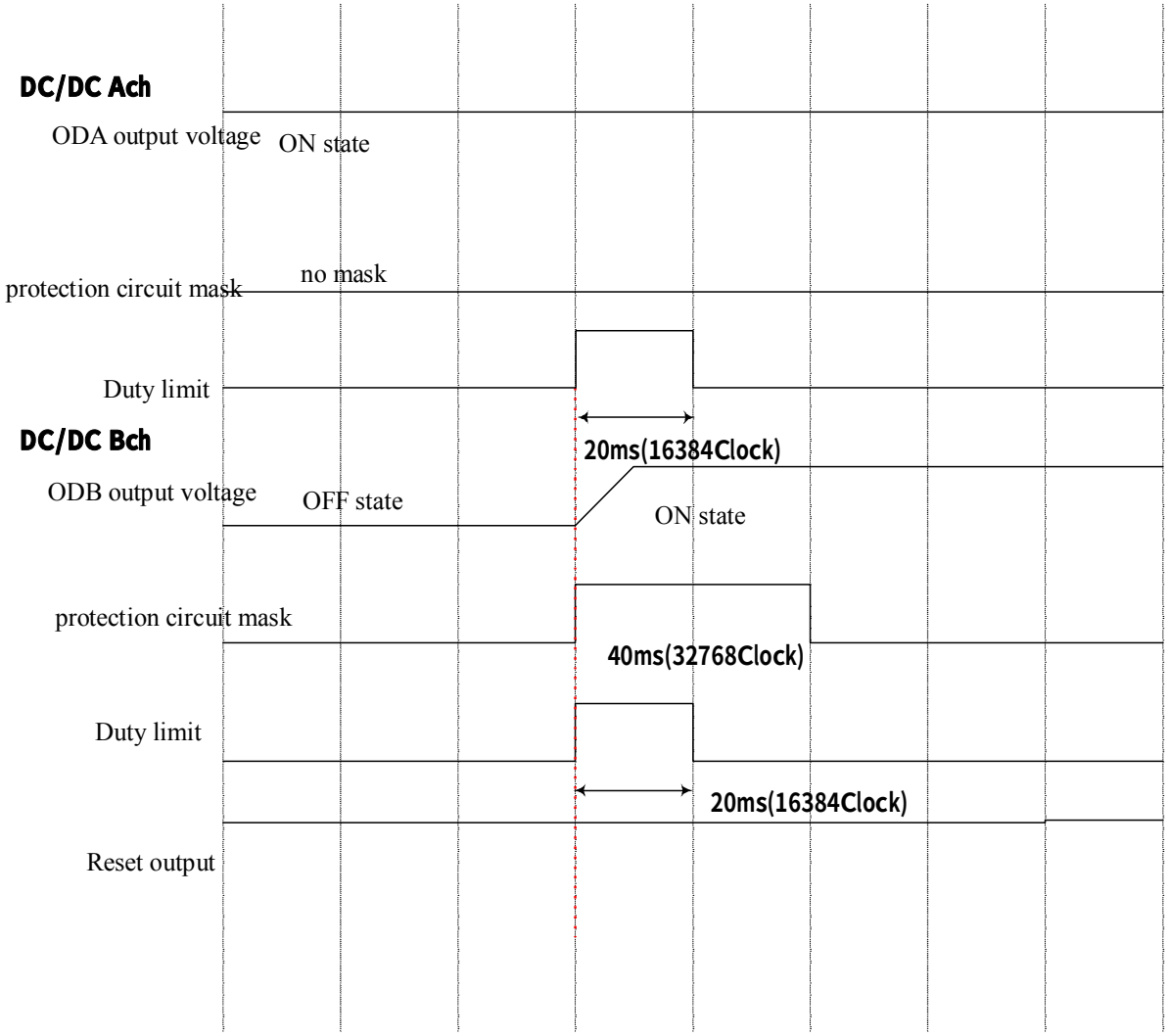


Notes: The above times are all predicated on f_{OSCDM}= 800kHZ and 1 CR_CLK = 1.25 us.

Duty limit is a function that limits the duty between 70 to 100% during the corresponding time frame.

Protection mask period is a period during which error detection is not performed.

(3) When DC-DC converter B-channel dynamically go on

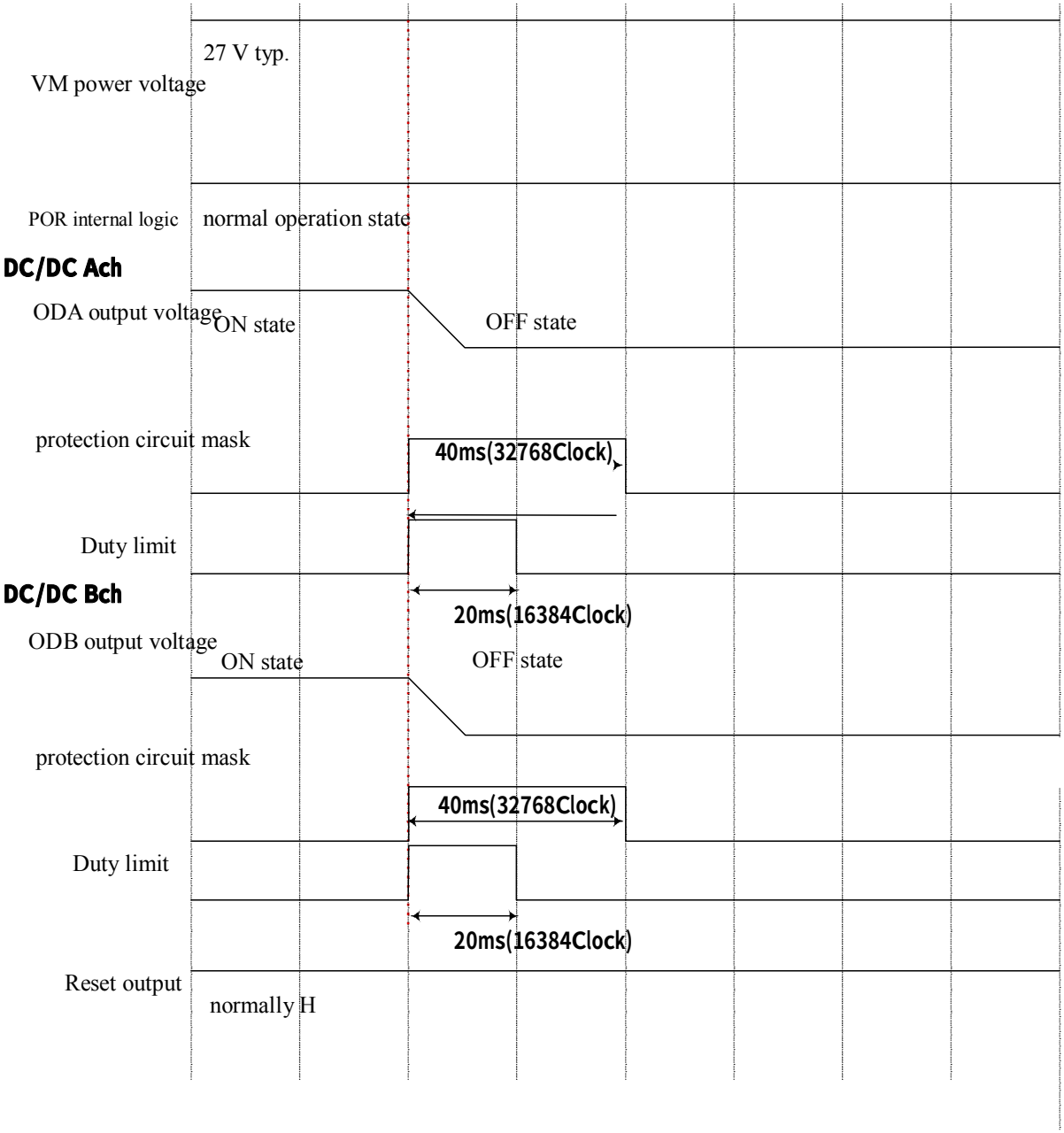


Notes: The above times are all predicated on f_{OSCDM}= 800kHZ and 1 CR_CLK = 1.25 us.

Duty limit is a function that limits the duty between 70 to 100% during the corresponding time frame.

Protection mask period is a period during which error detection is not performed.

(4) When both DC-DC converter channels dynamically go off after VM rise (after POR reset)

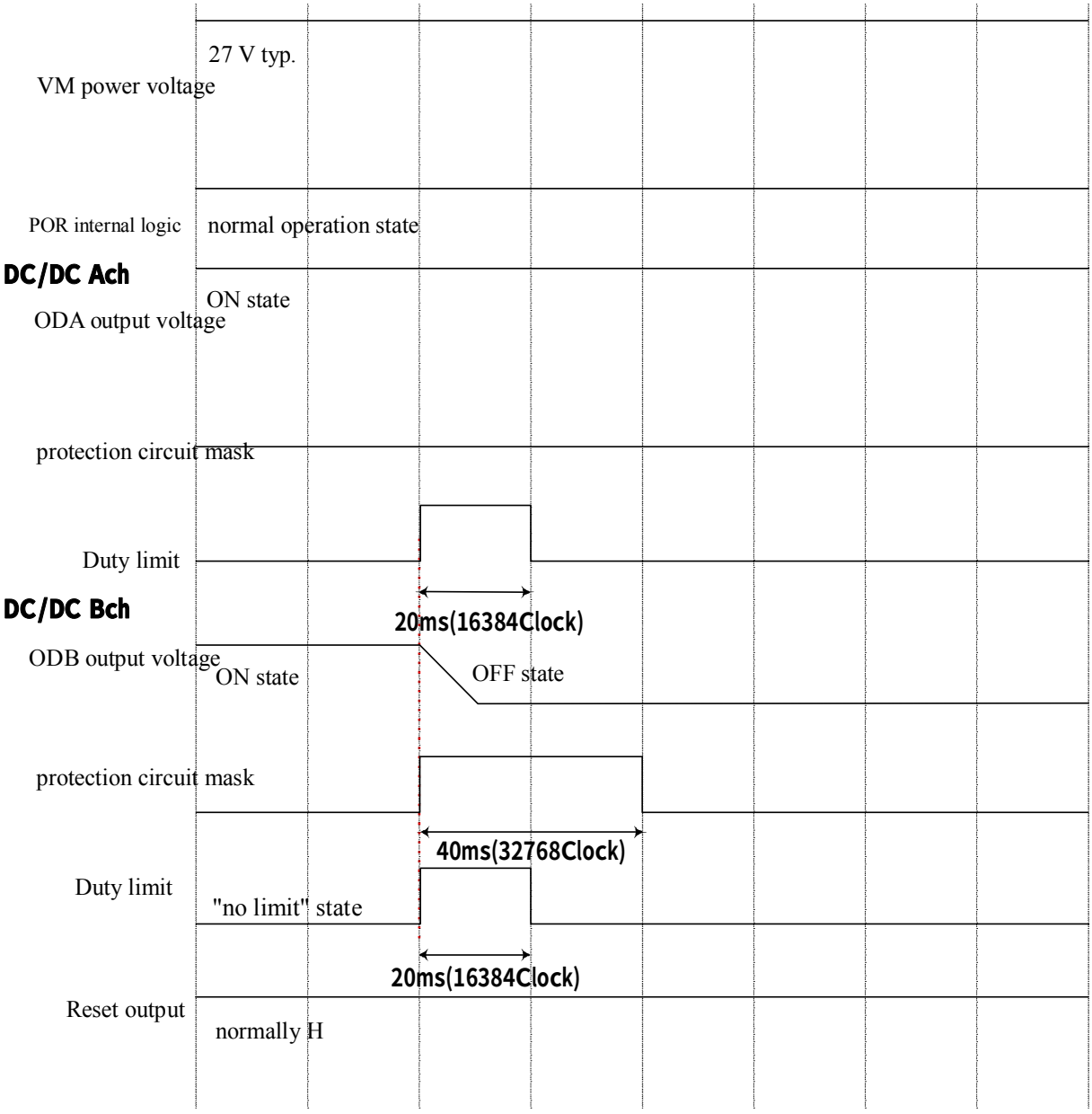


Notes: The above times are all predicated on f_{OSCDM}= 800kHZ and 1 clock = 1.25 us.

Duty limit is a function that limits the duty from going higher than 72% during the corresponding time frame. In addition, should a delay in going from Bch OFF to Ach OFF during the 40ms protective period occur, a 40ms protective mask will commence from the moment the Bch starts to go OFF. For example, if a 10ms delay occurs when the Bch OFF control starts, and Ach OFF is also being performed, both channels will be given a protective mask of 10ms + 40ms = 50ms.

Protection mask period is a period during which error detection is not performed.

(5) When only one DC-DC converter channel dynamically goes off after VM rise (after POR reset)



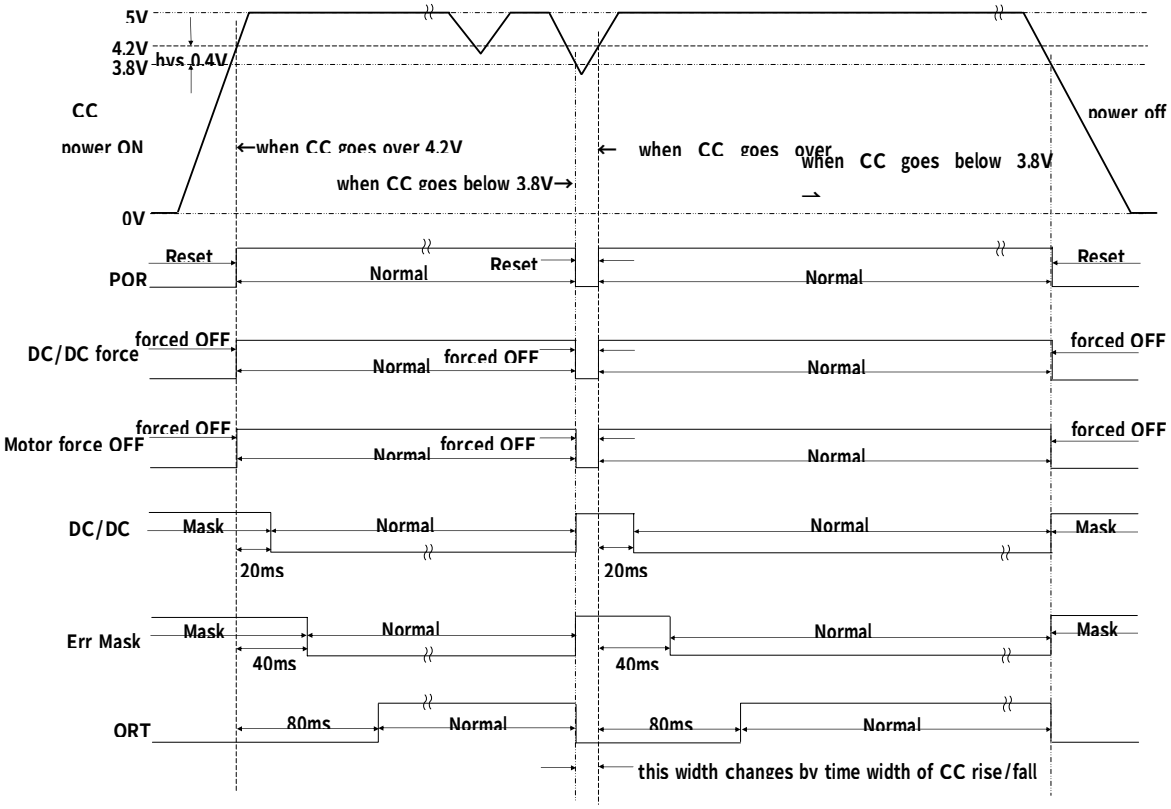
Notes: The above times are all predicated on f_{OSCDM}= 800kHZ and 1 CR_CLK = 1.25 us.

Duty limit is a function that limits the duty between 70 to 100% during the corresponding time frame.

Protection mask period is a period during which error detection is not performed.

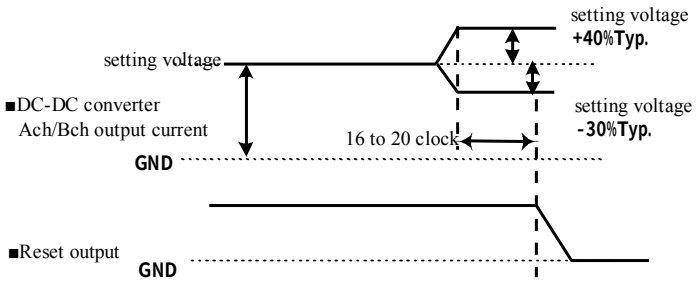
■**Various Sequences**

(1) Power ON/OFF

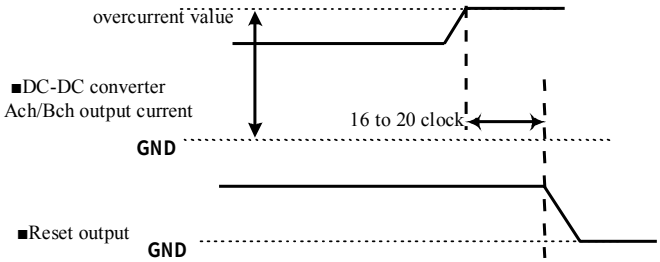


#2.5 POR/Mask/ORT operation

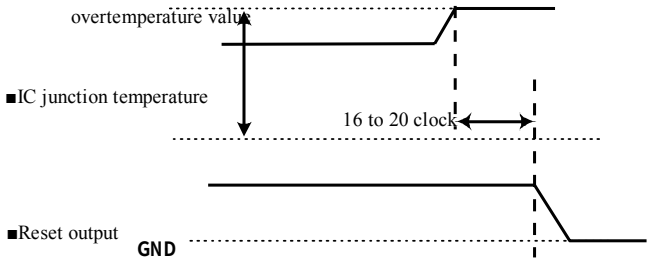
(2) Increase/Decrease Voltage Protection Function (when detected, the IC shuts down)



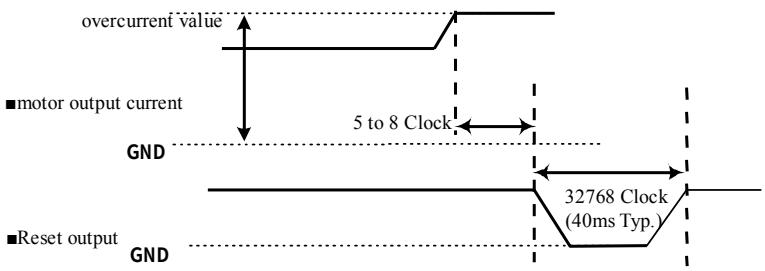
(3) DC-DC Converter Overcurrent Protection Function (when detected, the IC shuts down)



(4) IC Overtemperature Protection Function (when detected, the IC shuts down)



(5) Motor Overcurrent Protection Function (when detected, the IC shuts down)



Note: L pulse time is 40ms when F_{OSCDM} = 800kHz and 1Clock = 1.25us

■True Values Table

POR	Motor Sleep	Sleep	Cselect	DC-DC Select	Motor protection	DC-DC protection			DC/DC Ach (ODA)	DC/DC Bch (ODB)	Motor Out	Sleep Mode	16-bit register	ORT
					ISD	VSD	ISD	TSD						
1	1	X	X	X	X	X	X	X	1	1	1	X	ALL CLR	L
0	1	1	X	X	X	X	X	X	0	0	1	1	initial register overwrite OK	H
0	1	0	X	X	X	X	X	X	0	0	0	0	normal register overwrite OK	H
0	1	0	L	00	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	L	00	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	00	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	00	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	L	01	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	L	01	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	01	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	01	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	L	10	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	L	10	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	10	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	L	10	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	L	11	X	X	X	X	1	1	1	0	normal register overwrite OK	H
0	1	0	M	00	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	M	00	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	00	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	00	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	M	01	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	M	01	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	01	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	01	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	M	10	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	M	10	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	10	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	M	10	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	M	11	X	X	X	X	1	1	1	0	normal register overwrite OK	H
0	1	0	H	00	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	H	00	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	00	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	00	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	H	01	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	H	01	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	01	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	01	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	H	10	X	0	0	0	0	0	1	0	normal register overwrite OK	H
0	1	0	H	10	X	1	0	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	10	X	0	1	0	1	1	1	0	normal register overwrite OK	L
0	1	0	H	10	X	0	0	1	1	1	1	0	normal register overwrite OK	L
0	1	0	H	11	X	X	X	X	1	1	1	0	normal register overwrite OK	H
0	0	1	X	X	X	X	X	X	0	0	1	1	initial register overwrite OK	H
0	0	0	X	X	0	0	0	0	0	0	0	0	normal register overwrite OK	H
0	0	0	X	X	0	1	0	0	1	1	1	0	normal register overwrite OK	L pulse
0	0	0	X	X	0	0	1	0	1	1	1	0	normal register overwrite OK	L pulse
0	0	0	X	X	0	0	0	1	1	1	1	0	normal register overwrite OK	L pulse
0	0	0	X	X	1	0	0	0	1	1	1	0	normal register overwrite OK	H

Notes:
POR: 1 = internal initialization, 0 = normal operation
Motor Sleep: 1 = motor off, 0 = normal operation
See p.14 for Cselect details
DC/DC Select: the internal register value
ISD (overcurrent protection function): 1 = error detected, 0 = error not detected
VSD (abnormal output voltage protection function): 1 = error detected, 0 = error not detected
TSD (overtemperature protection function): 1 = error detected, 0 = error not detected
ODA, ODB, Motor output: 1 = ON, 0 = OFF
ORT L pulse: 32768 clock (40ms when fOSCM = 800Khz), L stands for length of time (period)
Motor Sleep and Sleep Mode Difference: Sleep mode is used to mean that the register overwrite switch
X = doesn't matter

■CSELECT Function and Powering On Related

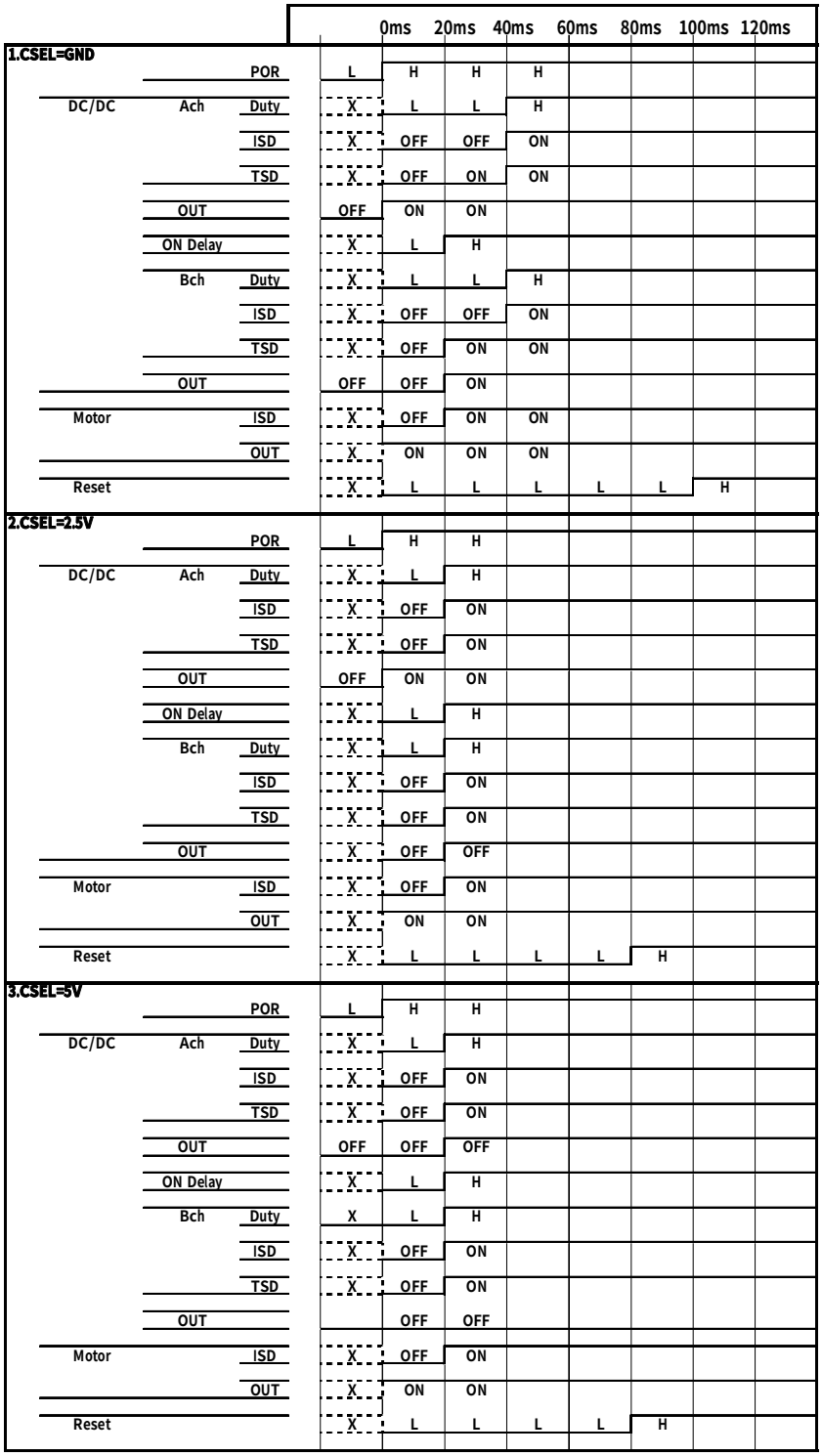
Note: The time axis is 0ms when the power is turned on and POR is released.

ON Delay: The Ach → Bch delay time generating logic

Duty: The time during which a duty limit is imposed on the DC-DC converter

ISD/TSD: The time during which a mask is placed on the protection

X: Don't care



■ DC-DC Converter Dynamic ON/OFF and Protection Mask Related

4. Dynamic ON/OFF

				"X"ms	+20ms	+40ms	+60ms
			POR	H	H		
Ach ON → A/Bch ON		CSELECT		2.5V	→ GND		
				2.5V	GND	GND	
DC/DC Conv	Ach	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON		
		OUT		ON	ON		
	ON Delay			X	L	H	
DC/DC Conv	Bch	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		OFF	OFF	ON	
Motor		ISD		ON	ON	ON	
		OUT		ON	ON	ON	
Reset				H	H	H	
A/Bch ON → Ach ON		CSELECT		GND	→ 2.5V		
				GND	2.5V	2.5V	
DC/DC Conv	Ach	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		ON	ON	ON	
	ON Delay			X	L	H	
DC/DC Conv	Bch	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		ON	OFF	OFF	
Motor		ISD		ON	ON	ON	
		OUT		ON	ON	ON	
Reset				H	H	H	
A/Bch ON → All OFF		CSELECT		GND	→ 5.0V		
				GND	5.0V		
DC/DC Conv	Ach	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON		
		OUT		ON	OFF	OFF	
	ON Delay			X	L		
DC/DC Conv	Bch	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		ON	OFF	OFF	
Motor		ISD		ON	ON	ON	
		OUT		ON	ON	ON	
Reset				H	H	H	

				"X"ms	+20ms	+40ms	+60ms
			POR	H	H		
Ach ON → All OFF		CSELECT		2.5V	→ 5.0V		
				2.5V	5.0V	5.0V	
DC/DC Conv	Ach	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		ON	OFF	OFF	
	ON Delay			X	L	H	
DC/DC Conv	Bch	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		OFF	OFF	OFF	
Motor		ISD		ON	ON	ON	
		OUT		ON	ON	ON	
Reset				H	H	H	
All OFF → All ON		CSELECT		5.0V	→ GND		
				5.0V	GND	GND	
DC/DC Conv	Ach	Duty		H	L		H
		ISD		ON	OFF		ON
		TSD		ON	ON	ON	
		OUT		OFF	ON	ON	
	ON Delay			X	L	H	
DC/DC Conv	Bch	Duty		H	L		H
		ISD		ON	OFF		
		TSD		ON	ON	ON	
		OUT		OFF	OFF	ON	
Motor		ISD		ON	ON	ON	
		OUT		OFF	OFF	ON	
Reset				H	H	H	
All OFF → Ach ON		CSELECT		5.0V	→ 2.5V		
				5.0V	2.5V	2.5V	
DC/DC Conv	Ach	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		OFF	ON	ON	
	ON Delay			X	L	H	
DC/DC Conv	Bch	Duty		H	L	H	
		ISD		ON	OFF	ON	
		TSD		ON	ON	ON	
		OUT		OFF	OFF	OFF	
Motor		ISD		ON	ON	ON	
		OUT		ON	ON	ON	
Reset				H	H	H	

■ **Various Protection Operations**

Protection Operation (DC-DC Converter ISD)						
DC/DC Conv	ISD	normal	detect	normal		
	TSD			normal	detect	normal
	OUT	ON	OFF			
Motor		X				
	ISD					
	OUT	ON	OFF			
Reset		H	L			

Protection Operation (TSD)						
DC/DC Conv	ISD			normal	detect	normal
	TSD	normal	detect	normal		
	OUT	ON	OFF			
Motor	ISD	X				
	OUT	ON	OFF			
Reset		H	L			

Protection Operation (Motor ISD)						
DC/DC Conv	ISD	normal				
	TSD	normal				
	OUT	ON				
Motor	ISD	normal	detect	normal		
	OUT	ON	OFF			
Reset		H	L	H		

■ Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Motor output voltage	VM	37	V	
Motor output current (Note 1) (Note 2)	IOST	1.3	A/phase	Stepper
	IOLAP	8.0	A	DC Motor B (500ns)
	IOLAE	3.0	A	DC Motor B (100ms)
	IOLAC	0.8	A	DC Motor B (Const)
	IOSAP	4.0	A	DC Motor S (500ns)
	IOSAE	2.5	A	DC Motor S (100ms)
	IOSAC	0.8	A	DC Motor S (Const)
DC-DC Conv output current	ICO A	750	mA	
	IDC B	750	mA	
DC-DC Converter maximum drive frequency	fDCDC	200	kHz	
Current detection pin voltage	VRS	VM ± 4.5	V	
Reset pin supply voltage	VRST		V	
Reset output current	IRST	-60	mA	
Logic input voltage	VIN	-0.4 to 6.0	V	
Power dissipation	PD	1.4	W	(Note 3)
		3.2	W	(Note 4)
Operating temperature	Topr	-40 to 85	°C	
Storage temperature	Tstg	-55 to 150	°C	
Junction temperature	Tj	150	°C	

Note 1: Refer to other chart for combinations
Note 2: Peak maximum during DC motor drive (less than 500ns)
Note 3: During unit measurement (Ta = 25°C)
Note 4: When mounted to dedicated mounting board (Ta = 25°C)
Ta: IC ambient temperature
Topr: IC ambient temperature when commencing operation
Tj: IC chip temperature during operation
The Tj maximum is limited by the TSD (thermal shutdown circuit)

In addition, if the thermal setting is designed to be within the proscribed thermal range, the initial torque current can be used as the normal operating current

■ Recommended Operating Conditions (Ta = 0 to 85°C)

Item	Symbol		Measurement Condition	Min.	Typ.	Max.	Unit
VM supply voltage	VM		excluding motor unit	7	27	32	V
			motor unit	15	27	32	
Output current	IOLA	Stepper	Ta = 25°C, per phase (during single axis drive)	-	0.6	1.0	A
	IOSL	DC	Ta = 25°C, peak 500 ns per H-bridge	-	–	4.0	
			Ta = 25°C, 100ms pulse per H-bridge	-	–	2.5	
			Ta = 25°C, Const	–	–	0.8	
DC-DC Current	IDC A		-	0	-	600	mA
	IDC B		-	0	-	600	mA
Reset output voltage	VRST		–	–	3.0	–	V
Reset output current	IRST		when VRST = 3.0V	–	–	-50	mA
Logic input voltage	VIN		-	GND	-	5.0	V
Clock frequency	fCLK		VM = 27	1.0	6.25	25	MHz
Motor chopping frequency	fchop		VM = 27	40	100	150	KHz
DC-DC chopping frequency	fchop		VM = 27	40	100	150	KHz
Vref reference voltage	Vref		VM = 27	0	2.0	3.0	V
Sleep current	Isleep OFF		SLEEP Mode (when VM = 7V) DC-DC Conv A/B OFF However, it is possible to set a serial default fCLK = 800kHz	–	2.0		mA
	Isleep7		SLEEP Mode (when VM = 7V) output 10mA at DC-DC Conv A/B total, other than that results in no action However, it is possible to set a serial default fCLK = 800kHz	–	4.8	10.0	
	Isleep27		SLEEP Mode (when VM = 27V) output 10mA at DC-DC Conv A/B total, other than that results in no action However, it is possible to set a serial default fCLK = 800kHz	–	5.0	10.0	
CC pin voltage	VOcc		IC internal autogeneration	–	5.0	–	V
CC decoupling capacity	Ccc		–	0.5	1.0	10	uF
Motor oscillation capacity	COSCM		Main clock for the whole IC. May result in malfunction if left open.	–	68	–	pF
DC-DC converter oscillation capacity	COSCD		–	–	120	–	pF
Motor oscillation frequency	fOSCM		COSCM = 68pF	–	800	–	KHz
DC-DC converter oscillation frequency	fOSCD		COSCD = 120pF	–	100	–	KHz
Release voltage when POR power input	POR1		vs. VM voltage	–	**5.1**		V
Release voltage when POR power turned off	POR2		vs. VM voltage	–	**4.2**		V

Note: This device does not incorporate an overvoltage protection circuit. Thus, if excess voltage is applied to the IC, the IC may be destroyed. Please make sufficient considerations during the design stage so that excess voltage will not be applied to the IC.

■ Motor Electrical Characteristics 1 (unless otherwise specified, Ta = 25°C, VM = 27 V)

Item		Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
Input voltage	HIGH	VIH	DC	CLK, STROBE, DATA pins	2.0	—	—	V
	LOW	VIL			—	—	0.8	
Input clamp voltage		VIK		IIK = -10mA	—	—	-0.4	
Input hysteresis width		VIN(HIS)	DC	CLK, DATA, STROBE, ENABLE, SLEEP input pins	-	200	-	mV
Input current	HIGH	IIN(H)		Pull Down pings (when 5 V)	—	50	100	µA
	LOW	IIN(L)			—	0	1	
Consumption current (VM pin)		IM1	DC	OUT OPEN, MOTOR LOGIC = L DC-DC 3 ON (100 kHz eternal operation) VM = 27V, output step OFF	—	—	8	mA
		IM2		OUT OPEN, CHOPPING = 200kHz (Phase input 200kHz) DC-DC 3 ON (100 kHz eternal operation) VM = 27V, output step OFF	—	—	30	
		IM3		OUT OPEN, MOTOR LOGIC=L DC-DC 3 ON (100 kHz eternal operation) DC-DC 5 ON (100 kHz eternal operation)	—	—	15	
Output standby current	Upper	IOH	DC	VRS = VM = 27V, Vout = 0V DATA = ALL L	-1.0	—	—	µA
Output leakage current	Lower	IOL		VRS = VM = CcpA = Vout = 27V	—	—	1.0	
Comparator reference voltage ratio	HIGH (reference)	VRS (H)	DC	Vref=3.0V, Vref(Gain)=1/10 TORQUE=(H.H)=100% setting	—	100	—	%
	LOW	VRS(L)		Vref=3.0V, Vref(Gain)=1/10 TORQUE=(L.H)=70% setting	68	70	72	
Output current differential		ΔIout1	DC	Difference between output current channels Iout=600mA	-5	—	5	%
Output current setting differential		ΔIout2	DC	Iout=600mA	-5	—	5	%
RS pin current		IRS	DC	VRS=27V, VM=27V,	—	—	300	µA
Output transistor drain-source On-resistance		RON(D-S)1	DC	Iout=0.6A, Tj=25°C, normal direction	—	0.6	0.72	Ω
		RON(D-S)1		Iout=0.6A, Tj=25°C, reverse direction	—	0.6	0.72	
		RON(D-S)2		Iout=0.6A, Tj=105°C, normal direction	—	0.78	1.01	
		RON(D-S)2		Iout=0.6A, Tj=105°C, reverse direction	—	0.78	1.01	

■ Motor Electrical Characteristics 2 (unless otherwise specified, Ta = 25°C, VM = 27 V)

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
Internal logic power supply voltage	V_{DD}	DC	(internally auto generated)	4.5	5.0	5.5	V
V_{ref} input voltage	Vref	DC	output ON	0.8	—	3.5	V
V_{ref} input current	Iref	DC	output OFF, Vref=3.0V	—	—	1.0	μA
V_{ref} attenuation ratio	Vref(Gain10)	DC	output ON Vref = 0 to 3.3V	1/9.6	1/10	1/10.4	—
	Vref(Gain20)			1/19.2	1/20	1/20.8	
TSD temperature	TjTSD (Note 1)	DC	—	130	**150**	170	°C
motor unit VM return voltage	VMR	DC		—	15.0	—	V
Over current protected circuit operation current	ISD (Note 2)	DC	fchop=100kHz setting	—	5.0	—	A

Note 1: Thermal shutdown (TSD) circuit

When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit is activated switching the output off.

When the temperature is set between 130 (min) to 170°C (max), the TSD circuit operates. When the TSD circuit is activated, the function data latched at that time are cleared. Output is halted until the reset is released. While the TSD circuit is in operation, the charge pump is halted.

Note 2: Overcurrent protection circuit

When current exceeding the specified value flows to the DC-DC output, the internal reset circuit is activated switching the outputs of both shafts to off.

When the ISD circuit is activated, the function data latched at that time are cleared.

The overcurrent protection circuit remains activated until the V_M voltage is reapplied. Activating the ISD initializes all the circuits in the IC, which causes the charge pump to be stopped. For the failsafe operation, insert a fuse in the power supply.

■ **Motor Electrical Characteristics 3（Ta = 25°C, VM = 27 V、Iout = 1.0A）**

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
Chopper current level			θA=90 (θ16)	−	100	−	
			θA=84 (θ15)	−	100	−	
			θA=79 (θ14)	93	98	−	
			θA=73 (θ13)	91	96	−	
			θA=68 (θ12)	87	92	97	
			θA=62 (θ11)	83	88	93	
			θA=56 (θ10)	78	83	88	
			θA=51 (θ9)	72	77	82	
			θA=45 (θ8)	66	71	76	
			θA=40 (θ7)	58	63	68	
			θA=34 (θ6)	51	56	61	
			θA=28 (θ5)	42	47	52	
			θA=23 (θ4)	33	38	43	
			θA=17 (θ3)	24	29	34	
			θA=11 (θ2)	15	20	25	
			θA=6 (θ1)	5	10	15	
			θA=0 (θ0)	−	0	−	

■ DC-DC Converter Electrical Characteristics （Tj = 0 to 120°C VM = 7 to 27 V）

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
output voltage error	ΔVout U	DC	Tj=**0 to 120**°C, fchop=100, when 150kHz setting, 50mA to 600mA	-7.0	0	7.0	%
	ΔVout L	DC	Tj=**0 to 120**°C,fchop=100, when 150kHz setting , 50mA to 600mA	**-7.0**	**0**	**7.0**	
DC-DC output OFF leakage current	IODC	DC	VM=27V, upper	-2.0	−	−	uA
			VM=27V, lower			2.0	
Output transistor drain – source ON resistance	RON (D-S) 1	DC	Iout=300mA, Tj=25°C, normal direction, upper	-	0.7	0.84	Ω
			Iout=300mA, Tj=25°C, normal direction, lower	-	1.1	1.32	
	RON (D-S) 1		Iout=300mA, Tj=25°C, reverse direction, lower	-	1.1	1.32	
	RON (D-S) 2		Iout=300mA, Tj=105°C, normal direction, upper	-	0.9	1.1	
			Iout=300mA, Tj=105°C, normal direction, lower	-	1.4	1.7	
	RON (D-S) 2		Iout=300mA, Tj=105°C, reverse direction, lower	-	1.4	1.7	
Over current protected circuit operation current	ISD DC	DC	when fchop=100kHz setting	-	1.2	-	A
abnormal voltage protection circuit	VSDU DCU	DC	vs. setting voltage	+30	+40	+50	%
	VSDD DCL			-40	-30	-20	
feedback voltage	VFB	DC	−		1.5		V
CSELECT voltage	VCsel	DC	DC/DC Ach and Bch All ON	−	0	−	V
			DC/DC Ach ON	1.25	2.5	3.75	
			DC/DC Ach and Bch All OFF	−	5.0	−	

■ Reset Electrical Characteristics （Tj = 0 to 120°C VM = 7 to 27 V）

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
VM power reset voltage	VMR(ALL)		all functions OFF	-	5.1	−	V
	VMR(Motor)		only motor OFF	−	15	−	
DC-DC converter reset voltage	VDCU		vs. output setting voltage	+30	+40	+50	%
	VDCL			-40	-30	-20	
Reset delay time	trst		65536 CR-CLK from Bch ON	−	80	−	ms
Reset output pulse width	t rst(ON)		4096 CR-CLK	40	−	−	ms
Reset signal output current	IRST			−	−	50	mA
Instant voltage reaction time	t			-	2fcr	−	us

* CR-CLK is the frequency of OSC_M.

■**Motor AC Characteristics (Ta = 25°C, VM = 27 V, motor impedance 6.8mH/5.7Ω)**

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
Clock frequency	fCLK		—	1.0	—	25	MHz
Minimum clock pulse width	tw (CLK)		—	40	—	—	ns
	twp (CLK)			20	—	—	
	twn (CLK)			20	—	—	
Minimum strobe pulse width	tSTROBE		—	40	—	—	ns
	tSTROBE (H)			20	—	—	
	tSTROBE (L)			20	—	—	
Data setup time	tsuSIN-CLK		—	10	—	—	ns
	tsuST-CLK			10	—	—	
Data hold time	thSIN-CLK		—	10	—	—	ns
	thCLK-ST			10	—	—	
Output transistor switching characteristic	tr		when load of 6.8mH/5.7Ω	—	0.4	1.0	µs
	tf			—	0.4	1.0	
	tpLH (ST)		when load of 6.8mH/5.7Ω between STROBE (↑) and OUT	—	15	—	
	tpHL (ST)			—	10	—	
	tpLH (CR)		when load of 6.8mH/5.7Ω between CR and OUT	—	1.2	—	
	tpHL (CR)			—	2.5	—	
Noise rejection dead band time	tBLNK		Iout=0.6A	200	300	400	ns
CR reference signal oscillation frequency	f_{OSC_M}		Osc_M=68pF	600	800	1000	kHz
Chopping possible frequency	fchop (Min)		Output active (Iout=0.6A) Step fixed	40	100	150	kHz
	fchop(Typ.)						
	fchop(Max)						
Motor chopping setting frequency	fchop(M)		Output actrive (Iout=0.6A) When M_osc CLK=800kHz	—	100	—	kHz

■DC-DC Converter AC Characteristics（Tj = 0 to 120°C, VM = 7 to 27 V）

Item	Symbol	Test Circuit	Measurement Conditions	Min.	Typ.	Max.	Unit
Output transistor switching characteristic	tr_D	AC	−	−	0.1	−	µs
	tf_D			−	0.1	−	
DC-DC reference signal oscillation frequency	fOSC_D	AC		80	100	120	kHz
DC-DC setting frequency	fchop_D	AC	−	40	100	**200**	kHz

Calculation of Motor Setting Current

The motor setting current value is determined by R_{RS} and V_{ref} as shown in the equation below:

$$I_{out}\ (max) = \frac{1}{V_{ref\ (gain)}} \times V_{ref}\ (V) \times \frac{Torque\ (torque = 100, 75, 65, 60\%:\ input\ serial\ data)}{R_{RS}\ (\Omega)}$$

For example, if

$1/V_{ref}$ (gain): $1/V_{ref}$ attenuation ratio (typ.) is 1/10.0 (Typ),
and if you want to input

V_{ref} = 1 V
and

Torque = 100%

and output

I_{out} = 0.1A,
then

R_{RS} = 1.0 Ω (0.5 W or more) is required.

- **Calculating the Motor and DC Converter CR Oscillating Frequency(chopping reference frequency)**

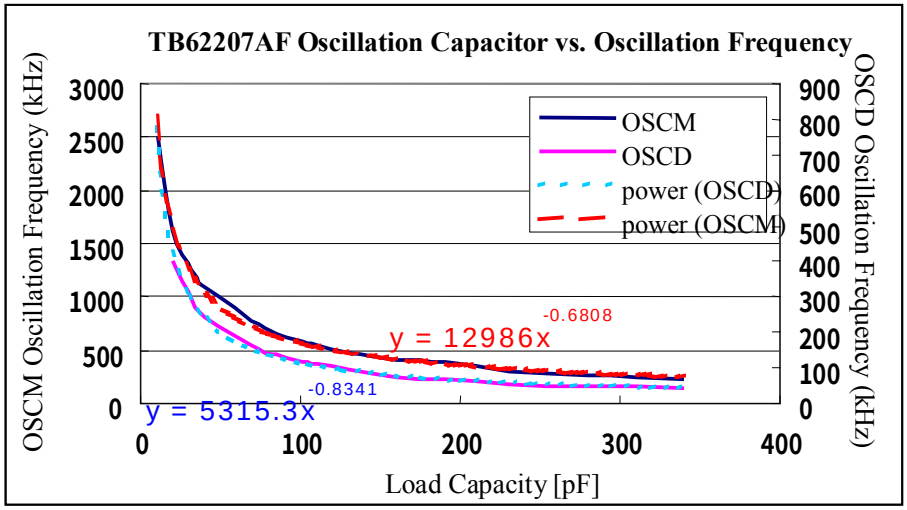
①Calculating for the Motor (Typ.)

OSCM $y = 0.0879 * C^{-0.6808}$

②Calculating for the DC Converter (Typ.)

OSCD $y = 0.0005 * C^{-0.8341}$

■Reference Characteristic Graph



■ Reference Data

Actual Measurement References Capacity (pF) = capacitor capacity (pF) + probe capacity (10pF)

Capacity (pF)	OSCM	OSCD	Capacity (pF)	OSCM	OSCD
20	1620	404	110	540	110
32	1260	295	130	480	93
40	1100	246	160	405	76
78	710	144	190	385	70
85	655	136	230	300	55
92	620	125	280	258	45
101	580	116	340	235	40

■ Reference Data

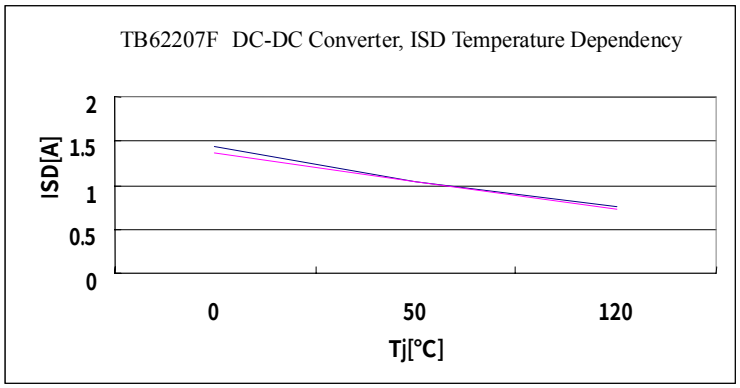
DC-DC Converter, ISD temperature, Power Voltage Dependency

VM voltage [V]	Tj [°C]	Actual ISD [A]
7 ↓	0	1.43
	50	1.04
	120	0.76
27 ↓	0	1.36
	50	1.03
	120	0.74

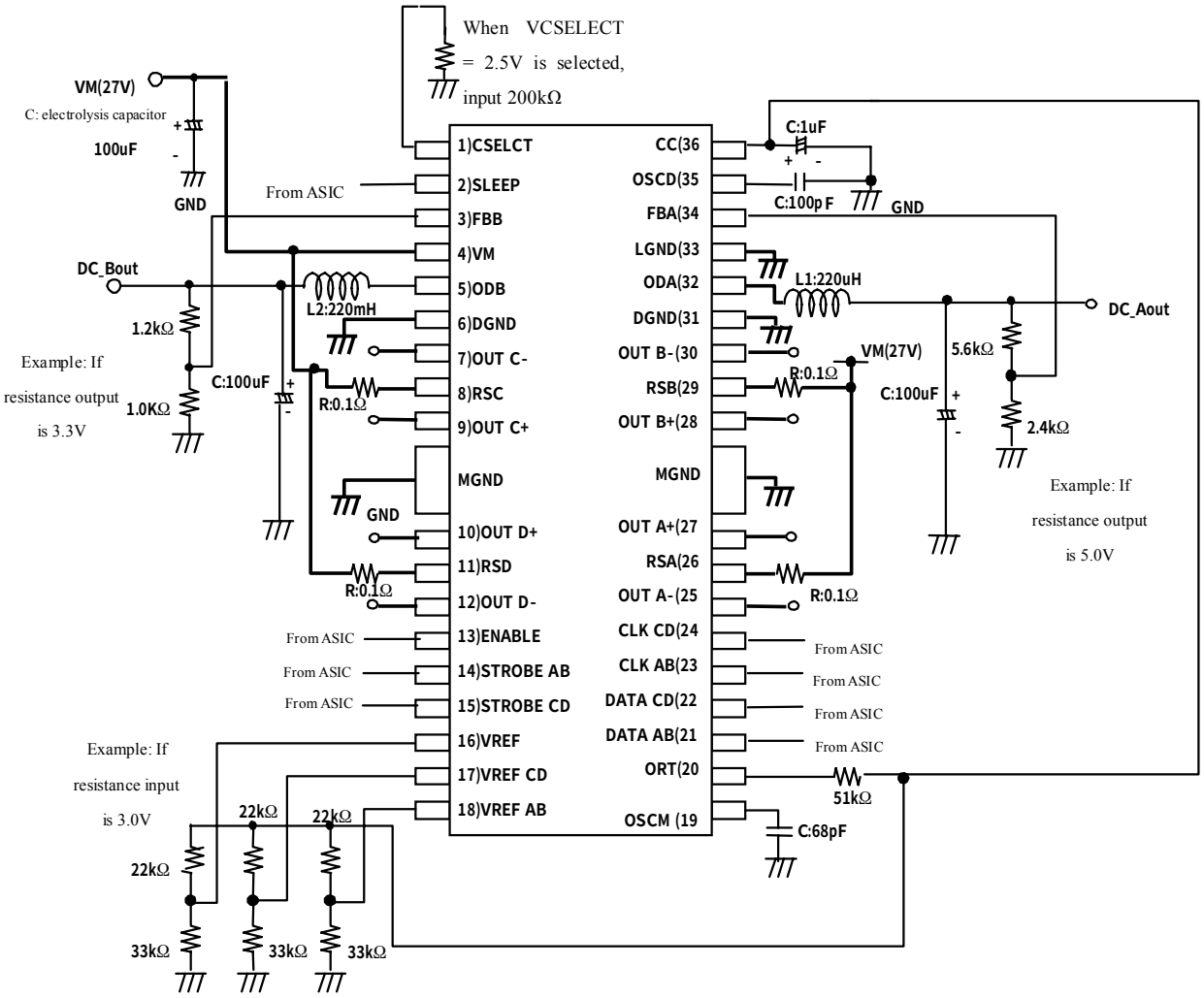
upper

VM voltage [V]	Tj [°C]	Actual ISD [A]
7 ↓	0	0.72
	50	0.73
	120	0.72
27 ↓	0	0.71
	50	0.72
	120	0.68

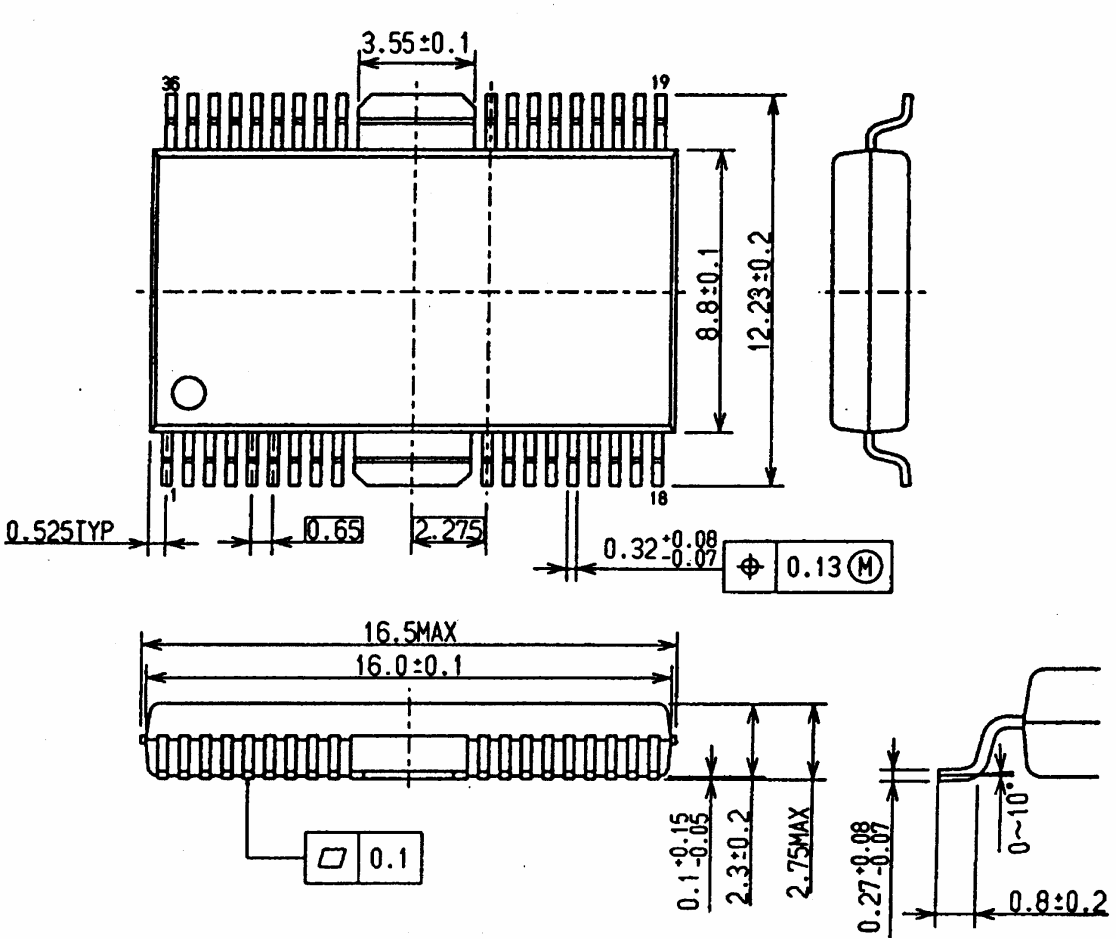
lower



■ **Application Circuit**



Pacakge Dimensions HSOP36-P-450-0.65



weight 0.79 g (typ.)

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