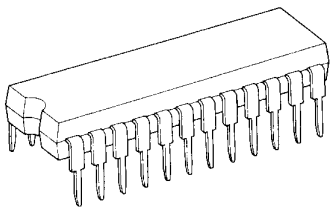
TOSHIBA Bi−CMOS INTEGRATED CIRCUITS SILICON MONOLITHIC

TB62713N,TB62713F

7 × 5 DOT DISPLAY DECODER AND DRIVER (COMMON CATHODE ROW CAPABILITY)

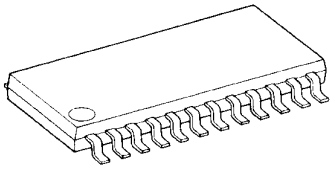
The TB62713N and TB62713F are multifunctional, compact, 7×5 dot matrix LED display drivers.
Each of these ICs can directly drive and control one 7×5 dot matrix LED display.
The display shows the common cathode rows.
Row output uses a constant current, which is set using an external resistor.
The column output is standard PNP output.
A synchronous serial port connects the IC to the CPU.
The different modes of control provided by this device, including Duty Control Register Set, Digit Set, Decode Set and Standby Set, are all based on every 16−bit of serial data.

TB62713N



SDIP24-P-300-1.78

TB62713F



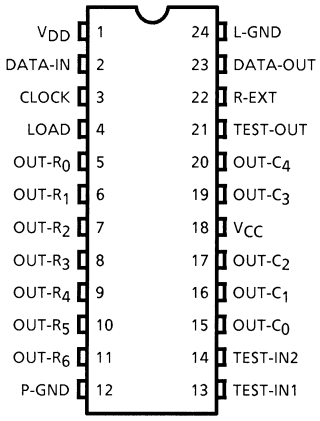
SSOP24-P-300-1.00

Weight
SDIP24-P-300-1.78: 1.62 g (typ.)
SSOP24-P-300-1.00: 0.32 g (typ.)

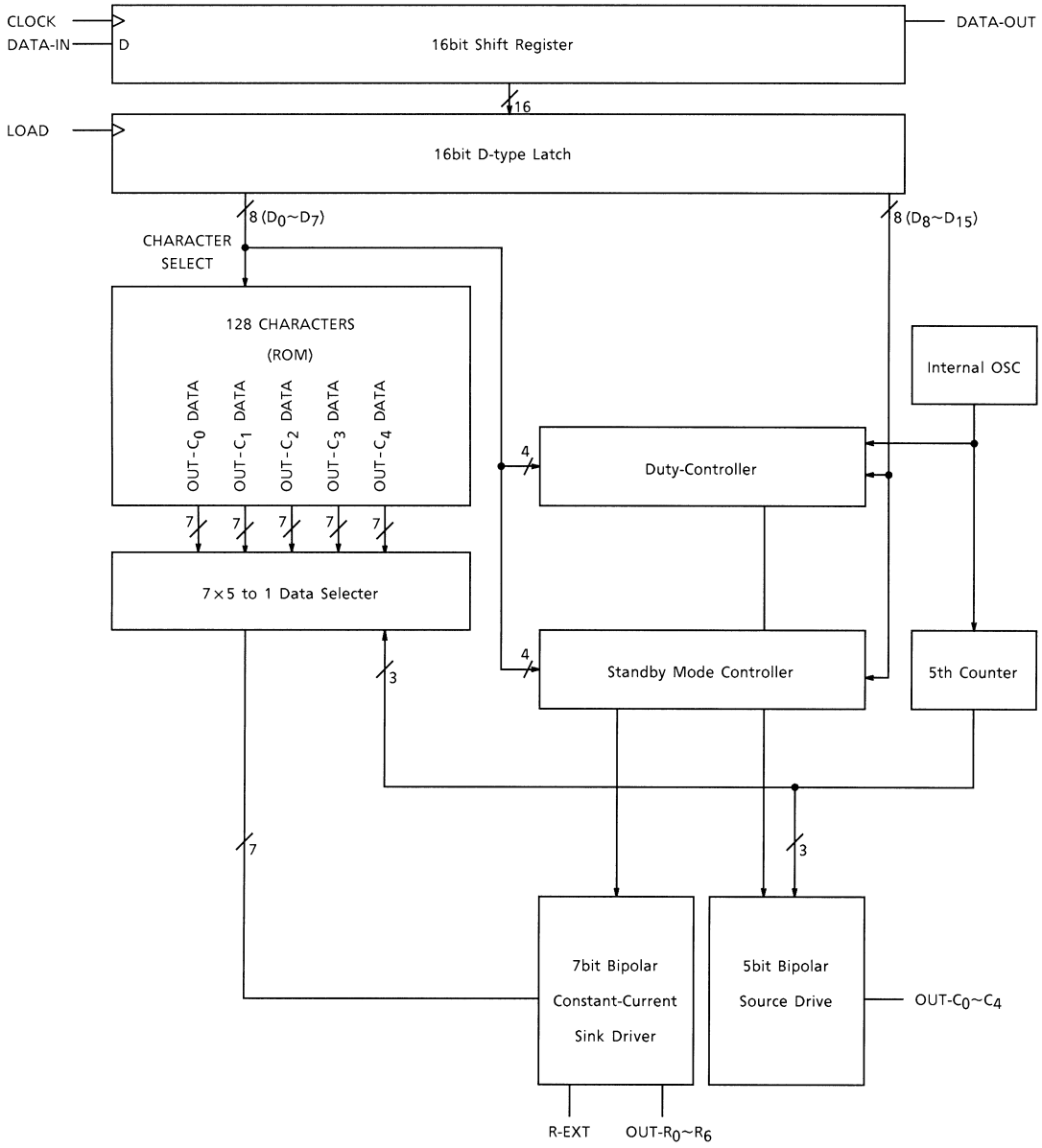
FEATURES

- Control circuit power supply voltage
  : V_{DD} = 4.5 to 5.5 V
- Digit output rating
  : −17 V / −350 mA
- Row output rating
  : 17 V / 50 mA
- Built−in decoder
  : Decoding based on ASCII code.
- Digit control function
  : Automatically turns on column output OUT−C_0 to OUT−C_4 in sequence.
- Maximum transmission frequency (for serial data transmission)
  : f_{CLK} = 15 MHz
- Row output (OUT−R_0 to OUT−R_6)
  Output current can be set to 50 mA using an external resistor.
- Constant current tolerance (Ta = 25°C, V_{DD} = 5.0 V)
  : Variation between bits = ±7%, variation between devices (including variation between bits) = ±15%, @$V_{CE} \geq$ 0.7 V
- Package
  : 24−pin SDIP (SDIP24−P−300−1.78)
  24−pin SSOP (SSOP24−P−300−1.00)

PIN ASSIGNMENT (Top view)



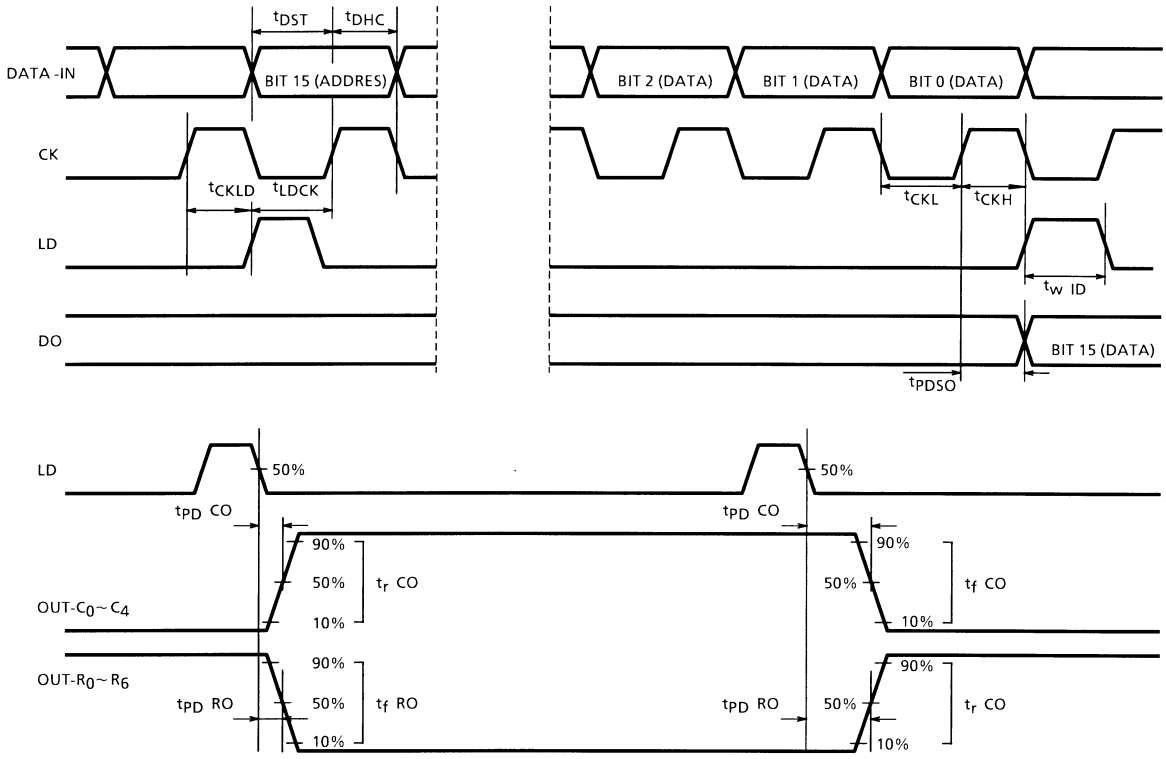
EQUIVALENT CIRCUIT DIAGRAM / BLOCK DIAGRAM



PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION
1	V_{DD}	5 V power pin.
2	DATA−IN (DI)	Serial data input pin.
3	CLOCK (CK)	Clock input pin. The shift register shifts data on the clock's rising edge.
4	LOAD (LD)	Load signal input pin. The data in the D_8 to D_{15} bits of the 16−bit shift register. Are read on the rising edge of the load signal and the current load register is selected from among the Duty Register, the Decode & Digit Register, or Data Registers 0 to 3. The D_0 to D_7 bits contain data corresponding to the same registers just described, which are read on the load signal's falling edge.
5~11	OUT−R_0 to R_6	Row output pins. These pins output constant sink current. Connect these pins to the LED's cathode.
12	P−GND	Ground pin for row output.
13	TEST−IN2	Product test pin. In normal use, be sure to connect to ground.
14	TEST−IN1	Product test pin. In normal use, be sure to connect to ground.
15, 16, 17, 19, 20	OUT−C_0 to C_4	Column output pins. These pins output the V_{CC} pin voltage as a source current output. Connect these pins to the LED common anodes.
18	V_{CC}	Power pin for column output.
21	TEST−OUT	Product test pin. In normal use, be sure to leave this pin open.
22	R−EXT	Current setting pin for the OUT−R_0 to OUT−R_6 pins. Connect a resistor between this pin and GND when setting the current.
23	DATA−OUT (DO)	Serial data output pin. Use this pin when TB62713N or TB62713F devices are cascade−connected.
24	L−GND	Ground pin for logic and analog circuits.

TIMING DIAGRAM



DATA INPUT

- Transfer data to the DATA−IN pin on every 16−bit including address (8 bits) and data (8 bits). After the 16th clock−signal input following this data transfer, input a load signal from the LD pin.

- Input the load signal using an Active High pulse. The register address is set on the rising edge of the load pulse. On the subsequent falling edge, the data are read as data of the mode of the register.

DESCRIPTION OF OPERATION

- Data input (DATA−IN, CLOCK, LOAD)

  The data are input serially using the SERIAL−IN pin. The data input interface consists of a total of three inputs : SERIAL−IN, LOAD, and CLOCK.
  Binary code stored in the 16−bit shift register offers control modes including Duty Control Register Set, Digit Set, Decode Set and Standby Set.
  The data are shifted, starting from the MSB, on the rising edge of the clock. Cascade−connecting TB62713N or TB62713F devices provides capability for controlling a larger number of digits extensibility.
  The serial data in the 16−bit shift register are used as follows : the four bits D_{15} (MSB) to D_{12} select the IC operating mode (Table 1), while bits D_{11} to D_8 select the register corresponding to the operating mode (Table 2).
  Bits D_7 to D_0 (LSB) are used for detail settings such as number of digits in use, character settings in each digit, and light intensity of these.
  The internal registers are loaded on the rising edge of the LOAD signal, which causes loading of data from an external some into the D_{15} (MSB) to D_8 bits of the shift register, operating mode and the corresponding register selection data. On the subsequent falling edge, the detail setting data of D_7 to D_0 (LSB) are loaded.
  Normally LOAD is Low. After a serial transfer of 16bits, the input of a High−level pulse loads the data.
  Note the following caution. Use the D_{15} to D_8 setting and the D_7 to D_0 detail data setting as a pair. If just the D_7 to D_0 data are input without setting D_{15} to D_8 an error condition may result, in which the device will not operate normally. The register settings will not be normal. If the current mode is set again by a new signal, the data for D_{15} to D_8 must also be re−input.

- Operating precautions

  At power−on or after operation in Clear mode (in initial state), the data are reset. If the IC enters Normal mode after data are input and characters are specified, LEDs are lit according to the input data.
  Operating the IC in Blank mode (all lights off) or in All ON mode (all lights lit) does not affect the internal data. Setting the IC to Normal mode again continues the LED lighting in the state governed by the settings made immediately before mode change.
  Normal mode (not Shut Down, Clear, Blank, or All On mode) continues the operations set in Load Register mode. In Normal mode, operations are governed by any new settings msde in the Load register, as soon as the changed setting values are loaded.

OPERATING MODE SETTINGS

- Operating modes (Table 1)
  These ICs support the following five operating modes :

  1. Blank : Forcibly turns OFF the constant−current output both for data and digit setting. This mode is not affected by the values in bits D_{11} to D_0.

  2. Normal : Used for display operations after the settings of the digits are complete. This mode is not affected by D_{11} to D_0. Note that setting this mode without making any other settings results in a blank display (all lights off).

  3. Load Register : Used for the detail settings of the Duty Control Register and for inputting display data. D_{11} to D_0 of the shift register are used for the detail settings of the digits currently being driven. (Table 2).

  4. All On : Forcibly turns ON the constant−current data output. This mode is not affected by D_{11} to D_0.

  5. Standby : Used to set Standby state (in which internal data are not cleared) and to clear data (initialization).
     The settings in D_3 to D_0 determine the choice between standby state or initialization.

Table 1 Operating mode settings

	REGISTER DATA								INITIAL SETTING
	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}~D_8	D_7~D_4	D_3~D_0	HEX CODE	
BLANK (OUT−n & OUT−R_n ALL−OFF)	0	0	0	0	—	—	—	0−−−H	■
NORMAL (OPERATION)	0	0	0	1	—	—	—	1−−−H	
LOAD REGISTER (DUTY & CHARACTER−DATA)	0	0	1	0	X	X	X	2XXXH	
ALL ON (OUT−C_n ALL ON)	0	0	1	1	—	—	—	3−−−H	
STANDBY	0	1	0	0	—	—	X	4−−XH	

X = Input H or L. "—" = Are not affected by the truth table.

LOAD REGISTER SELECTION

- Load Register Selection modes (Table 2)

  These modes select the register to provide the data to control the IC operation. The Load Register selection mode is determined by the settings of D_{15} to D_{12} and D_{11} to D_8 of the shift register

  1. Duty Register : Sets the digit output duty cycle. Duty Settings can be made in 16 steps from 0 / 16 to 15 / 16. (Table 3)

  2. Data Register : Sets 7 × 5 display characters. D_7 to D_0 are used to set the display characters.

Table 2 Load register selection

	REGISTER DATA							
	D_{15}~D_{12}	D_{11}	D_{10}	D_9	D_8	D_7~D_4	D_3~D_0	HEX CODE
LOAD DUTY REGISTER	2H	0	0	0	0	X	X	20XXH
LOAD CHARACTER−DATA REGISTER	2H	0	0	0	1	X	X	21XXH

X = Input H or L.

DUTY CONTROL REGISTER SETTINGS

- Duty Control Register detail settings and operation (Table 3)

  Writing 20H to D_{15}~D_8 and writing 0~FH to D_3~D_0 sets the duty cycle shown in the following table for the digit−side source driver output. The duty cycle can be set in 16 steps.
  The initial setting is 15 / 16. After Data Clear, the setting is also 15 / 16.
  The current settings remain in force until changed (to the initial state, Data Clear state, standby state, or by reset execution).

Table 3 Duty control register settings

DUTY CYCLE	REGISTER DATA							INITIAL SETTING
	D_{15}~D_8	D_7~D_4	D_3	D_2	D_1	D_0	HEX CODE	
0 / 16	20H	—	0	0	0	0	20X0H	
1 / 16	20H	—	0	0	0	1	20X1H	
2 / 16	20H	—	0	0	1	0	20X2H	
3 / 16	20H	—	0	0	1	1	20X3H	
4 / 16	20H	—	0	1	0	0	20X4H	
5 / 16	20H	—	0	1	0	1	20X5H	
6 / 16	20H	—	0	1	1	0	20X6H	
7 / 16	20H	—	0	1	1	1	20X7H	
8 / 16	20H	—	1	0	0	0	20X8H	
9 / 16	20H	—	1	0	0	1	20X9H	
10 / 16	20H	—	1	0	1	0	20XAH	
11 / 16	20H	—	1	0	1	1	20XBH	
12 / 16	20H	—	1	1	0	0	20XCH	
13 / 16	20H	—	1	1	0	1	20XDH	
14 / 16	20H	—	1	1	1	0	20XEH	
15 / 16	20H	—	1	1	1	1	20XFH	■

X = Input H or L. "—" = Are not affected by the truth table.

STANDBY MODE SETTINGS

- Standby mode settings and operation (Table 4)

  Writing 4H to D_{15}~D_8 and writing 0001 to D_3~D_0 sets Standby mode. Writing 4H to D_{15}~D_8 and writing 0001 to D_3−D_0 sets All Data Clear mode.

  Standby mode maintains the settings made immediately before this mode came in force, turns the output current OFF, and controls the bias current the internal circuits. Resets all settings to their initial states.

Table 7 Standby mode settings

	REGISTER DATA						
	D_{15}~D_8	D_7~D_4	D_3	D_2	D_1	D_0	HEX CODE
STANDBY (NO DATA CLEAR)	4−H	—	0	0	0	0	4XX0H
ALL DATA CLEAR	4−H	—	0	0	0	1	4XX1H

X = Input H or L. "—" = Are not affected by the truth table.

- Character (ASCII) genetator decoding

As the following table show,the characters are decoded using combinations of the data in D_0 to D_7.

Table 6.1 List of ASCII character set decoding data

D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D_7 D_6 D_5 D_4																
0 0 0 0									See Table 6.2.							
0 0 0 1																
0 0 1 0																
0 0 1 1																
0 1 0 0																
0 1 0 1																
0 1 1 0																
0 1 1 1																

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Table 6.2 List of ASCII character set decoding data

D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D_7 D_6 D_5 D_4	See Table 6.1.															
0 0 0 0	0															
0 0 0 1	1															
0 0 1 0	2															
0 0 1 1	3															
0 1 0 0	4															
0 1 0 1	5															
0 1 1 0	6															
0 1 1 1	7															

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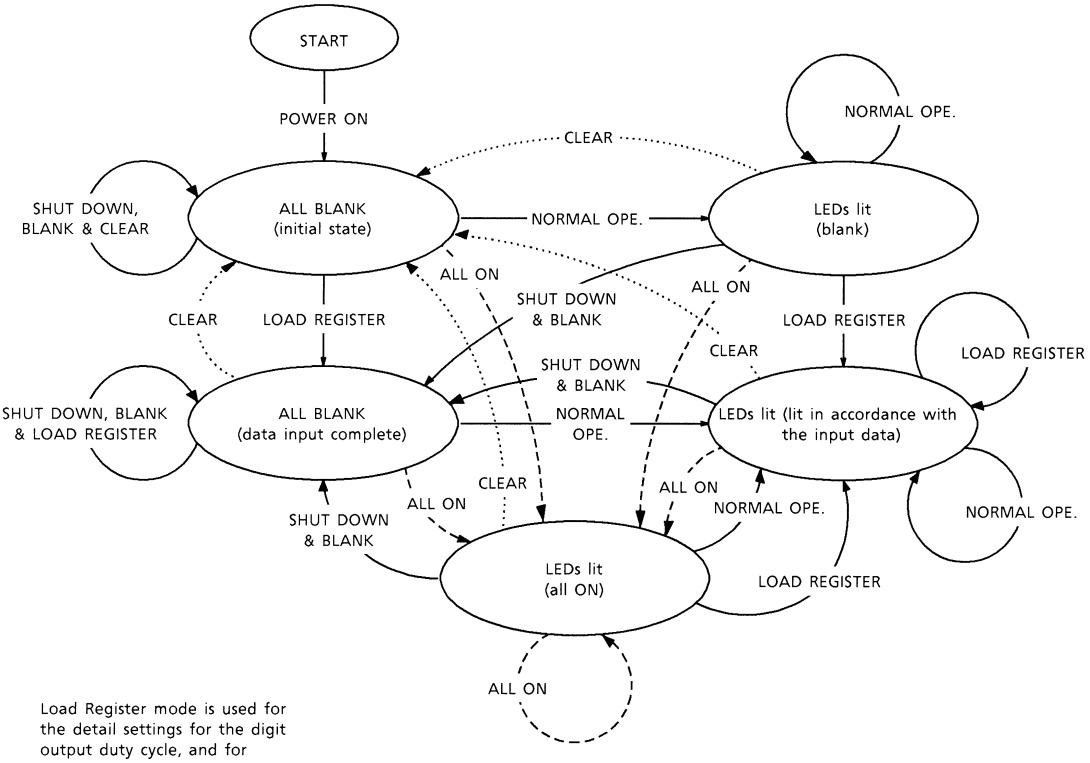
DATA INPUT
(Example 1: Displays A to G, blinks F and G, and adjusts luminance.)

STEP	D_{15} ~D_{12}	D_{11} ~D_8	D_7 ~D_4	D_3 ~D_0	OUT−R_0~R_6	OUT−C_0~C_4	MODE	DISPLAY INFORMATION
0	—	—	—	—	OFF	OFF	At power−on (= CLEAR MODE)	ALL BLANK
1	0010	0000	XXXX	1111	OFF	OFF	DUTY = 15 / 16	ALL BLANK
2	0010	0001	0100	0001	OFF	OFF	CHARACTER−DATA = A	ALL BLANK
3	0001	XXXX	XXXX	XXXX	OFF	ON	NORMAL	A
4	0010	0001	0100	0010	ON	ON	CHARACTER−DATA = B	B
5	0010	0001	0100	0011	ON	ON	CHARACTER−DATA = C	C
6	0010	0001	0100	0100	ON	ON	CHARACTER−DATA = D	D
7	0010	0001	0100	0101	ON	ON	CHARACTER−DATA = E	E
8	0010	0000	0100	0110	ON	ON	CHARACTER−DATA = F	F
9	0000	XXXX	XXXX	XXXX	OFF	OFF	BLANK	ALL BLANK
10	0010	0000	XXXX	1000	OFF	OFF	DUTY = 8 / 16	ALL BLANK
11	0001	XXXX	XXXX	XXXX	ON	ON	NORMAL	F (MIDDLE BLIGHT)
11	0000	XXXX	XXXX	XXXX	OFF	OFF	BLANK	ALL BLANK
12	0010	0000	0100	0111	ON	OFF	CHARACTER−DATA = G	ALL BLANK
13	0001	XXXX	XXXX	XXXX	ON	ON	NORMAL	G (MIDDLE BLIGHT)
15	0100	XXXX	XXXX	0000	OFF	OFF	STANDBY (SHUT DOWN)	ALL BLANK

STATE TRANSITION DIAGRAM



Load Register mode is used for the detail settings for the digit output duty cycle, and for inputting display data.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage for Logic Circuits		V_{DD}	7.0	V
Supply Voltage		V_{CC}	17	V
OUT−C_0 to OUT−C_3 Output Current		I_{CO}	−420	mA
OUT−R_0 to OUT−R_6 Output Current		I_{RO}	60	mA
Output Current for Logic Block		I_{OH} / I_{OL}	±5	mA
Input Voltage		V_{IN}	−0.3~V_{DD}+0.3	V
Operating Frequency		f_{CK}	15.0	MHz
Total Supply Current		I_{VDD}	420	mA
Power Dissipation	TB62713N	P_D	1.78	W
	TB62713F		0.62	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, R_{EXT} = 580 Ω, Ta = −40 to 85°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Perating Power Supply Current for Output Block	I_{CC1}	1	SET NORMAL OPE. MODE, R_{EXT} = 590 Ω @OUT−R_0~R_6 ALL ON, Ta = 25°C	—	370	—	mA
	I_{CC2}	1	SET NORMAL OPE. MODE, R_{EXT} = 590 Ω @OUT−R_0~R_6 ALL ON, V_{CC} = 12 V, Ta = 25°C	—	390	—	
OUT−C_0 to OUT−C_4 Scan Frequency	f_{OSC}	2	NORMAL OPE. MODE, V_{DD} = 4.5~5.5 V	300	600	1200	Hz
OUT−R_0 to OUT−R_6 Output Sink Current	I_{RO}	3	NORMAL OPE. MODE, V_{CE} = 0.7 V, R_{EXT} = 590 Ω	36.5	43.0	49.4	mA
OUT−C_0 to C_4 Output Leakage Current	I_{leak1}	4	ALL OFF MODE, V_{CC} = 17 V	—	—	−20	μA
OUT−R_0 to R_6 Output Leakage Current	I_{leak2}	4	ALL OFF MODE, V_{CC} = 17 V	—	—	20	μA
OUT−C_0 to C_4 Output Voltage	V_{OUT}	5	NORMAL OPE. MODE, I_{OUT}−C_n = −350 mA	3.0	—	—	V

Logic block

CHARACTERISTIC	SYMBOL	Test Cir−cuit	TEST CONDITION	MIN	TYP.	MAX	UNIT
Static Power Supply Current for Logic Circuits	I_{DD1}	6	STANDBY MODE, Ta = 25°C	—	—	200	μA
	I_{DD2}	6	BLANK MODE, Ta = 25°C	—	—	12.5	mA
Operating Power Supply Current for Logic Circuits	I_{DD3}	6	NORMAL OPE. MODE, f_{CLK} = 10 MHz, DATA−IN : OUT−R_0~R_6 = ON, Ta = 25°C	—	—	20.5	mA
High Input Current for Logic Circuits	I_{IH}	—	DATA−IN, LOAD & CLOCK : V_{IN} = 5 V	—	—	1	μA
Low Input Current for Logic Circuits	I_{IL}	—	DATA−IN, LOAD & CLOCK : V_{IN} = 0 V	—	—	−1	μA
High Output Voltage for Logic Circuits	V_{OH1}	6	DATA−OUT, I_{OH} = −1.0 mA	4.6	—	—	V
	V_{OH2}	6	DATA−OUT, I_{OH} = −1.0 μA	—	V_{DD}	—	
Low Output Voltage for Logic Circuits	V_{OL1}	6	DATA−OUT, I_{OL} = 1.0 mA	—	—	0.4	V
	V_{OL2}	6	DATA−OUT, I_{OH} = 1.0 μA	—	0.1	—	
Clock Frequency	f_{CLK}	6	CASCADE CONNECTED, Ta = −40~85°C	10	—	—	MHz

SWITCHING CHARACTERISTICS

(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	Test Cir−cuit	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D−IN−CLOCK)	t_{DHO}	—	—	—	10	—	ns
Data Setup Time (D−IN−CLOCK)	t_{DST}	—	—	—	20	—	ns
Serial Output Delay Time (CLOCK−D−OUT)	t_{PDSO}	—	C_L = 10 pF	—	25	—	ns
High Clock Pulse Width	t_{CKH}	—	—	—	30	—	ns
Low Clock Pulse Width	t_{CKL}	—	—	—	30	—	ns
Load Pulse Width	t_{wLD}	—	—	—	100	—	ns
Load Clock Time (CLOCK−LOAD)	t_{CLK-LD}	—	—	—	50	—	ns
Clock Load Time (LOAD−CLOCK)	t_{LD-CLK}	—	—	—	50	—	ns
OUT−C_0 to OUT−C_6 Output Delay Time (LOAD−OUT−C_n)	t_{PD} CO	—	C_L = 10 pF	—	—	5.0	μs
OUT−C_0 to OUT−C_6 Output Rise Time(OUT−C_n)	t_r CO	—	C_L = 10 pF	0.2	1.0	—	μs
OUT−C_0 to OUT−C_6 Output Fall Time (OUT−C_n)	t_f CO	—	C_L = 10 pF	0.2	1.0	—	μs
OUT−R_0 to OUT−R_4 Output Delay Time (LOAD−OUT−Rn)	t_{PD} RO	—	C_L = 10 pF	—	—	10.0	μs
OUT−R_0 to OUT−R_4 Output Rise Time (OUT−R_n)	t_r RO	—	C_L = 10 pF	0.4	2.0	—	μs
OUT−R_0 to OUT−R_4 Output Fall Time (OUT−R_n)	t_f RO		C_L = 10 pF	0.4	2.0	—	μs

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, Ta = −40 to 85°C)

CHARACTERISTIC	SYMBOL	Test Cir−cuit	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Output Block	V_{CC}	—	—	4.0	—	15.0	V
OUT−R_0 to R_4 Output Source Current	I_{CO}	—	V_{OUT} = 3.0 V	—	—	−280	mA
OUT−C_0 to C_6 Output Sink Current	I_{RO}	—	V_{CE} = 0.7 V	—	—	50	mA

Logic block

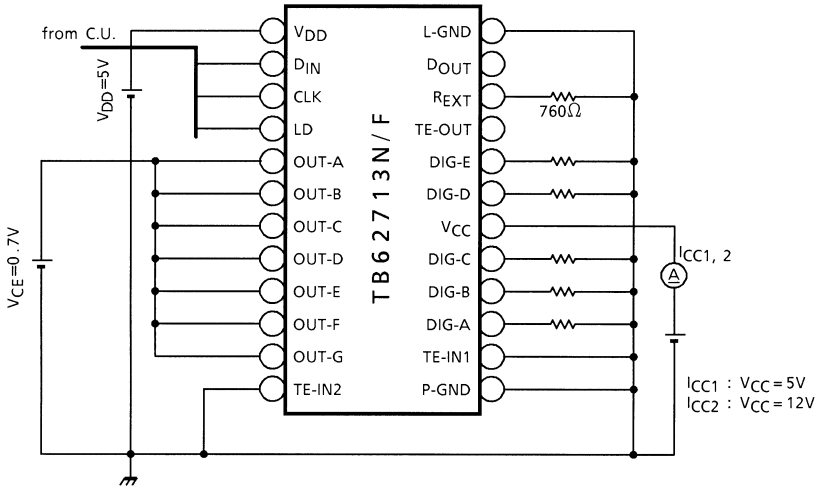
CHARACTERISTIC	SYMBOL	Test Cir−cuit	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Logic Block	V_{DD}	—	—	4.5	—	5.5	V
High Input Current for Logic Circuits	I_{IH}	—	DATA−IN, LOAD & CLOCK, V_{IN} = V_{DD}	—	—	1	μA
Low Input Current for Logic Circuits	I_{IL}	—	DATA−IN, LOAD & CLOCK, V_{IN} = 0 V	—	—	−1	μA
High Input Voltage for Logic Circuits	V_{IH}	—	—	0.7 V_{DD}	—	—	V
Low Input Voltage for Logic Circuits	V_{IL}	—	—	—	—	0.3 V_{DD}	V

SWITCHING CONDITIONS

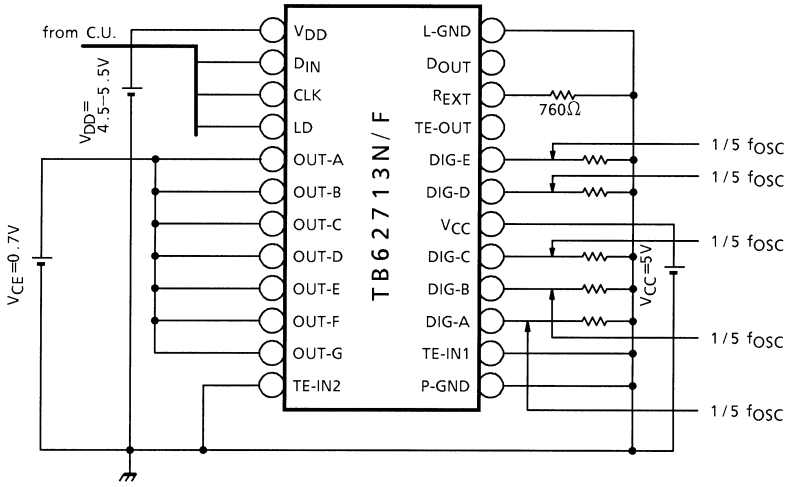
CHARACTERISTIC	SYMBOL	Test Cir−cuit	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D−IN−CLOCK)	t_{DHO}	—	—	30	—	—	ns
Data Setup Time (D−IN−CLOCK)	t_{DST}	—	—	50	—	—	ns
Serial Output Delay Time (CLOCK−D−OUT)	t_{PDSO}	—	C_L = 10 pF	50	—	—	ns
High Clock Pulse Width	t_{CKH}	—	—	30	—	—	ns
Low Clock Pulse Width	t_{CKL}	—	—	30	—	—	ns
Load Pulse Width	t_{wLD}	—	—	150	—	—	ns
Load Clock Time (CLOCK−LOAD)	t_{CLKLD}	—	—	100	—	—	ns
Clock Load Time (LOAD−CLOCK)	t_{LDCLK}	—	—	100	—	—	ns

TEST CIRCUITS

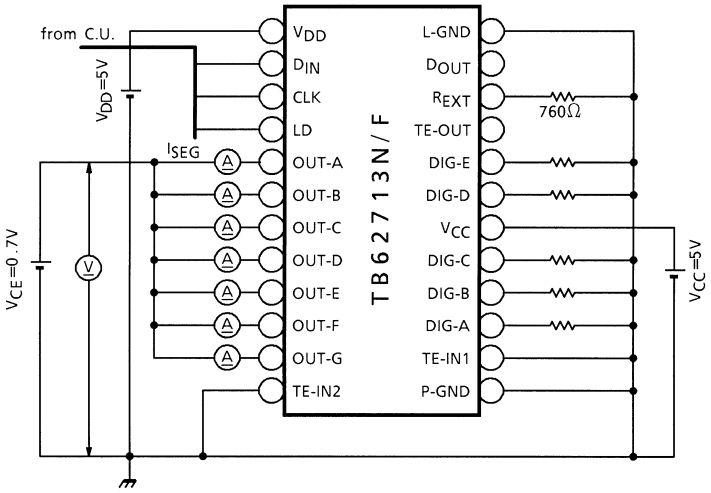
(1) I_{CC1}, I_{CC2}



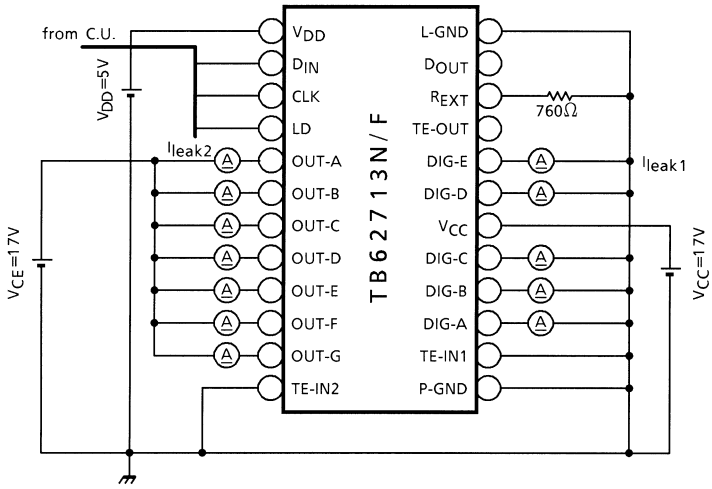
(2) f_{OSC}



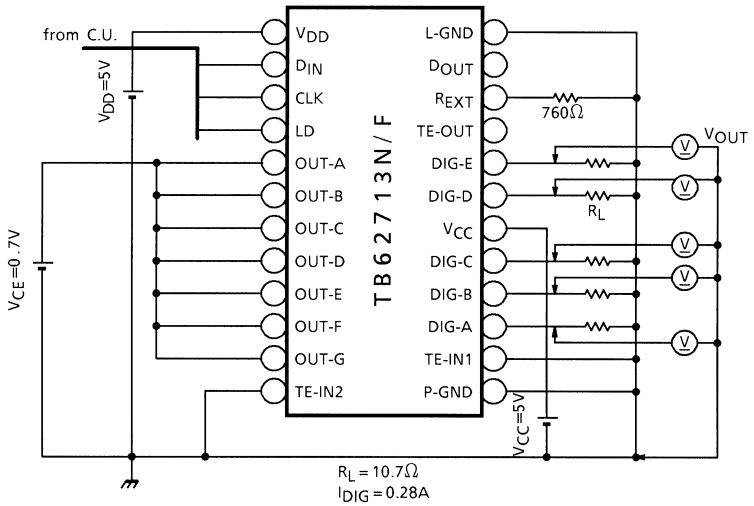
(3) I_{SEG}



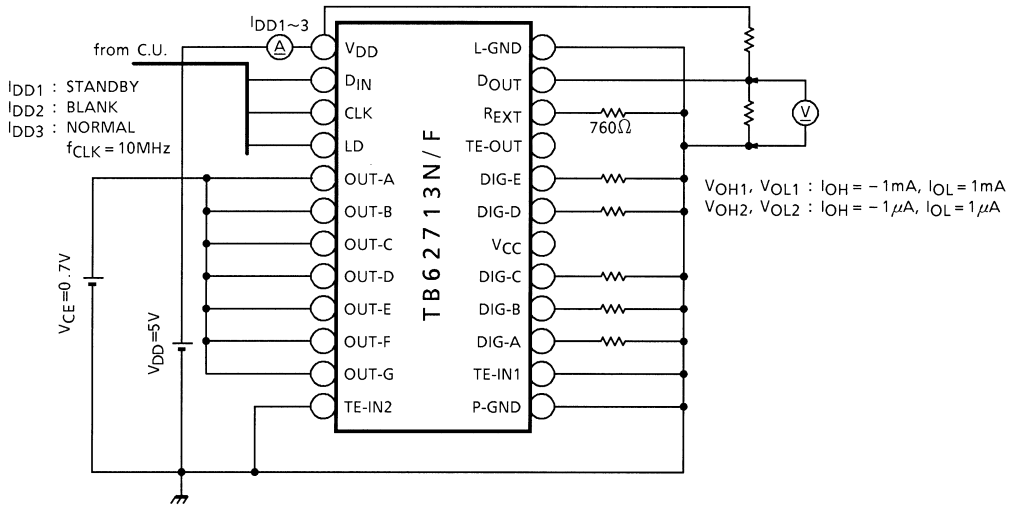
(4) I_{leak1}, I_{leak2}



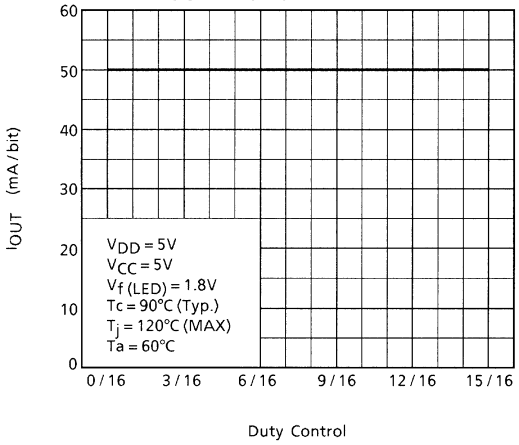
(5) V_{OUT}



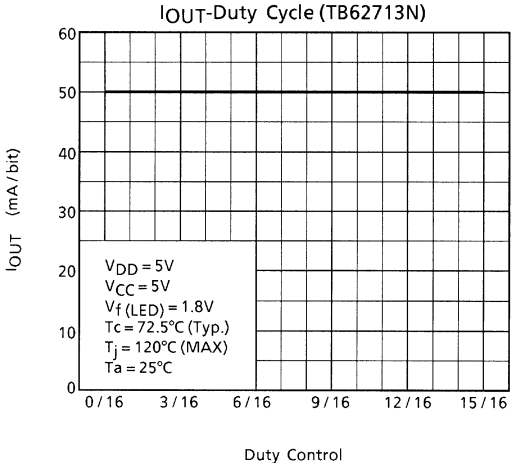
(6) I_{DD1}, I_{DD2}, I_{DD3}, V_{OH1}, V_{OH2}, V_{OL1}, V_{OL2}, f_{CLK}



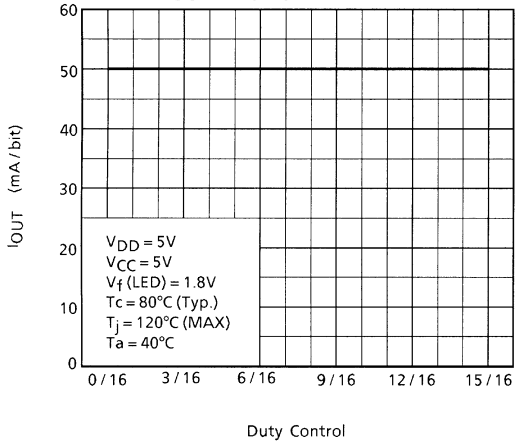
I_{OUT}-Duty Cycle (TB62713N)



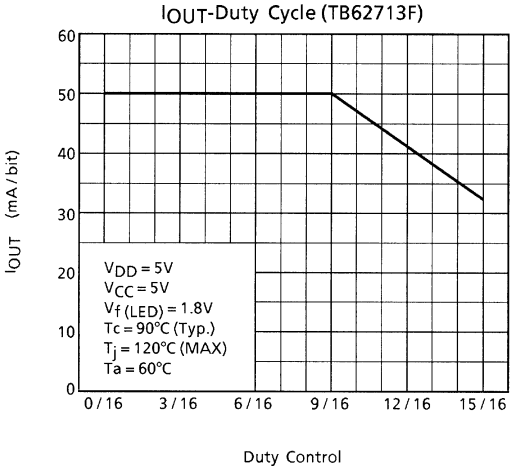
I_{OUT}-Duty Cycle (TB62713N)



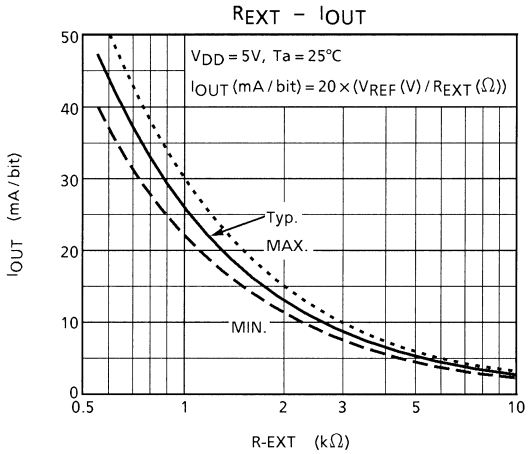
I_{OUT}-Duty Cycle (TB62713F)



I_{OUT}-Duty Cycle (TB62713F)

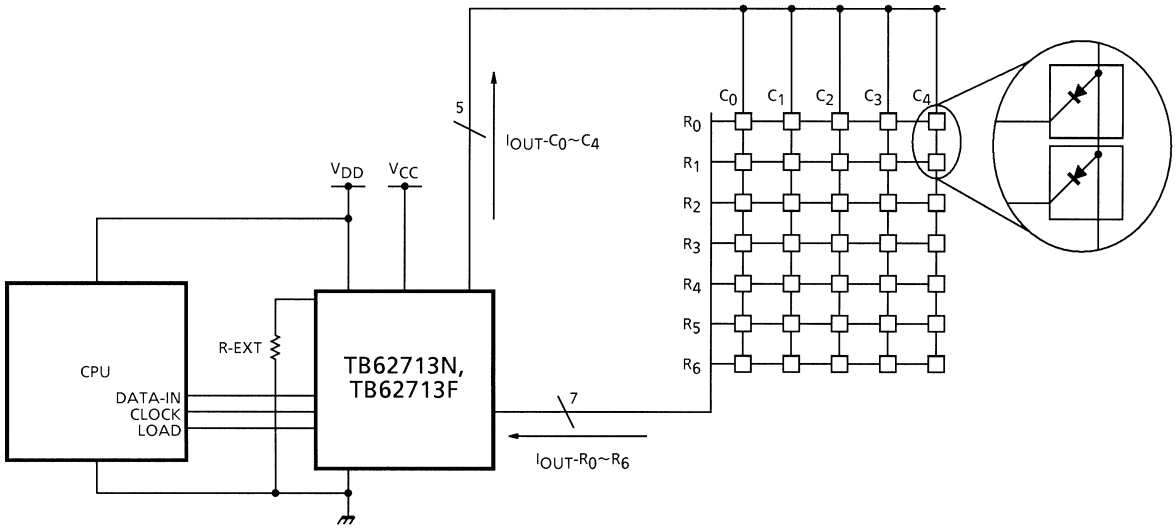


EXTERNAL RESISTANCE AND OUTPUT CURRENT VALUES



The following diagram shows the application circuit.
Because operation may be unstable due to influences such as the electromagnetic induction of the wiring, the IC should be located as close as possible to the LED.
The L−GND and P−GND of this IC are connected to the substrate in the IC.
Take care to avoid a potential difference exceeding 0.4 V at two pins.
When executing the pattern layout, Toshiba recommends not including inductance components in the GND or output pin lines, and not inserting capacitance components exceeding 50 pF between the R_{EXT} pin and GND.

APPLICATION CIRCUIT EXAMPLE (Connection example)

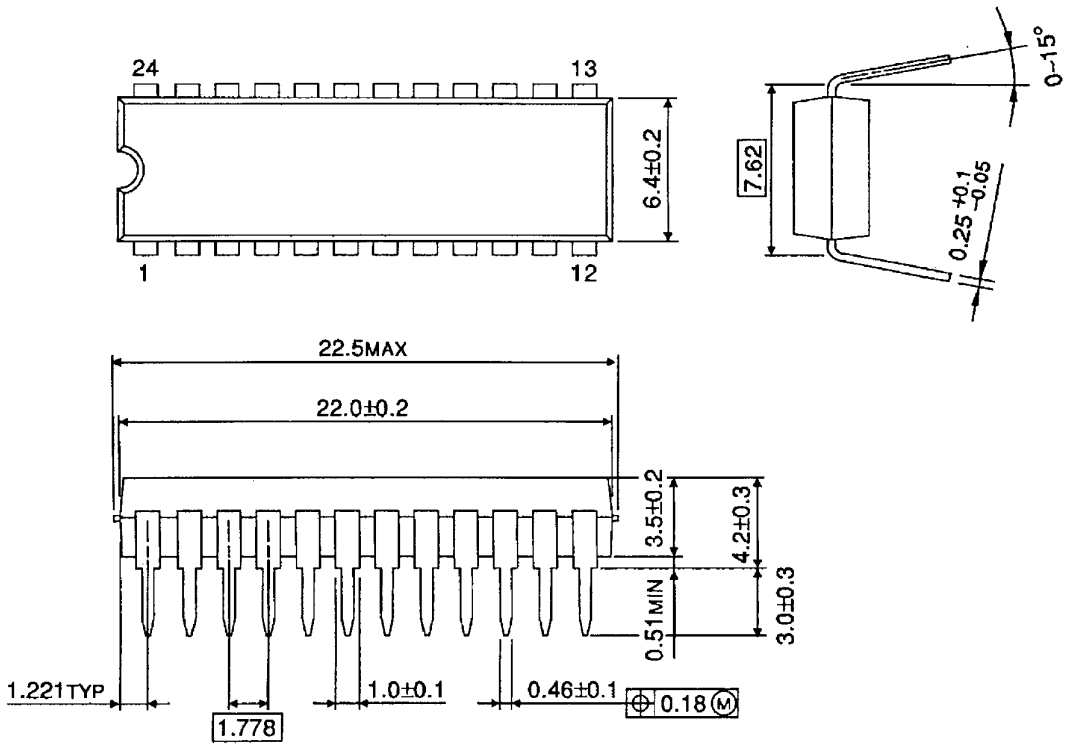


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L−GND, P−GND) line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

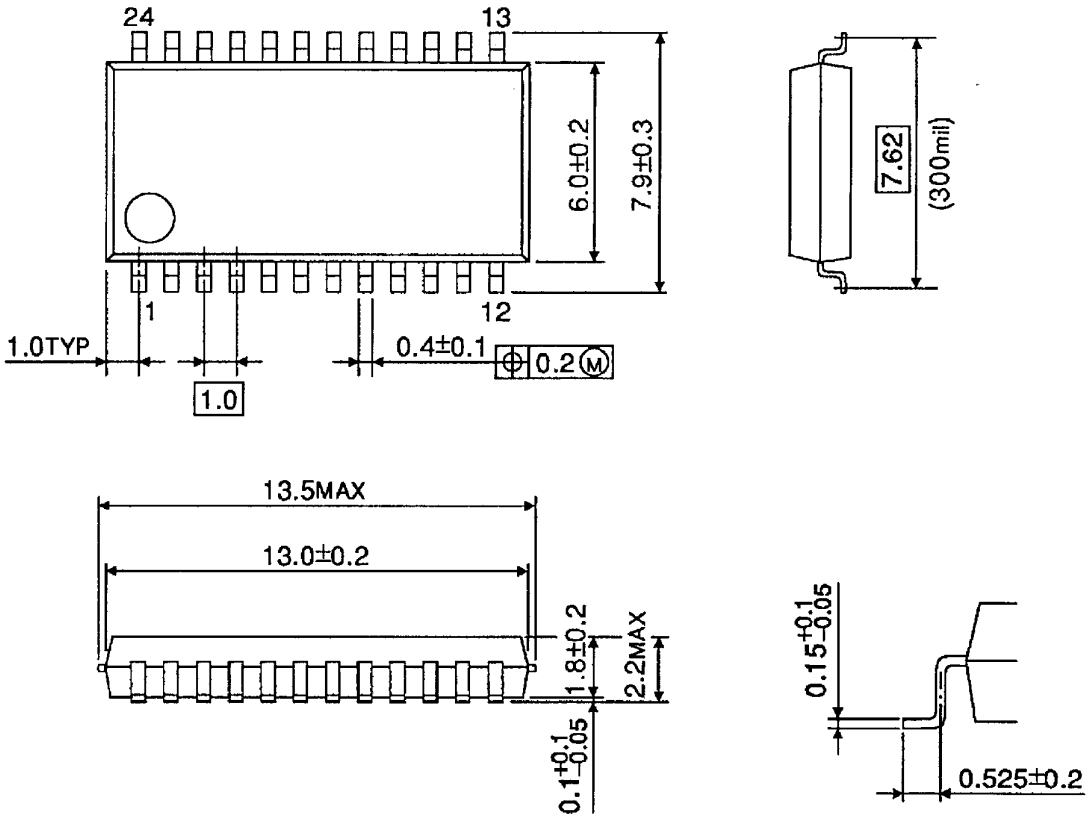
SDIP24-P-300-1.78 Unit : mm



Weight: 1.62 g (typ.)

Package Dimensions

SSOP24-P-300-1.00 Unit : mm



Weight: 0.32 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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