TB77-Series

Low Voltage Detectors(V_{DF}=1.5V~5.5V)

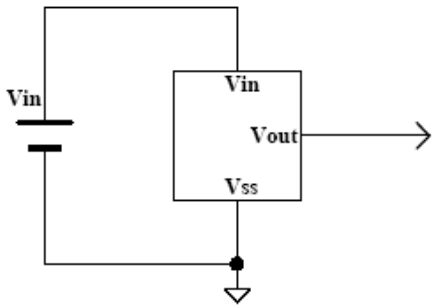
CMOS
Highly Accurate : ± 2%
Low Power Consumption : 0.8μA (VIN = 1.5V)
Ultra small SOT-23 Package

General Description

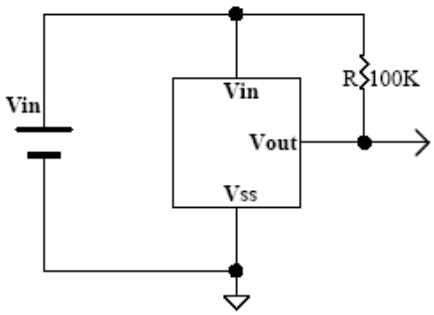
The **TB77** series are highly precise, low power consumption voltage
detectors, manufactured using CMOS and poly fuse technologies.
Detect voltage is extremely accurate with minimal temperature drift.
Both CMOS and N-channel open drain output configurations are
available.

※**Highly accurate**：± 2%
※**Low power consumption**
：TYP 0.8 μA [VIN=1.5V]
※**Detect voltage range**
：1.5V ~ 5.5V in 0.1V increments
※**Operating voltage range** : 1.2V ~ 6.0V
※**Detect voltage temperature characteristics**
：TYP± 100ppm/°C
※**Output configuration**
：N-channel open drain or CMOS
※**Ultra small package**
：SOT-23 (150mW) mini-mold
SOT-89 (500mW) mini-power mold

Typical Application Circuits

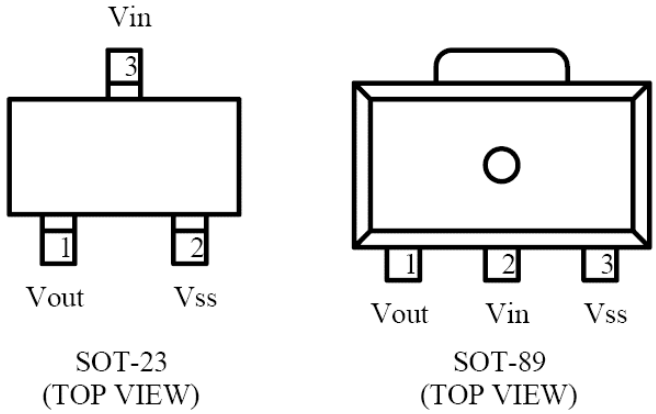


CMOS Output



N-ch Open Drain Output

Pin Configuration



SOT-23
(TOP VIEW)

SOT-89
(TOP VIEW)

Pin Assignment

Pin Number		Pin Name	Function
SOT-23	SOT-89		
3	2	V_{IN}	Supply Voltage
2	3	V_{SS}	Ground
1	1	V_{OUT}	Output

Product Classification

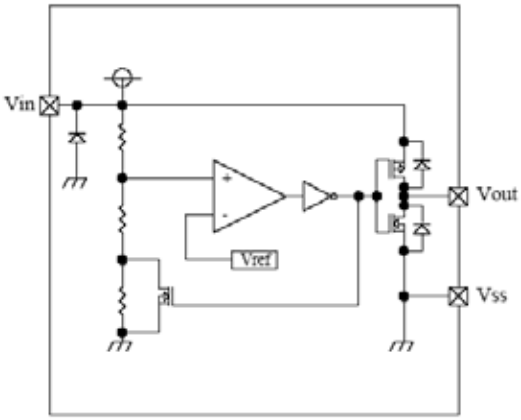
Ordering Information

TB77 XX X X
a b c

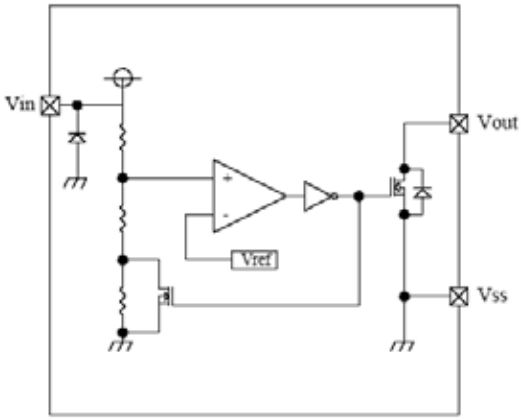
Designator	**Description**
a	**Detect Voltage** **15 = 1.5V** **:** **55 = 5.5V**
b	**C = COMS** **N = N-ch** **(open dirain)**
C	**Package Type** **A = SOT-23** **B = SOT-89**

Block Diagram

(1) CMOS Output



(2) N-ch Open Drain Output



Absolute Maximum Ratings

Ta = 25℃

Parameter		Symbol	Ratings	Units
Input Voltage		Vin	9	V
Output Current		Iout	50	mA
Output Voltage	CMOS	Vout	Vss-0.3 ~ Vin+0.3	V
	N-ch open drain		Vss-0.3 ~ 9.0	
Power Dissipation	SOT-23	Pd	150	mA
	SOT-89		500	
Operating Ambient Temperature		Topr	-40 ~ +85	℃
Storage Temperature		Tstg	-40 ~ +125	℃

Electrical Characteristics

T =25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Detection Voltage	V_{DET}		V_{DET} x 0.98	V_{DET}	V_{DET} x 1.02	V
Hysteresis Voltage Range	V_{HYS}		V_{DET} x 0.02	V_{DET} x 0.05	V_{DET} x 0.09	V
Supply Current	I_{SS}	Vin = 1.5V Vin = 2.0V Vin = 3.0V Vin = 4.0V Vin = 5.0V Vin = 6.0V	- - - - - -	0.8 0.9 1.0 1.1 1.2 1.3	2.4 2.4 2.4 2.4 2.4 2.7	uA
Operating Voltage	V_{IN}		1.2		6	V
Output Current	I_{OUT}	N-ch V_{DS}=0.5V Vin=1.5V	-	2.8		mA
		P-ch V_{DS}=2.1V Vin=6.0V (with CMOS output)		8		
Detection Voltage Temperature Coefficient		T = -40°C to 85°C		±100		ppm/°C
Response Time	t_{DLY}				200	nS

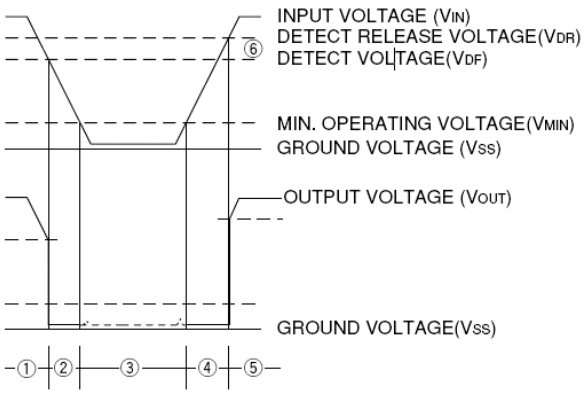
Note :
VDF (T) : Established Detect Voltage Value
Release Voltage : VDR = VDF + VHYS

Functional Description

Functional Description (CMOS output)

1. When input voltage (VIN) rises above detect voltage (VDF), output voltage (VOUT) will be equal to VIN. (A condition of high impedance exists with N-ch open drain output configurations.)
2. When input voltage (VIN) falls below detect voltage (VDF), output voltage (VOUT) will be equal to the ground voltage (VSS)level.
3. When input voltage (VIN) falls to a level below that of the minimum operating voltage (VMIN), output will become unstable.In this condition, VIN will equal the pulled-up output (should output be pulled-up.)
4. When input voltage (VIN) rises above the ground voltage (VSS) level, output will be unstable at levels below the minimumoperating voltage (VMIN). Between the VMIN and detect release voltage (VDR) levels, the ground voltage (VSS) level will be maintained.
5. When input voltage (VIN) rises above detect release voltage (VDR), output voltage (VOUT) will be equal to VIN.(A condition of high impedance exists with N-ch open drain output configurations.)
6. The difference between VDR and VDF represents the hysteresis range.

●Timing Chart



Directions for use

Notes on Use

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
5. In order to stabilise the IC's operations, please ensure that VIN pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor RIN is connected between the VIN pin and power source. In such cases, please ensure that RIN is less than 10kΩ and that C is more than 0.1μF.

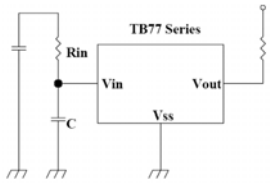


Diagram:Circuit using an input resistor

Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow at RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again. Oscillation may occur with this " release - detect - release " repetition. Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the TB77 series are CMOS IC S, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (RIN) during release voltage operations. (refer to diagram 2)
Since hysteresis exists during detect operations, oscillation is unlikely to occur.

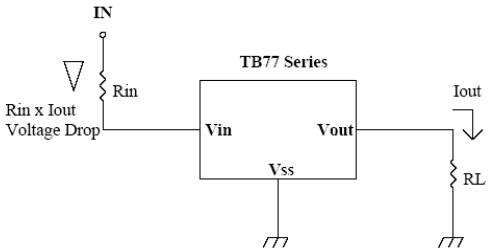


Diagram 1:Oscillation in relation to output current

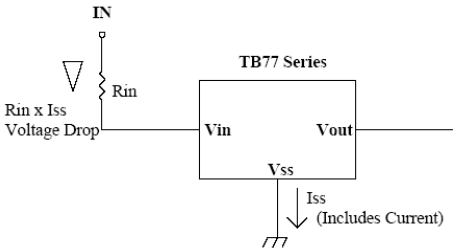
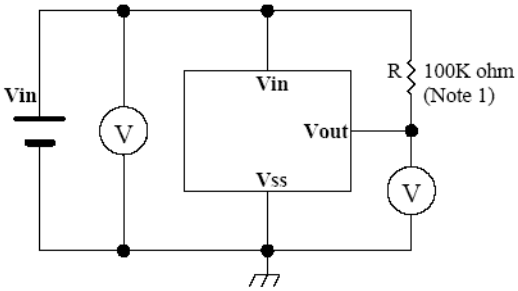


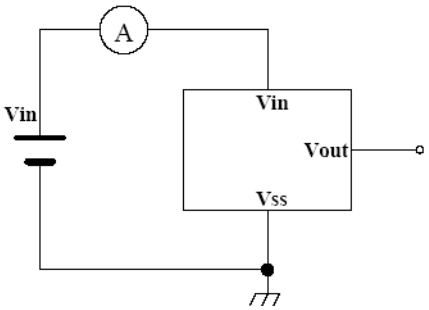
Diagram 2:Oscillation in relation to output current

Measuring Circuits

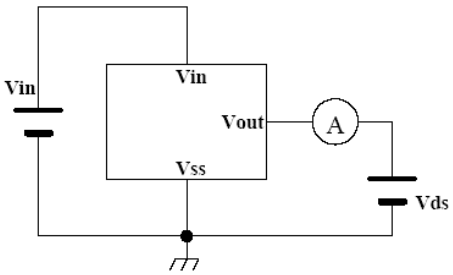
Circuit 1



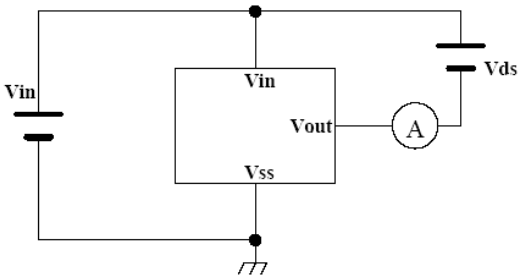
Circuit 2



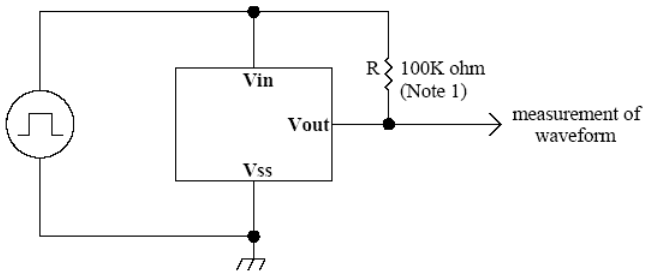
Circuit 3



Circuit 4



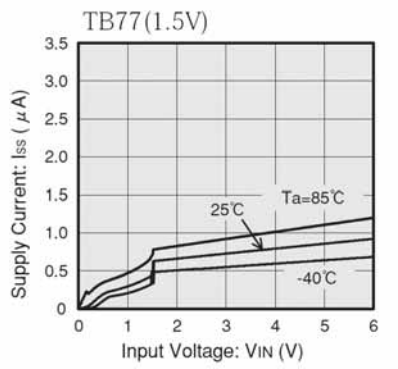
Circuit 5



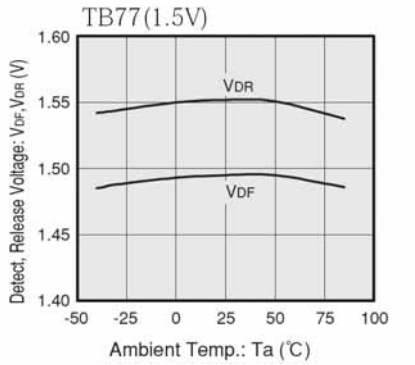
Note 1:Not necessary with CMOS output products.

Typical Performance Characteristics

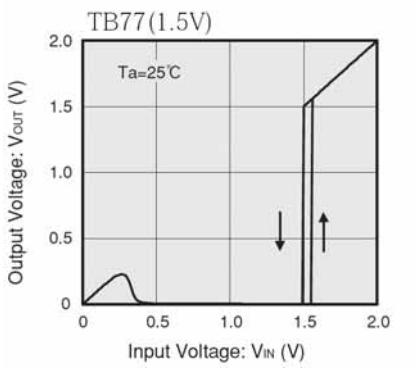
(1) SUPPLY CURRENT vs. INPUT VOLTAGE



(2) DETECT, RELEASE VOLTAGE vs. AMBIENT TEMPERATURE

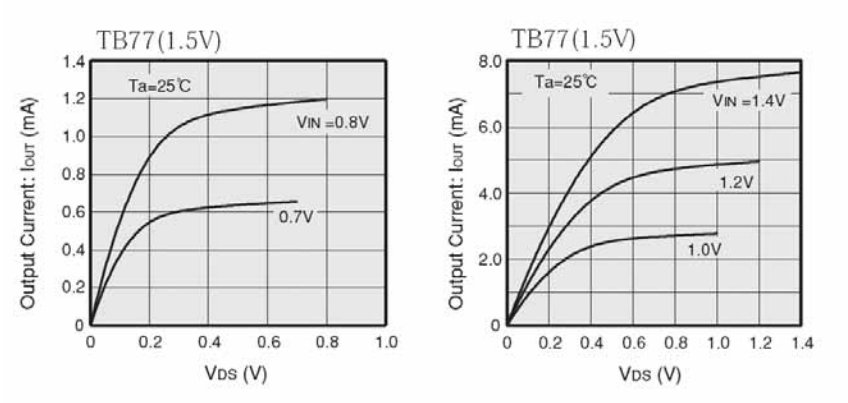


(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE

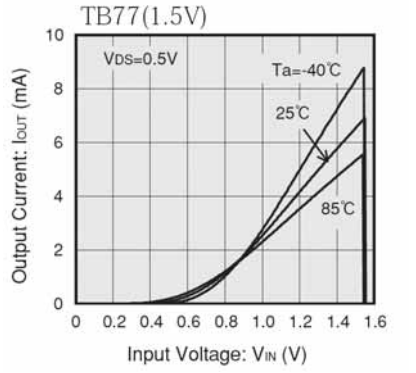


Note : The N-channel open drain pull up resistance value is 100kΩ

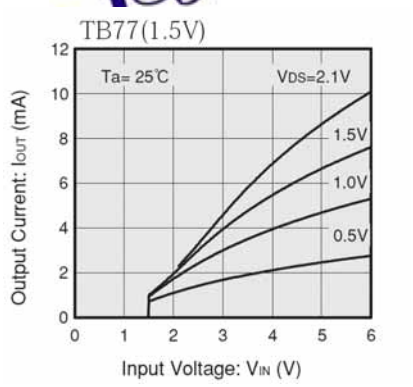
(4) N-ch DRIVER OUTPUT CURRENT vs. VDS



(5) N-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

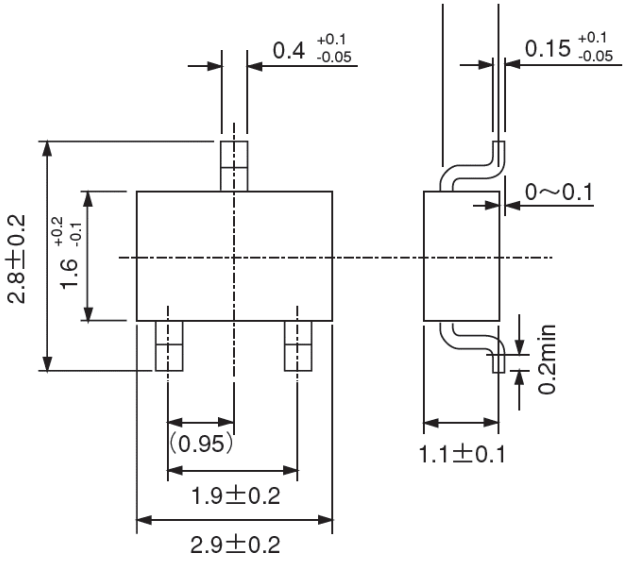


(6) P-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

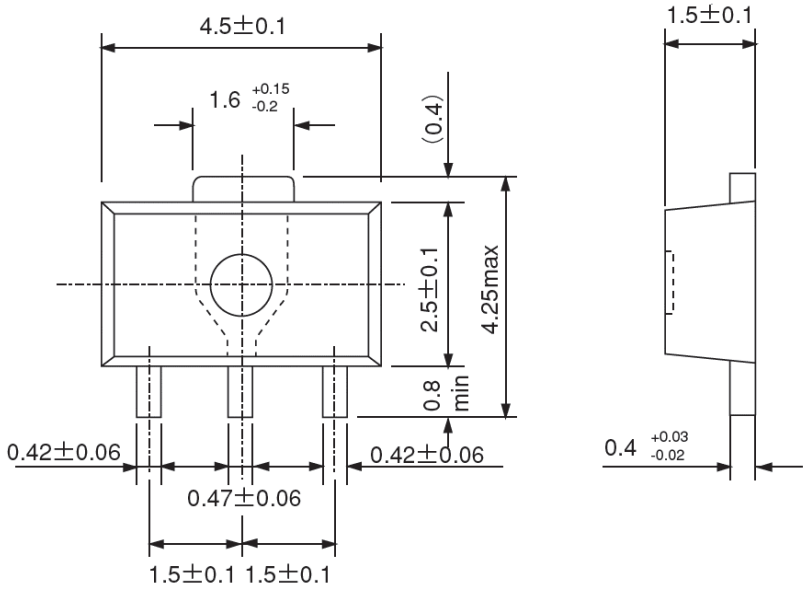


Packaging Information

SOT-23



SOT-89


4.5±0.1
1.6 +0.15 -0.2
(0.4)
2.5±0.1
4.25max
0.8 min
0.42±0.06
0.42±0.06
0.47±0.06
1.5±0.1 1.5±0.1
1.5±0.1
0.4 +0.03 -0.02