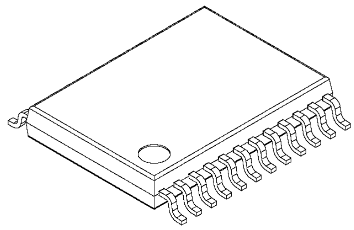
TOSHIBA Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB9102FNG

3ch H-bridge / 6ch Half-bridge driver for DC Brushed Motor

TB9102FNG is a 3chH-bridge / 6ch Half-bridge driver which is designed specifically for Automotive. 6High-side/6Low-side DMOS transistors are built-in for directly driving small DC Brushed motor. SPI interface is built-in for motor operation by external MCU. Also, miscellaneous abnormal detection such as Over Current/Over Voltage/Over Temperature are built-in. the TB9102FNG is for wide application such as for Automotive Air-condition system (Dumper control), Door Mirror control.



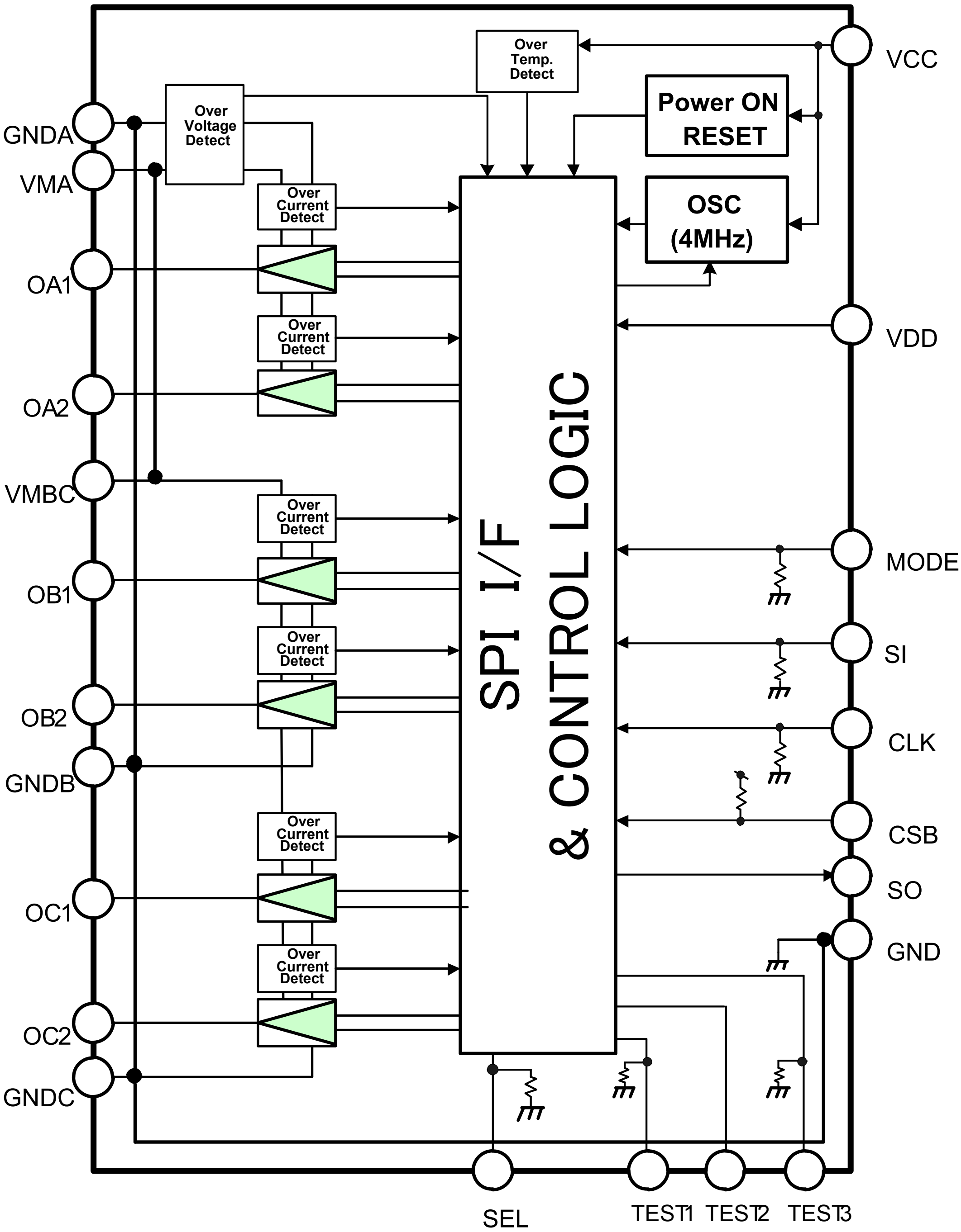
SSOP24-P-300-0.65A

Weight: 0.14 g (typ.)

Features

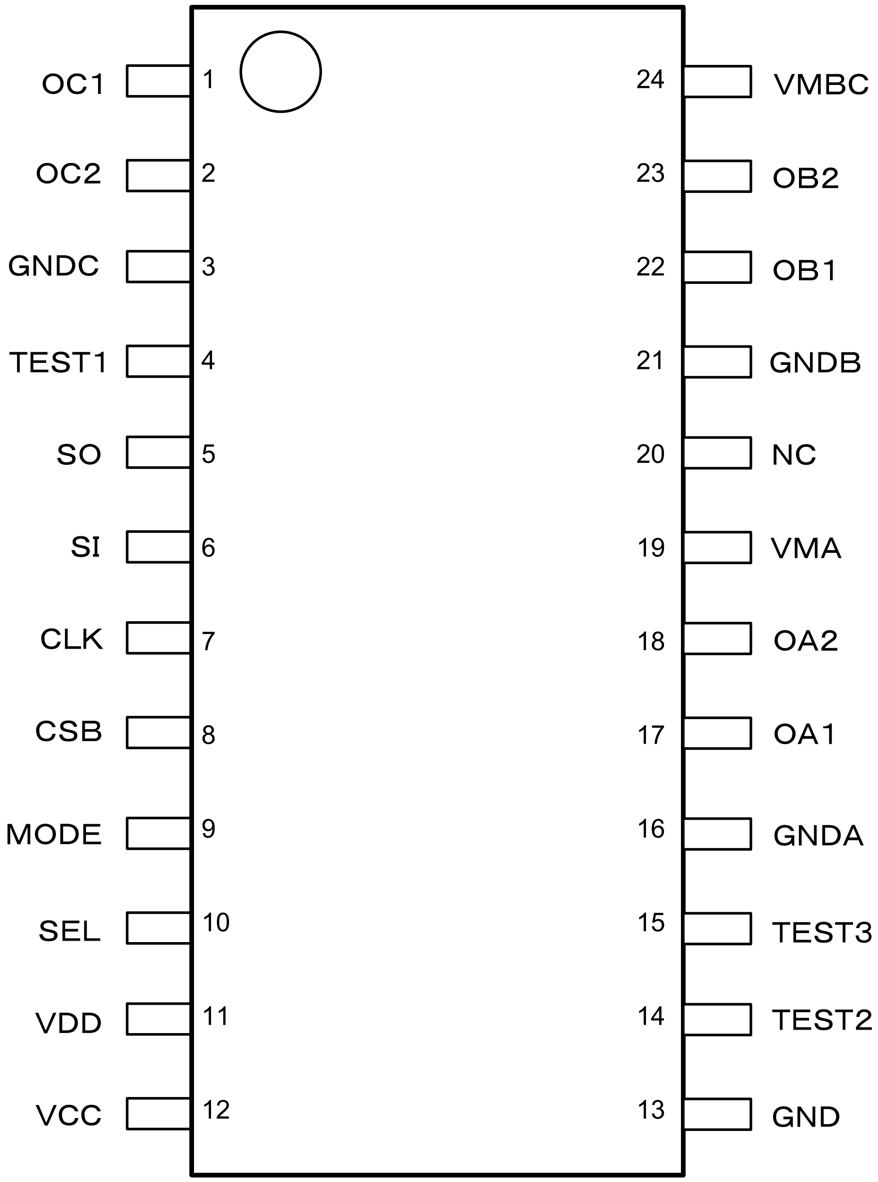
- Motor Driver : Build-in 3ch H-bridge/6ch Half-bridge (RHON=0.5Ω (typ.)/RLON=0.5Ω (typ.) at 25°C)
- External MCU I/F : SPI Interface(16Bit Shift Register, CLK,CSB)
- Abnormal detection : Over Current / Over Temperature / Over Voltage / 5V (VDD, VCC) Low Voltage Detection (Power on reset) with monitoring by SPI I/F (output)
- Operating Voltage range (VM) : 7 to 18V (Absolute maximum voltage: 40V)
- Operating Temperature range : -40 °C to 125 °C
- Package: SSOP24-P-300-0.65A
- AEC-Q100 Qualified
- The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV").

Block Diagram



Note1: Some of the functional blocks, or circuit in the block diagram may be omitted or simplified for explanatory purpose.

PIN Layout


OC1
1
OC2
2
GNDC
3
TEST1
4
SO
5
SI
6
CLK
7
CSB
8
MODE
9
SEL
10
VDD
11
VCC
12
24
VMBC
23
OB2
22
OB1
21
GNDB
20
NC
19
VMA
18
OA2
17
OA1
16
GNDA
15
TEST3
14
TEST2
13
GND

PIN Connection

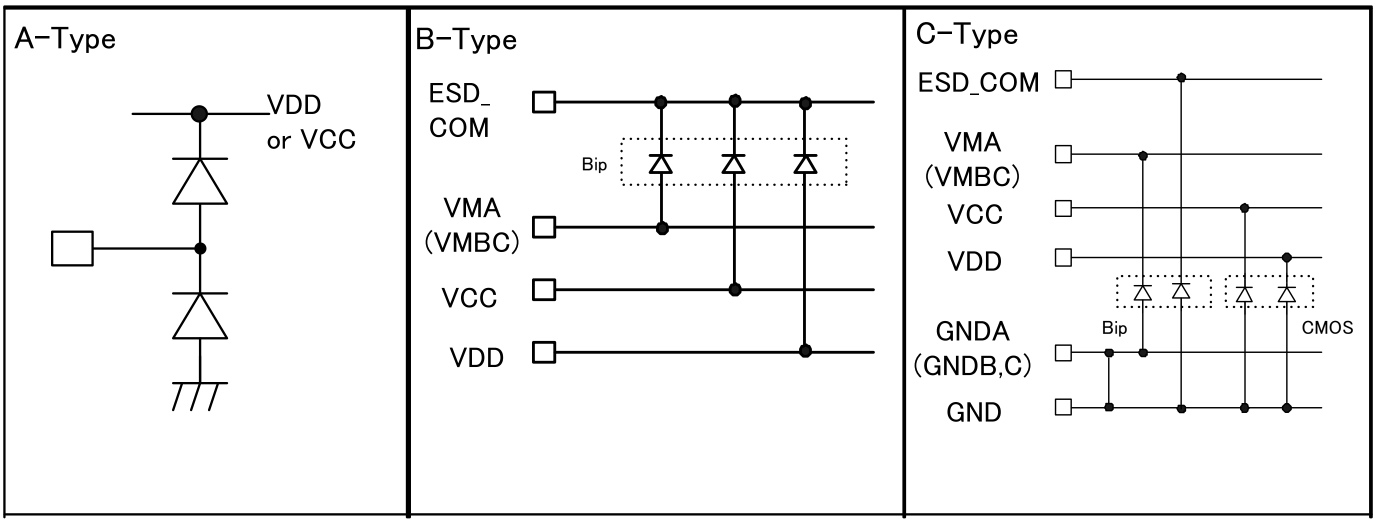
PIN No	PIN NAME	DESCRIPTION	IN / OUT	CIRCUIT	NOTE
1	OC1	Half-bridge C Out1	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
2	OC2	Half-bridge C Out2	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
3	GNDC	GND for OC1,OC2	-	-	-
4	TEST1	TEST Input Pin	IN	CMOS	Pull Down(100kΩ) Connect to GND on PCB
5	SO	SPI Output	OUT	CMOS	-
6	SI	SPI Input	IN	CMOS	Pull Down(100kΩ)
7	CLK	SPI Clock	IN	CMOS	Pull Down(100kΩ)
8	CSB	SPI CHIP Select	IN	CMOS	Pull Up(100kΩ)
9	MODE	Normal/Standby or Brake select Input	IN	CMOS	Pull Down(100kΩ)
10	SEL	Sleep Mode Control	IN	CMOS	Pull Down(100kΩ)
11	VDD	5V Input for CMOS LOGIC	VDD	-	Connect VDD and VCC on PCB
12	VCC	5V input for Bipolar	VDD	-	
13	GND	GND for 5V	-	-	-
14	TEST2	TEST Output Pin	OUT	CMOS	Keep OPEN.
15	TEST3	TEST Input Pin	IN	CMOS	Pull Down(100kΩ) Connect to GND on PCB
16	GNDA	GND for OA1,OA2	-	-	-
17	OA1	Half-bridge A Out1	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
18	OA2	Half-bridge A Out2	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
19	VMA	Power input for OA1,OA2	-	-	(Note2)
20	NC	No connection.	-	-	Keep OPEN
21	GNDB	GND for OB1,OB2	-	-	-
22	OB1	Half-bridge B Out1	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
23	OB2	Half-bridge B Out2	OUT	Bip/HVMOS (Note1)	RHON=RLON=0.5Ω(typ.)
24	VMBC	Power input for OB1,2, OC1,2	-	-	(Note2)

(Note1) HVMOS: Pch and Nch MOS which withstand voltage is the same as VMA,VMBC level

(Note2) Even if only using 1ch/2ch H-Bride (not using all 3ch H-bridge), VMA and VMBC should be connected to power supply on the board.

Internal protection circuit

PIN No.	NAME	Internal Protection circuit
1	OC1	-
2	OC2	-
3	GNDC	C-Type
4	TEST1	A-Type
5	SO	A-Type.(for VCC)
6	SI	A-Type
7	CLK	A-Type
8	CSB	A-Type
9	MODE	A-Type
10	SEL	A-Type
11	VDD	B-Type
12	VCC	B-Type
13	GND	C-Type
14	TEST2	A-Type.(for VCC)
15	TEST3	A-Type
16	GNDA	C-Type
17	OA1	-
18	OA2	-
19	VMA	B-Type
20	NC	-
21	GNDB	C-Type
22	OB1	-
23	OB2	-
24	VMBC	B-Type



Note1: VMA and VMBC are short-circuited internally.

Note2: GNDA, GNDB, GNDC and GND are short-circuited internally.

Functional Description

The TB9102FNG is a motor controller IC incorporating output driver, which is designed to operate brushed small DC motor for automotive directly. It can be used as a 3ch H-bridge driver or a 6ch Half-bridge driver. The motor control signal is inputted from the external MCU through SPI I/F. And the signals of various abnormal detections such as over current detection, thermal shutdown circuit, over voltage detection, and 5V-under voltage detection are outputted.

(1) SPI Interface control

The TB9102FNG has the SPI interface to control the motor by the external MCU. In SPI mode, input data is stored to 16 Bit Shift register in synchronizing with the falling edge of CLK (clock). And the data is outputted from SO terminal in synchronizing with the rising edge of CLK.
The detail is as follows.

(1)-1. SPI Communication

CSB: When “L” signal is inputted from external device, SPI communication is enable. Then, input signal of “CLK” and “SI” can be read internally and data of SPI Status register Bit 15 is outputted from the output SO. (1st bit is “Bit15”) When “CSB” is configured “L” to “H”, the data of SPI Receive Register latching 16 Bit data inputted from SI at the rising edge is transferred to the internal SPI Status register. Then, each data of Bit 1 to Bit 12 is outputted from each motor output terminal as a motor output signal. While “CSB” is “H”, “SO” is Hi-Z.

CLK: “CLK” is a clock terminal for SPI data communication which is inputted from external master device. SPI data is outputted from SO in synchronizing with the rising edge of CLK and read from SI in synchronizing with the falling edge of CLK.

SI: “SI” is a data input terminal for SPI communication which is inputted from external master device. Input data is read at the falling edge of “CLK”. Thus, the IC changes the SPI input data at the rising edge of “CLK”.

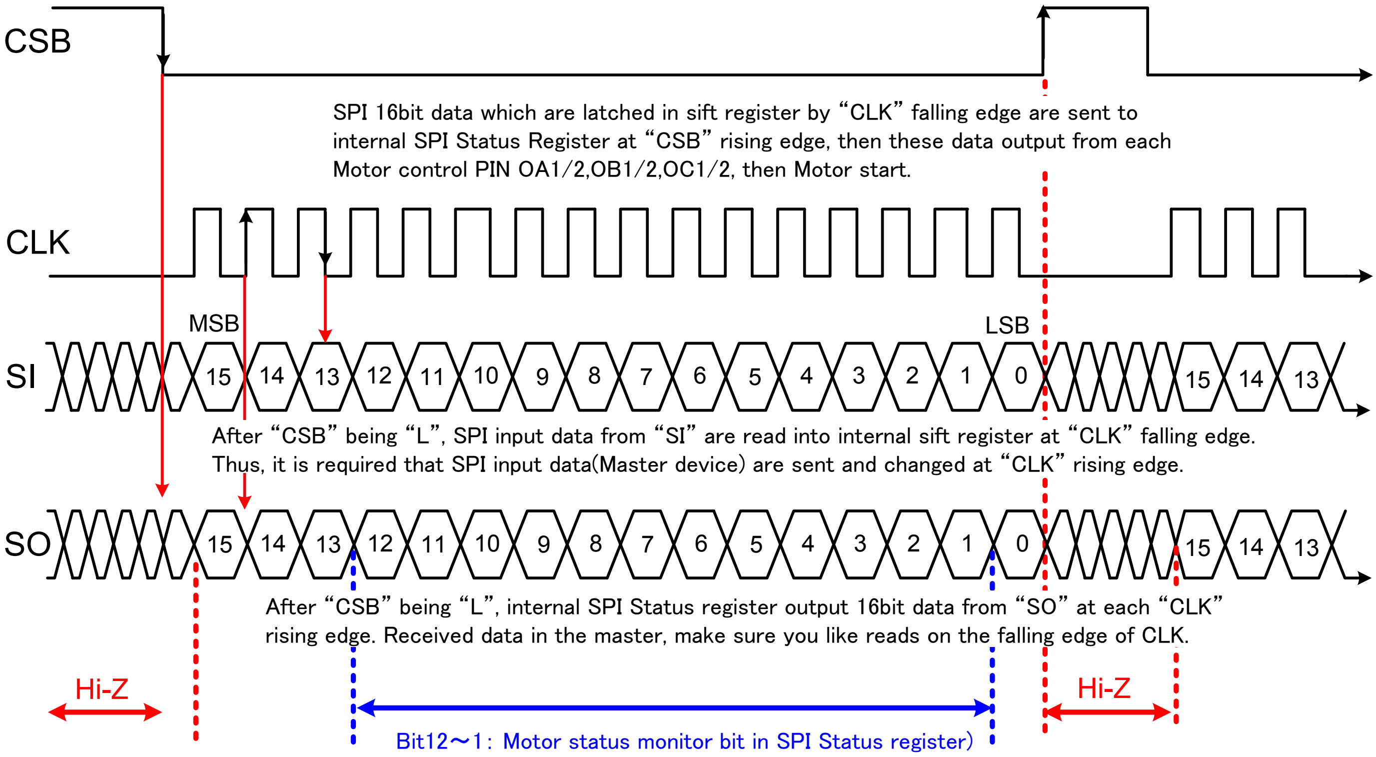
SO: “SO” is a output terminal for SPI data communication which is read by external master device. While “CSB” is “H”, ”SO” is Hi-Z. When “CBS” is “L”, data of Bit0 to Bit15 of the internal SPI Status register are outputted in synchronizing with the rising edge of the inputted clock from CLK. After that, data is switched at the rising edge of CLK and outputted from “SO”.

○ SPI DATA bit length error

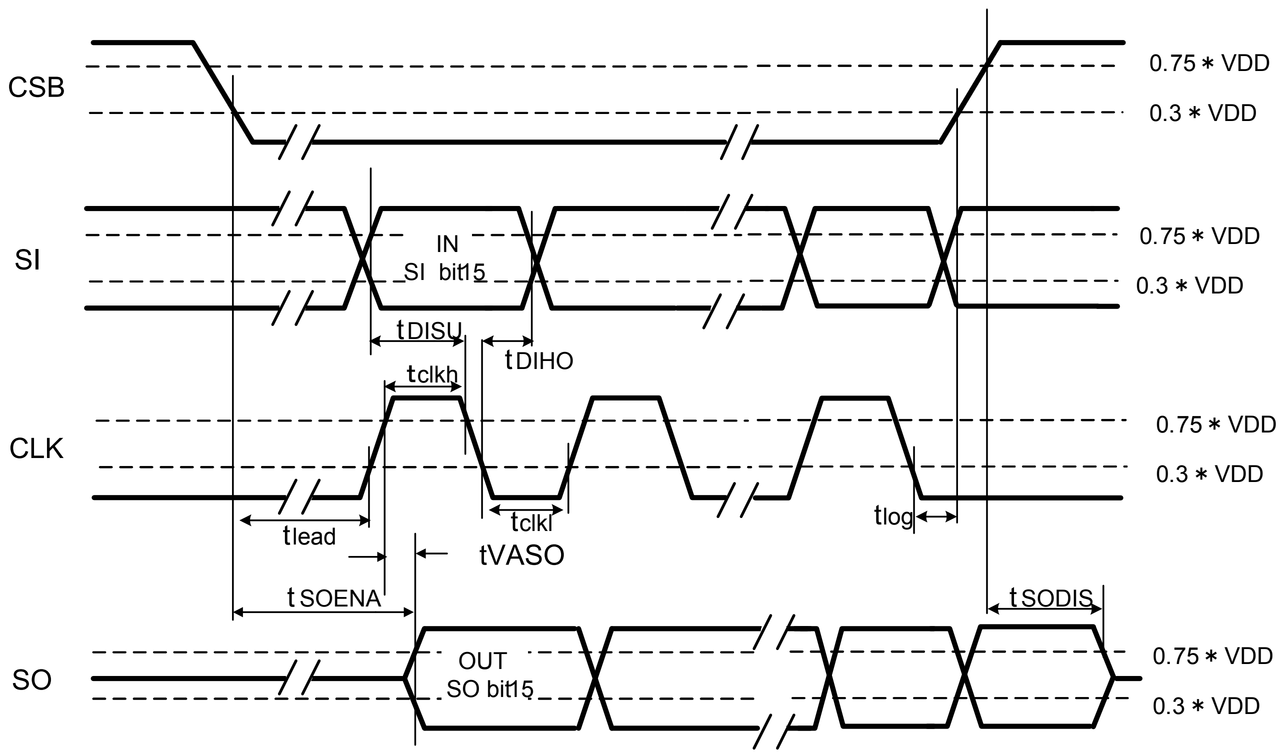
When inappropriate length of data (more than 17 bits or less than 15 bits) are inputted because of the communication error from MCU, all data of this cycle of this timing are ignored.
Sending and receiving data error should be detected by the master side, if necessary, and should be treated appropriately.

(1)-2. SPI Communication protocol timing

When “CSB” is changed H to L, SPI Communication of TB9102FNG is enable ,read Input ”SI” and “CLK”, and then outputs a predetermined data of SPI Status register from the output. (When “CSB” is “H”, SO is off (Hi-Z)



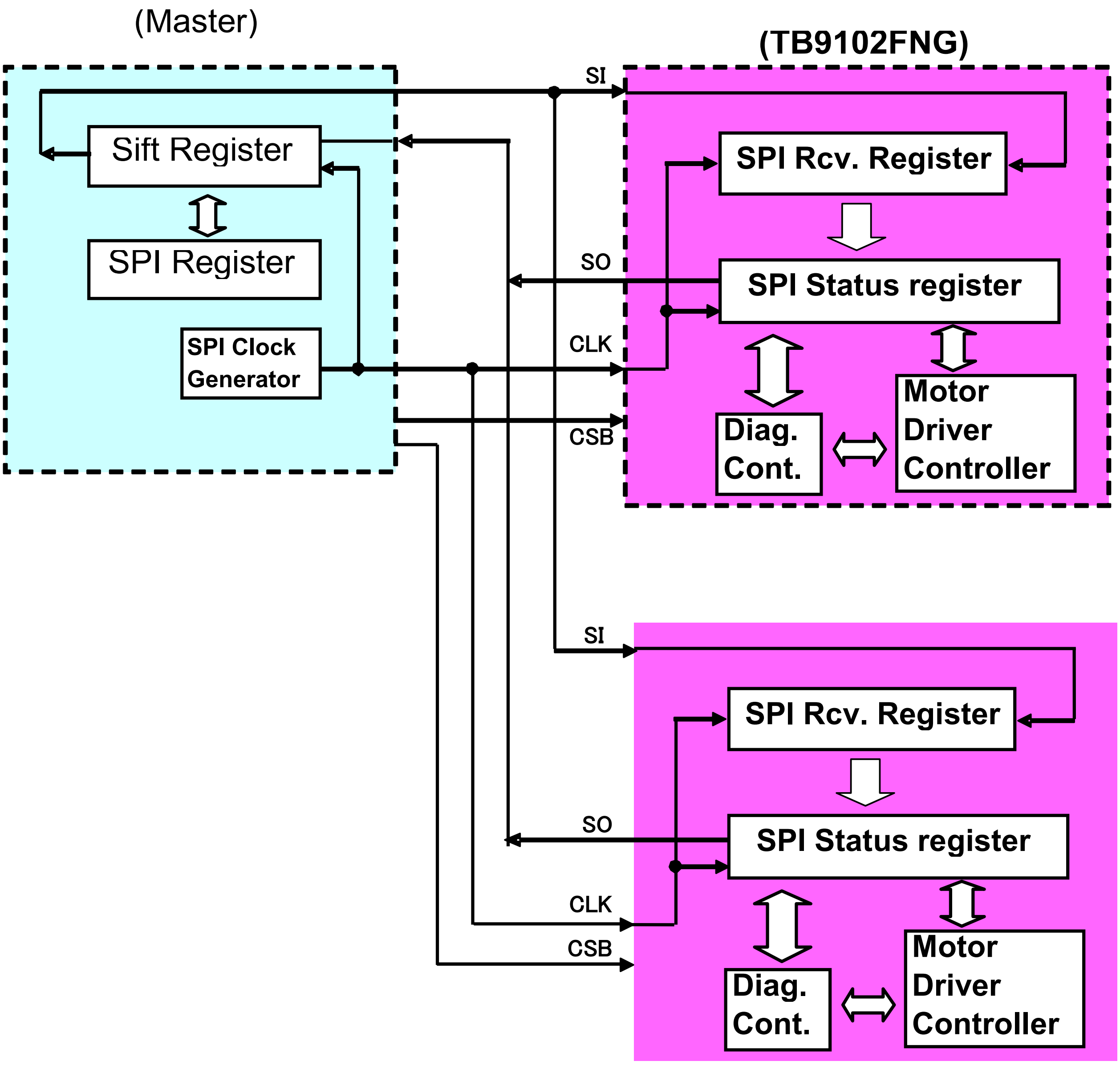
(1)-3. SPI Communication timing chart



(Note)Timing charts may be simplified for explanatory purpose.

(1)-4. SPI Connection (Example)

More than two ICs can be controlled by connecting them as below figure and controlling “CSB” signal of each IC.



(1)-5. SPI SI/SO Bit explanation

SI				SO			
Bit	Name	Initial	Notes	Bit	Name	Initial	Notes
15	OVreset	L	**H**: Over voltage flag in SPI Status register is reset and the operations of all motor outputs, which are turned off forcedly by the over voltage detection, are returned to normal. However, in case the operations are normalized before the address of "H" is inputted, each motor output has been already returned to normal. By configuring both Bit0 and Bit15 ”H”, internal SPI Status register is reset at the rising edge of “CSB”. **L**: (No operation)	15	VMfail	L	When the over voltage detection (26V (typ.)) operates for the power supply of H-bridge A (VMA), “H” is outputted from the bit. Even if VMA returns to the normal voltage (25.5 V (typ.)), the bit keeps”H” until it is reset by SPI “SI”Bit15 or Bit0/15.
14	OTreset	L	**H**: Over temperature flag in SPI Status register is reset and the operations of all motor outputs, which are turned off forcedly by the thermal shutdown circuit, are returned to normal. However, in case the operations are normalized before the address of "H" is inputted, each motor output has been already returned to normal. **L**: (No operation)	14	OTfail	L	When the thermal shutdown circuit (170°C(typ.)) operates, “H” is outputted from the bit. Even if the temperature returns to the normal value (160°C(typ.)), the bit keeps ”H” until it is reset by SPI “SI”Bit14 or Bit0/15.
13	OCreset	L	**H**: Over current flag in SPI Status register is reset and the operations of all motor outputs, which are turned off forcedly by the over current detection, are returned to normal.	13	OCfail	L	When the over current detection (1.5 A (typ.)) operates, “H” is outputted from the bit. Once the over current detection operates, the bit keeps”H” until it is reset by SPI “SI”Bit13 (OCreset) or Bit0/15.
12	C2Lcont.	L	Half-bridge C2 Low-side SW cont.	12	C2Lst	L	Half-bridge C2 Low-side SW status
11	C2Hcont.	L	Half-bridge C2 High-side SW cont.	11	C2Hst	L	Half-bridge C2 High-side SW status
10	C1Lcont.	L	Half-bridge C1 Low-side SW cont.	10	C1Lst	L	Half-bridge C1 Low-side SW status
9	C1Hcont.	L	Half-bridge C1 High-side SW cont.	9	C1Hst	L	Half-bridge C1 High-side SW status
8	B2Lcont.	L	Half-bridge B2 Low-side SW cont.	8	B2Lst	L	Half-bridge B2 Low-side SW status
7	B2Hcont.	L	Half-bridge B2 High-side SW cont.	7	B2Hst	L	Half-bridge B2 High-side SW status
6	B1Lcont.	L	Half-bridge B1 Low-side SW cont.	6	B1Lst	L	Half-bridge B1 Low-side SW status
5	B1Hcont.	L	Half-bridge B1 High-side SW cont.	5	B1Hst	L	Half-bridge B1 High-side SW status
4	A2Lcont.	L	Half-bridge A2 Low-side SW cont.	4	A2Lst	L	Half-bridge A2 Low-side SW status
3	A2Hcont.	L	Half-bridge A2 High-side SW cont.	3	A2Hst	L	Half-bridge A2 High-side SW status
2	A1Lcont.	L	Half-bridge A1 Low-side SW cont.	2	A1Lst	L	Half-bridge A1 Low-side SW status
1	A1Hcont	L	Half-bridge A1 High-side SW cont.	1	A1Hst	L	Half-bridge A1 High-side SW status
0	STreset1	L	**H**: By configuring both Bit0 and Bit15 ”H”, internal SPI Status register is reset at the rising edge of “CSB”. **L**: (No operation)	0	(nop)	L	(No operation and keep”L”)

(SPI Input: SI)

Input data from SI terminal by SPI communication is read to the internal IC at the rising edge of the CSB signal, and it is reflected on each function.

Bit0 (STreset1) / Bit15 (OVreset):

H**:** To avoid malfunction by noise, data of SPI Status register is reset by combining Bit0 and Bit15. When only Bit0 reads “H”, any function is invalid. By resetting SPI Status register, each resulting flag of abnormal detection in this resister is also reset. And the driving outputs of the motor, which were turned off forcedly by the abnormal detection, are returned to the normal operation. In case SPI Status register is reset, data of motor operation should be configured again because all driving outputs of each motor become Hi-Z.

In resetting SPI Status register by Bit0 and Bit15, data of other bits of SI inputs sent at the same timing (Bit1 to Bit12) are ignored. So, motor outputs should be configured at the next SPI transmission after resetting SPI Status register by STreset.

L**:** No operation.

Bit1 to Bit12 (A1Hcont. to C2Lcont) :

On and Off of 12 transistors, which consists 3ch H-bridge and 6ch Half-bridge, are controlled. When “H” level is inputted, the transistor which is controlled by the bit is turned on. When both High-side transistor and Low-side transistor are turned on by the same Half-bridge, the Half-bridge output becomes Hi-Z forcedly.

(Ex)

SI Bit 1=“H”	**:** Half-bridge A1 H-side		Tr ON
=“L”	**:**	〃	Tr OFF
Bit 2=“H”	**:** Half-bridge A1 L- side		Tr ON
=“L”	**:**	〃	Tr OFF

i.e.

SI Bit1=“H”, Bit2=“L” **:** Half-bridge A=“H”
Bit1=“L”, Bit2=“H” **:** Half-bridge A=“L”
Bit1=“L”, Bit2=“L” **:** Half-bridge A= OFF (Hi-Z)
Bit1=“H”, Bit2=“H” **:** Half-bridge A= OFF (Hi-Z)

Bit13 (OCreset):

Result flag of over current detection in SPI Status register is reset by inputting “H” to Bit13 (OCreset). Motor drive output that is forced OFF by the overcurrent detection operates in accordance with the Bit1 to Bit12 which are transmitted simultaneously with the Bit13.

H: The flag of the over current detection in the Status Flag is reset. Motor drive output that is forced OFF by the overcurrent detection is released. After resetting over current detection, the motor driver outputs in accordance with the Bit 1 to Bit12 of SPI signal which are transmitted simultaneously with the Bit13.

L: No operation.

Bit14 (OTreset):

Result flag of thermal shutdown detection in SPI Status register is reset by inputting “H” to Bit14. All motor drive outputs forced OFF by the thermal shutdown detection are returned to normal operation. In this time, the motor drive outputs in accordance with the Bit1 to Bit12 which are transmitted simultaneously by the SPI communication. Motor operation returns to the normal operation automatically when the chip temperature falls to 160 °C or less. At that time, motor operation is based on the data of Bit1 to Bit12 in the SPI Status register

H: The flag of thermal shutdown detection in the Status Flag is reset. Motor drive output that is forced OFF by the thermal shutdown detection is released. Motor drive output that is forced OFF by the thermal shutdown detection operates in accordance with the Bit1 to Bit12 of SPI signal which are transmitted simultaneously with the Bit14.

L: No operation.

Bit15 (OVreset):

Result flag of over voltage detection in SPI Status register is reset by inputting “H” to Bit15. All motor drive outputs forced OFF by the over voltage detection are returned to normal operation. In this time, the motor drive outputs in accordance with the Bit1 to Bit12 which are transmitted simultaneously by the SPI communication. Motor operation returns to the normal operation automatically when the voltage falls to 25.5 V or less. At that time, motor operation is based on the data of Bit1 to Bit12 in the SPI Status register

H: The flag of over voltage detection in the Status Flag is reset. Motor drive output that is forced OFF by the over voltage detection is released. Motor drive output that is forced OFF by the over voltage detection operates in accordance with the Bit1 to Bit12 of SPI signal which are transmitted simultaneously with the Bit15.

L: No operation.

(SPI Output: SO)

Bit1 to Bit12 (A1Hst to C2Lst):

The outputting state of 12 transistors consisting 3ch of H-bridge is outputted.

H: Transistor ON

L: Transistor OFF (Hi-Z)

Bit13 (OCfail):

When over current (1.5A (typ.)) is detected on each H-bridge Driver, “H” level is outputted. Refer to (5)-3 for over current detection. Once the over current is detected, this flag is kept “H” until SPI Status register is reset by setting SI Bit0(STrest1) and Bit15(OVreset) “H” at the same time or OC is reset by setting Bit13(OCreset) “H”.
(The state of “H” of Bit13 is kept though the current of LSI decreases less than the detecting value.)

Bit14 (OTfail):

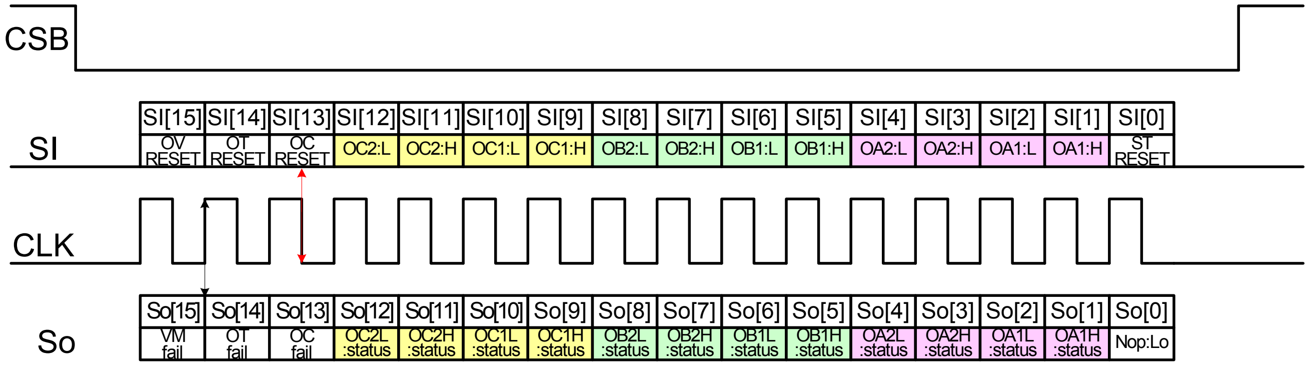
When over temperature (170°C (typ.)) is detected, “H” level is outputted. Refer to (5)-4 for thermal shutdown detection. Once the over temperature is detected, this flag is kept “H” until SPI Status register is reset by setting SI Bit0 (STrest1) and Bit15 (OVreset) “H” at the same time or OC is reset by setting Bit14 (OTreset) “H”.
(The state of “H” of Bit14 is kept though the temperature of LSI decreases less than the detecting value.)

Bit15 (VMfail):

When the over voltage of VMA (26V (typ.)) is detected by monitoring the power supply of H-bridge A (VMA), “H” level is outputted. Refer to (5)-2 for over voltage detection. Once the over voltage is detected, this flag is kept “H” until SPI Status register is reset by setting SI Bit0 (STrest1) and Bit15 (OVreset) “H” at the same time or OC is reset by setting Bit15 (OVreset) “H”.
(The state of “H” of Bit15 is kept though VMA decreases less than the detecting value.)

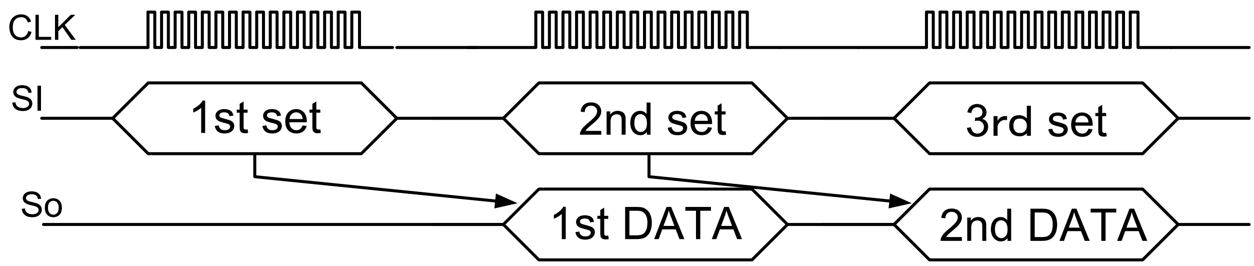
SPI Data

SPI interface is enabled when CSB is set ”H” to L.
The data is outputted from the SO at the rising edge of CLK. Then the SI input data is read to the internal shift register at the falling edge of CLK.



SI Data and SO Data

The status of SO output data is shown in the below figure.



(2) STANDBY MODE / BRAKE MODE (“MODE” terminal / “SEL” terminal)

The STANDBY mode and BRAKE mode can be selected by input terminal of “SEL”, and can move to each mode by setting input terminal of ”MODE” to “L”. Refer to below table for the detail of each mode. “MODE” terminal and “SEL” terminal incorporate pull-down resistance.
(Brake Mode in the table indicates the case the IC is used as a 3ch H-bridge.)

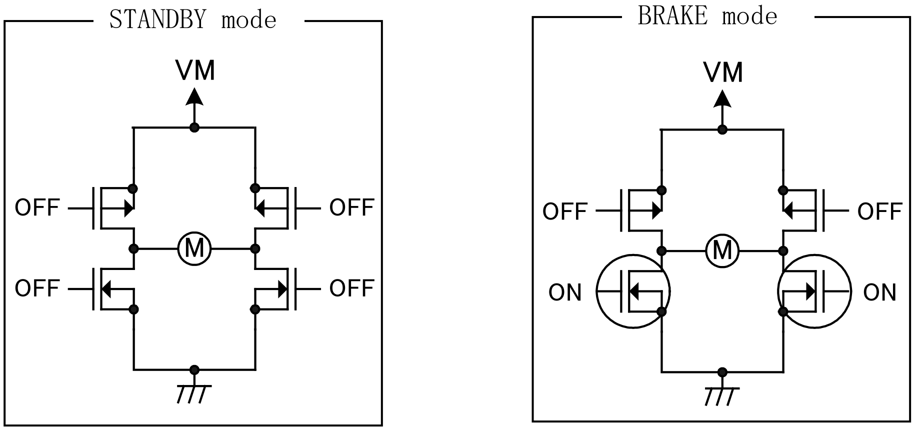
MODE	“MODE” terminal	“SEL” terminal	Operation of motor output circuit	Input data and power supply of each analog circuit
Normal	H	H/L (OPEN)	Normal	Normal
BRAKE	L (OPEN)	H	H-side: OFF(Hi-Z) L-side: ON	Each Input data: KEEP Analog circuit: OPERATE
STANDBY	L (OPEN)	L (OPEN)	H-side: OFF(Hi-Z) L-side: OFF(Hi-Z)	Each input data: Lost (Clear) Analog circuit: STOP

Note1: All of the above operations are under the conditions that the external power supplies of VMA, VMBC, VDD, and VCC are always supplied

Note2: When the input terminal of SEL is configured “L” or open in the BRAKE mode, the operation can move to the standby mode directly. However, when the input terminal of SEL is configured ”H” in the standby mode, the input data is ignored and the operation does not move to the BRAKE mode. In the standby mode, the abnormal detecting functions are turned off. In the standby mode, operations of all circuits including analog circuits are turned off and each input data are cleared (initial). So, as described above, in the standby mode, the input data are ignored though the input terminal of SEL is configured “H” and the operation does not move to the BRAKE mode. When it is necessary to move the operation from the standby mode to the brake mode, please set the operation to the normal mode and then set the brake mode. In this time, the time to start up the analog circuit is needed.

Note3: When use the IC in the standby mode with the MODE terminal by fixing the SEL terminal, please avoid generating the BEF(Back Electromotive Force) by turning on the low side of the H-bridge circuit by SI input signal and braking before moving to the standby mode. Otherwise, there is a possibility to damage the IC by BEF (Back Electromotive Force) if the operation is configured from motor rotating to the standby mode directly. Regardless of the input signal SI, the brake mode stops the motor output (HVMOS) directly.

●**Example: each mode (only 1ch H-bridge)**



Note1: When the mode is changed by the input terminal of “SEL” or “MODE” during SPI transmission, the SPI communication is stopped and all of the input data which are already sent to the TB9102FNG are ignored. Then, the mode is transmitted according to the input data.

Note2: Cautions in using the MODE terminal and the SEL terminal are written below.

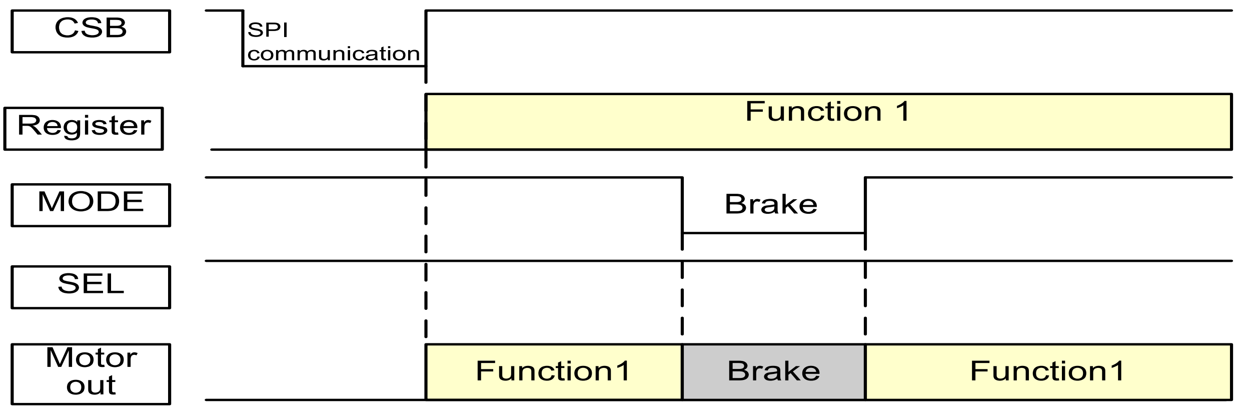
- **Brake mode**

  When the mode moves to the brake mode by using MODE terminal, SPI register data are stored.
  Therefore, the motor operates according to the previous SPI register data until new data is written to the SPI resister after releasing BRAKE mode and finishing 2nd SPI transmission. When the motor need to be operated differently just after releasing BRAKE, release BRAKE (set the MODE terminal “L” to “H”) just before the rising edge of CSB of 1st SPI transmission.

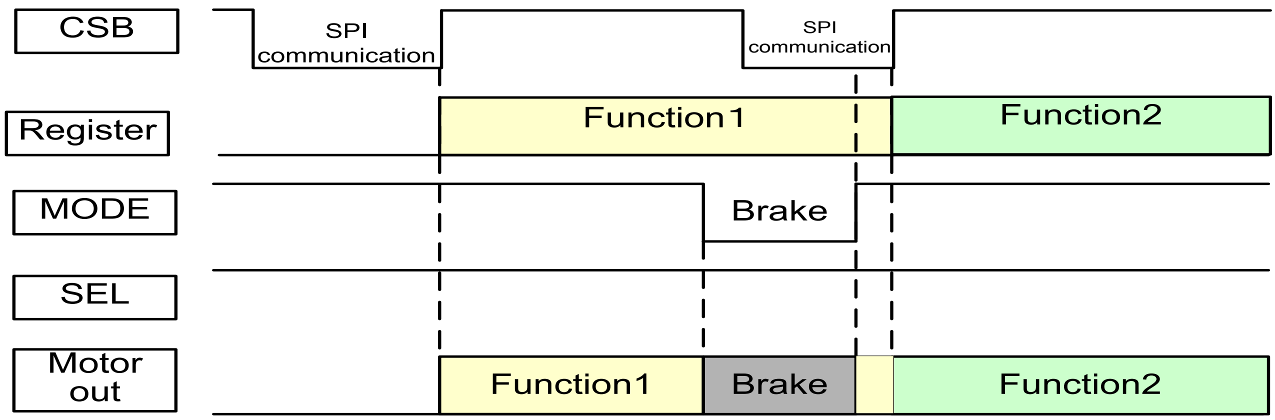
- **Standby mode**

  When the mode is moved to the standby mode by combining the “L” setting of the MODE terminal and “L” setting of the SEL terminal, all of data configured by SPI transmission are reset (cleared).
  Therefore, function should be configured again by SPI transmission after the standby mode is released. Data is not read if SPI is transmitted during the standby mode.

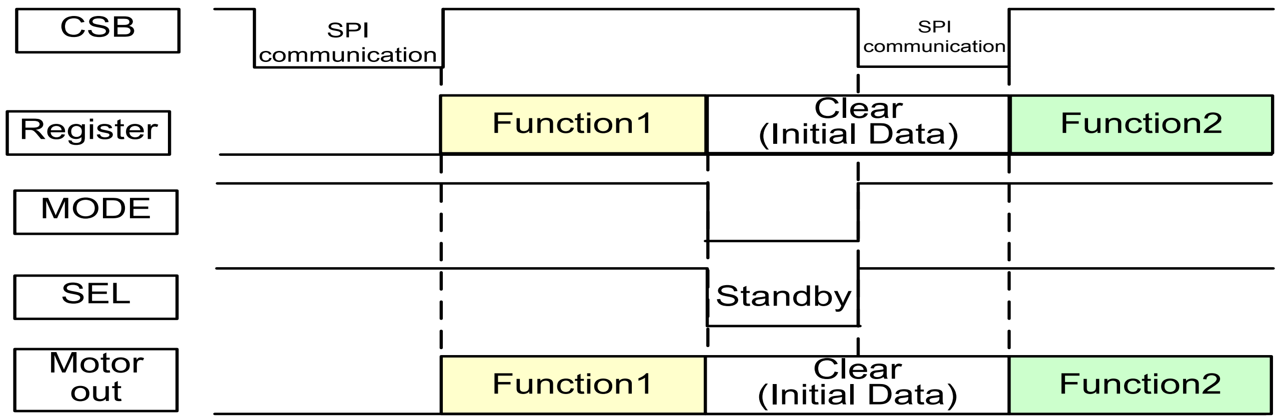
・**Case1: Brake ON/OFF**



・Case 2: New SPI transmission after releasing Brake

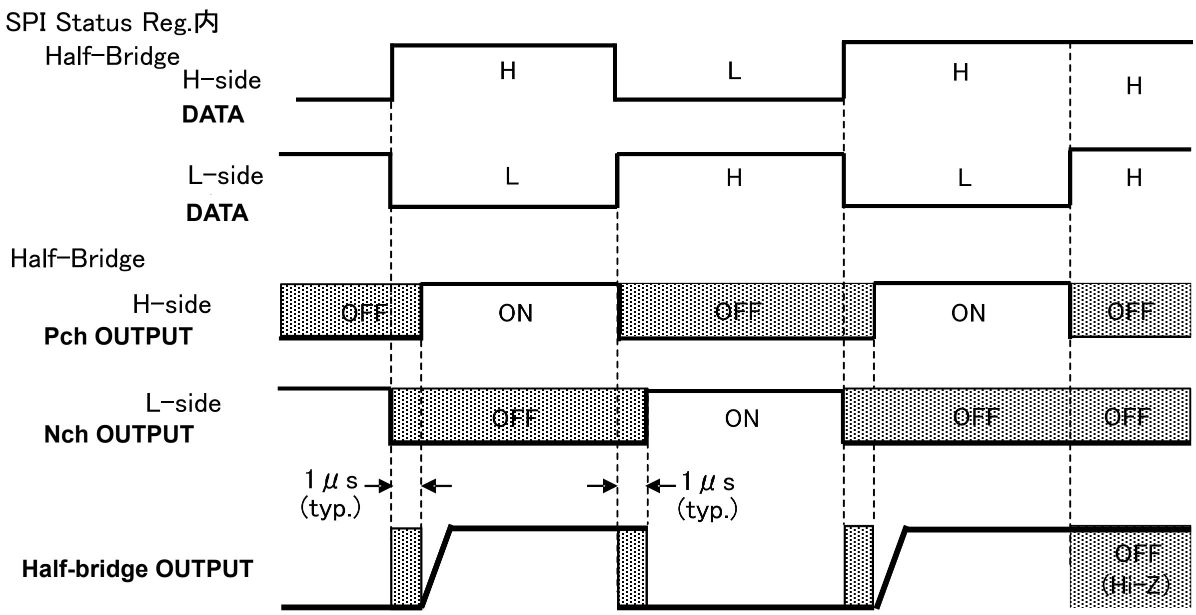


・Case3: Function after releasing the standby



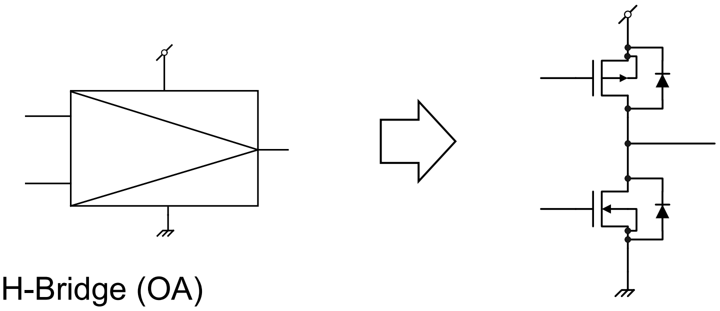
(3) DEAD TIME

The TB9102FNG generates 1μsec (typ.) of Hi-Z state to avoid the short circuit due to "ON" of both High-side and Low-side consisting each Half-bridge in each H-bridge. The state of Hi-Z is generated when HVMOS changes from OFF to ON as shown below. When both High-side and Low-side of the same Half-bridge are turned on by SPI communication, output of the Half-bridge becomes Hi-Z.

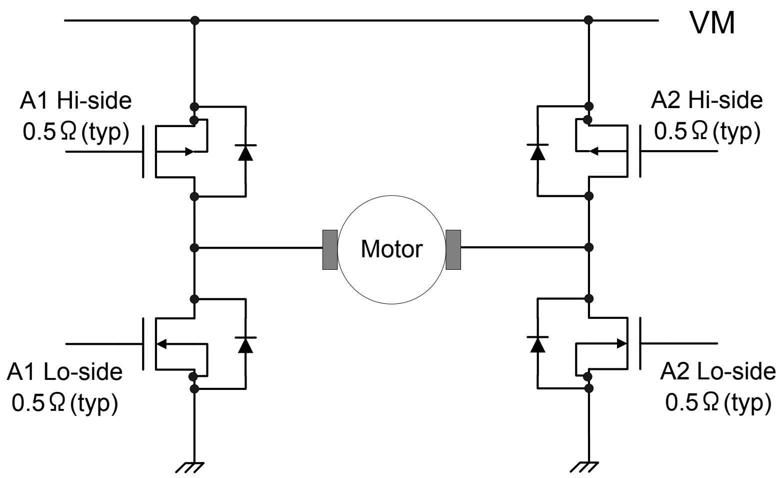


(4) Motor Driver

Each Half-bridge has the following construction.



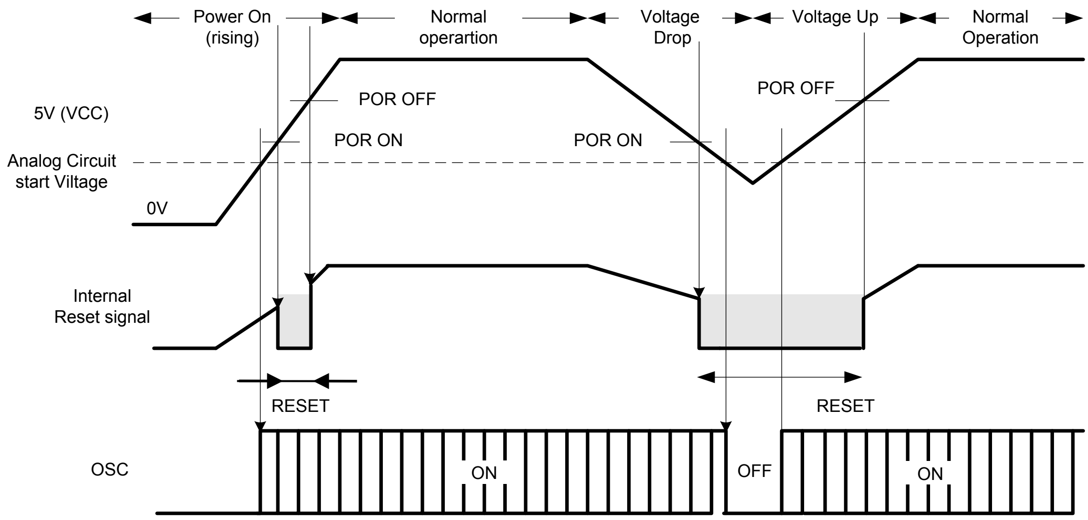
Example: H-Bridge (OA)



(5) Abnormal Detection

(5)-1. Under Voltage Detection circuit for 5V power supply (VCC and VDD supplies) (Internal power on reset)

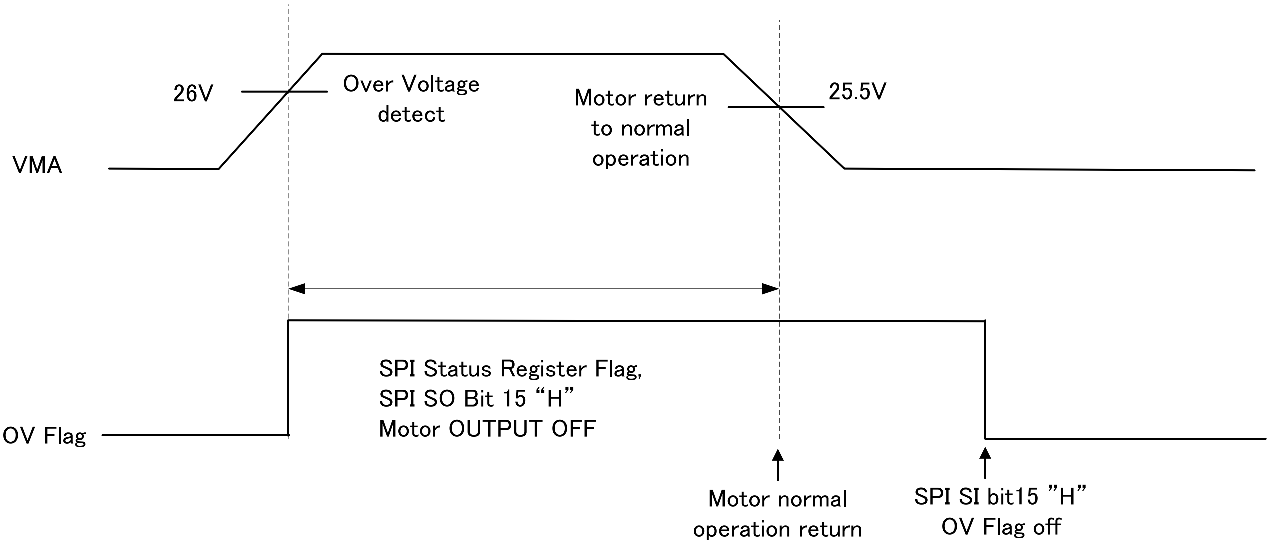
It monitors the externally applied voltage basing on internal band gap voltage and detect the under voltage. When 5V power supply VCC (VDD) falls to the detection voltage (4.0V (typ.)) or less, All circuits of the TB9102FNG are reset internally and driver outputs are turned off (Hi-Z). When VCC rises over returning voltage (4.1V (typ.)), the detection is released and the TB9102FNG returns to the normal operation from the initial state. The detection and return voltages have the hysteresis (Refer to “Electrical Specification).
And the internal detection and return signals incorporate the protection circuit against chattering to avoid malfunction.



(5)-2. Over Voltage Detection for power supply of H-bridge (VMA) driver (26V (typ.))

The TB9102FNG incorporates the over voltage detection circuit for H-bridge A based on the internal band gap voltage. When H-bridge A voltage (VMA) rises over 26V (typ.), all outputs of H-bridge are turned off (Hi-Z) to protect the driver from over voltage. “H” is outputted by Bit15 of SPI Status register output (SO).
When VMA falls to releasing voltage (25.5V (typ.)) or less, outputs of H-bridge, which are turned off forcedly, returns to the normal operation according to the data of SPI Status register. The flag of SPI Status register keeps “H”. This flag can be released by inputting “H” to both Bit0 and Bit15 of SI at the same time (SPI Status register Reset) or inputting “H” to Bit15(OVreset).
In case of SPI Status register Reset, data of Bit1 to Bit12 transmitted at the same time are ignored. So, the motor output should be configured by the following SPI transmission.

Internal detection and release signals of over voltage detection have the protection circuit against chattering to avoid malfunction. So, even if the over voltage detection is released, the over voltage is detected again and all motor outputs are turned off (Hi-Z) when the voltage continues to exceed the over voltage detection value.



【CAUTION】 This over voltage detection does not clamp the power supply voltage of the TB9102FNG.
Therefore, VMA and other power supplies should be protected externally not to exceed the absolute maximum rating. VMA should be connected to VMBC power supply or GND (GNDA, GNB, and GNC) externally, even in case of using 1ch and 2ch of H-bridge only. If VMA is not connected on PCB, over voltage detection does not operate.

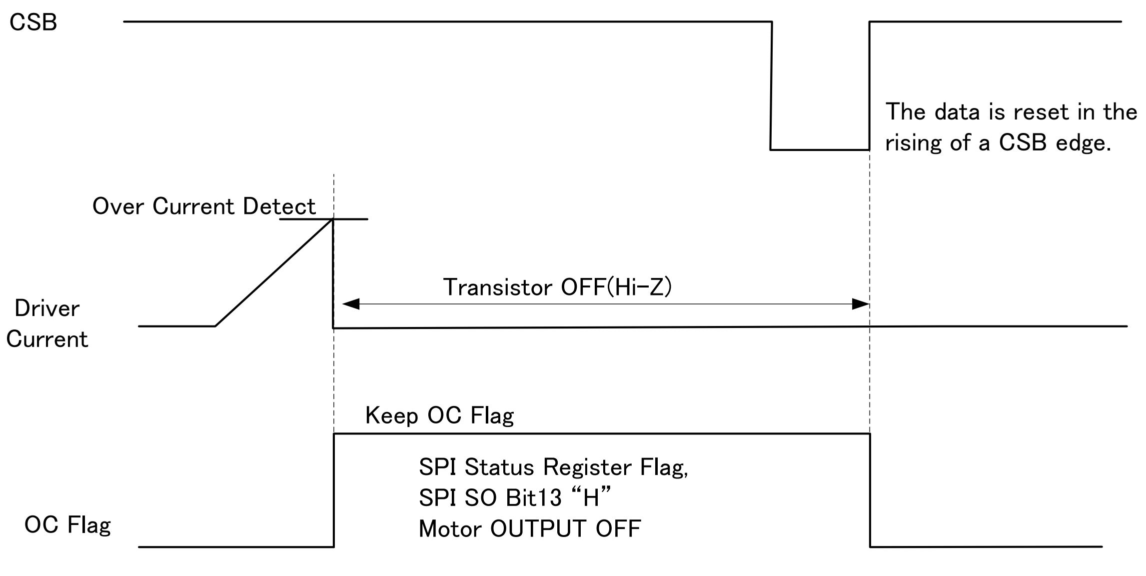
(5)-3. Over Current Detection for Driver (1.5A (typ.))

The TB9102FNG incorporates the over current detection for each High-side and Low-side driver, which consists each Half-bridge of the H-bridge circuit. When output current of ±1.5A (typ.) or more flows in one of the drivers, the driver output detected by the over current detection is turned off. And "H" is outputted by SPI output (SO) Bit13.
Once the over current is detected, the transistor continues to turn OFF (Hi-Z), if the current falls to the normal level. The over current detection is reset by inputting "H" to SPI SI Bit0 and Bit15 at the same time (SPI Status register Reset) or by inputting "H" to Bit13 (Ocreset). The configuration after resetting the over current detection by SI Bit0, Bit15, and Bit13 is described below.

STreset: All SPI Status registers are reset at the rising edge of the clock CSB by inputting "H" to both Bit0 and Bit15. Then, all outputs of each motor driver are turned off (Bit of OFF state keeps OFF). In this time, data of Bit1 to Bit12, which are transmitted at the same timing of Bit0 and Bit15, are ignored. So, configure the motor output by the next SPI transmission after resetting SPI Status register by Streset.

OCreset: Over current detection state is reset by inputting "H". In this time, data of Bit1 to Bit12 transmitted at the same time are valid and the motor output is configured by these Bit data.

Internal detection and release signals of the over current detection have protection circuit against chattering to avoid malfunction. Even after the above reset for over current detection, if the over current state continues, the over current detection operates again and the output of motor driver is turned off again.

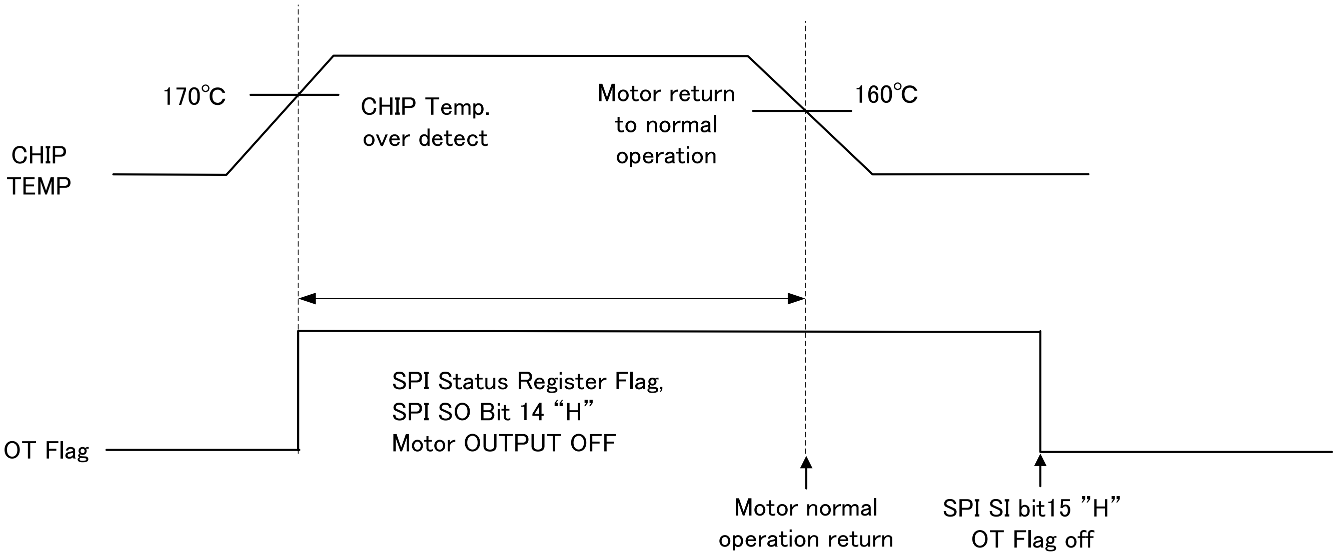


Note: The over current detection circuit is only intended to provide temporary protection against irregular conditions such as an output short-circuit. It does not necessarily guarantee the complete IC safety. Therefore, utmost care is necessary in the design of the output lines, VCC, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous terminals.

(5)-4. Thermal shutdown detection (170°C (typ.))

The TB9102FNG incorporates the thermal shutdown detection which monitors the temperature of the internal IC chip near the driver output circuit for the motor. When the chip temperature rises 170°C (typ.) or more, all driver outputs are turned off (Hi-Z) and Bit14 of SPI Status register Output (SO) is set to “H”. When the temperature falls to 160°C (typ.) or less after thermal shutdown circuit operates, H-bridge driver outputs, which were turned off forcedly, return to the normal operation according to the data of SPI Status register. The flag of Bit14 of SPI Status register is kept “H”. The flag is released when “H” is inputted to SPI SI Bit14 (OTreset) or to both Bit 0 and Bit15 (Streset). In case of SPI Status register reset, data of Bit1 to Bit12, which were transmitted at the same timing of Bit0 and Bit15, are ignored. So, configure the motor output by the next SPI transmission after resetting the thermal shutdown detection.

Internal detection and release signals of the thermal shutdown detection have protection circuit against chattering to avoid malfunction. Even after the above reset for thermal shutdown detection, if the over temperature state continues, the thermal shutdown detection operates again and the output of motor driver is turned off (Hi-Z) again.



Note: The Absolute maximum temperature of the TB9102FNG is 150°C. The absolute maximum temperature is never exceeded in using and storing the TB9102FNG. If any of the rating would be exceeded, the normal operation of the IC can no longer be guaranteed. Moreover, exceeding the absolute maximum rating may cause smoke or ignition of the device. Do not exceed any of the absolute maximum rating.

Though this IC incorporates thermal shutdown detection, this function does not reduce the over temperature of the IC (below 170 °C). It is a subservient function for the out of the range of the operating guarantee.

(As for this function, shipping test is not performed at the actual temperature individually. Operation of the thermal shutdown detection is pseudo-confirmed by the TEST function.)

(6) Internal Oscillator (4MHz (typ.))

The TB9102FNG incorporates the oscillation circuit of 4MHz (typ.) for operation of the internal circuit. It is used for generation of basic clock of the internal logic circuit and DEAD TIME, and for each abnormal detection circuit.
Pay attention that in STANDBY mode, this oscillation circuit is turned off and each abnormal detection circuit does not work.

(7) Electrical Characteristics

MAXIMUM ABSOLUTE RATINGS (Ta=25°C)

ITEM	SYMBOL	PIN	CONDITION	RATING	UNIT
Supply Voltage	VM	VMA, VMBC	DC Voltage	-0.3 to +40	V
	VDD, VCC	VDD ,VCC	DC Voltage	-0.3 to +6.0	
Output Current	IOUT	OA1, OA2, OB1, OB2, OC1, OC2	at Over Current Detection	±1.5	A
		OA1, OA2, OB1, OB2, OC1, OC2	-	±1.0	
		SO	-	±10	mA
Input/Output Voltage	VIN, VOUT	TEST1, TEST3 SEL, CSB, CLK, SI, MODE	-	-0.3 to VDD+0.3 (max: 6V)	V
		OA1, OA2, OB1, OB2, OC1, OC2	Note2	-0.3 to VM (max: 40V)	
		SO, TEST2	-	-0.3 to VDD+0.3 (max: 6V)	V
Storage Temperature	Tstg	-	-	-55 to +150	°C
Soldering Temperature	Tsol	-	Manual Soldering	260(10s)	
Max Power Dissipation	PD	-	PCB 76.2×114.3×t1.6 Mono Layer, Cu: 30%	1.32	W

CAUTION 1: The above current spec. value of "+" is Input from outside,"-" is Output from TB9102FNG.

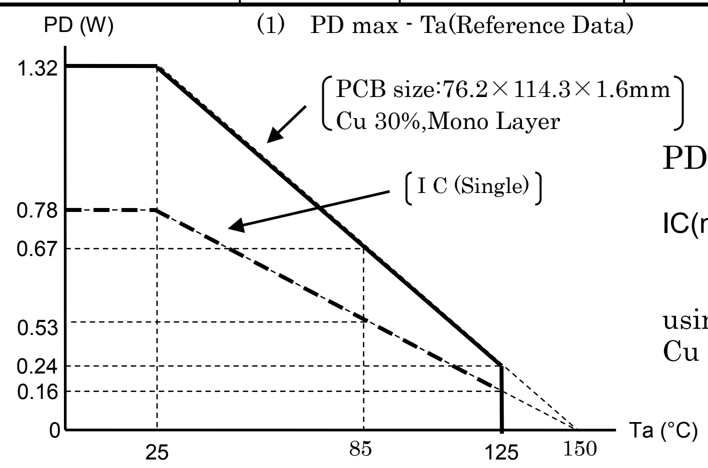
CAUTION 2: Please do not exceed the absolute maximum rating, including the reverse voltage.

CAUTION 3: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in these documents.

Package (SSOP24-P-300-0.65A) Thermal Resistance

ITEM	SYMBOL	RATING	CONDITION	UNIT
Thermal Resistance	Rθj-a	160	IC	°C/W
		95	PCB 1Layer, size:76.2×114.3×t1.6mm, Cu:30%, Cu thickness:35μm	°C/W
		60	PCB 4Layer, size:76.2×114.3×t1.6mm Cu:30%, Cu thickness:35μm	°C/W

(1) PD max - Ta(Reference Data)



$$PD = (150 - Ta)/R_{\theta j\text{-}a}$$

IC(no PCB) at 25°C.
(150-25)/160 = 0.781 (W)

using PCB(Mono Layer) size: 76.2×114.3×1.6mm
Cu 30% at 25°C.
(150-25)/95 = 1.32(W)

(7) Electrical Characteristics (cont.)

Operating Range

ITEM	SYMBOL	RATING	UNIT	NOTES
Supply Voltage	VM	7 to 18	V	-
	VDD,VCC	4.5 to 5.5		Operating range of 5V circuit (Logic circuit, Bipolar)
Operating Temperature	Topr	-40 to 125	°C	-

IC Characteristics

The following are under condition VMA=VMBC=7 to 18V, VDD=VCC=4.5 to 5.5V, Ta=-40 to 125°C. unless otherwise specified

ITEM	Symbol	PIN	CONDITION	MIN	TYP	MAX	UNIT
Current Consumption (operation)	I(VM)	VMA, VMBC	OA1/2,OB1/2,OC1/2 : OPEN(no load)	-	1.0	6.0	mA
	I(VDD+VCC)	VDD, VCC	(Logic circuit only)	-	1.4	2.0	mA
Standby Current	Istby(VM)	VMA, VMBC	at Standby mode(CSB=H, CLK=SI=SEL=MODE=L) each Motor off	-	1.0	30	μA
	Istby(VDD +VCC)	VDD,VCC	-	-	3.0	10	μA
Output Voltage Level “L”	VOL(SO)	SO	IOL=2.5mA	-	0.05	0.4	V
Output Voltage Level “H”	VOH(SO)	SO	IOH= -2.5mA	VDD-0.6	VDD-0.05	-	V
Output OFF Leak Current	IO(OFF)	SO	CSB=H	-3	-	3	μA
Input Current Level “L”	IIL1	CSB	VIN=0V	-100	-50	-10	μA
	IIL2	SI,CLK, MODE, SEL		-10	-	10	
Input Current Level ”H”	IIH1	CSB	VIN=VDD	-10	-	10	μA
	IIH2	SI,CLK, MODE,SEL		10	50	100	
Input Voltage Level ”L”	VIL1	MODE,SI,CLK, CSB,SEL	-	-	-	0.3*VDD	V
Input Voltage Level ”H”	VIH1		-	0.75*VDD	-	-	
Hysteresis of Input Voltage	VHYS1		-	-	0.5	-	

(7) Electrical Characteristics (cont.)

Motor Driver

The following are under condition VMA=VMBC=7 to 18V, VDD=VCC=4.5 to 5.5V, Ta=-40 to 125°C. unless otherwise specified

ITEM	Symbol	PIN	CONDITION	MIN	TYP	MAX	UNIT
High-side Output ON Resistance	RHON	OA1,OA2 OB1,OB2 OC1,OC2	IOUT=-0.5A,Ta=+25°C	-	0.5	0.8	Ω
			IOUT=-0.5A,Ta=125°C	-	0.7	1.2	
			IOUT=-0.5A,Ta=-40°C	-	0.4	0.6	
Low-side Output ON Resistance	RLON		IOUT=+0.5A,Ta=+25°C	-	0.5	0.8	
			IOUT=+0.5A,Ta=125°C	-	0.6	1.2	
			IOUT=+0.5A,Ta=-40°C	-	0.3	0.6	
Output OFF Leak Current	ILO		Output OFF,VOUT=0V Ta=25°C	-1	-	-	μA
			Ta=-40 to 125°C	-5	-	-	
			Output OFF,VOUT=VM Ta=25°C	-	-	1	
			Ta=-40 to 125°C	-	-	5	

Note1: When Motor is rotated, it makes Electromotive Force. The Electrical Specification must be kept, even with this Electromotive Force.

Abnormal Detection

The following are under condition VMA=VMBC=7 to 18V, VDD=VCC=4.5 to 5.5V, Ta=-40 to 125°C. unless otherwise specified

ITEM	Symbol	PIN	CONDITION	MIN	TYP	MAX	UNIT
Under Voltage Detection circuit RESET OFF Voltage of VCC	VRSTH	VCC	-	3.9	4.1	4.3	V
Under Voltage Detection circuit RESET ON Voltage of VCC	VRSTL		-	3.8	4.0	4.2	V
RESET Hysteresis Voltage	VRSTHYS		VRSTHYS=VRSTH-VRSTL	-	0.1	-	V
Over current detection Current ("-" short)	ISLMAX	OA1,OA2 OB1,OB2 OC1,OC2	-	-2.5	-1.6	-1.0	A
Over Current Detection Current ("+" short)	ISHMAX		-	1.0	1.5	2.5	
Over Voltage Detection ON	VSDH	VMA,VMBC	Motor no load	24.5	26.0	27.5	V
Over Voltage Detection OFF	VSDL			24.0	25.5	27.0	
Over Temp. Detection ON	TSDH	OA1,OA2 OB1,OB2 OC1,OC2	Note2: Design value	155	170	-	°C
Over Temp. Hysteresis	TSDHYS			-	10	-	

Note2: This Temperature detection function is only checked by circuit simulation, it is not tested on production.

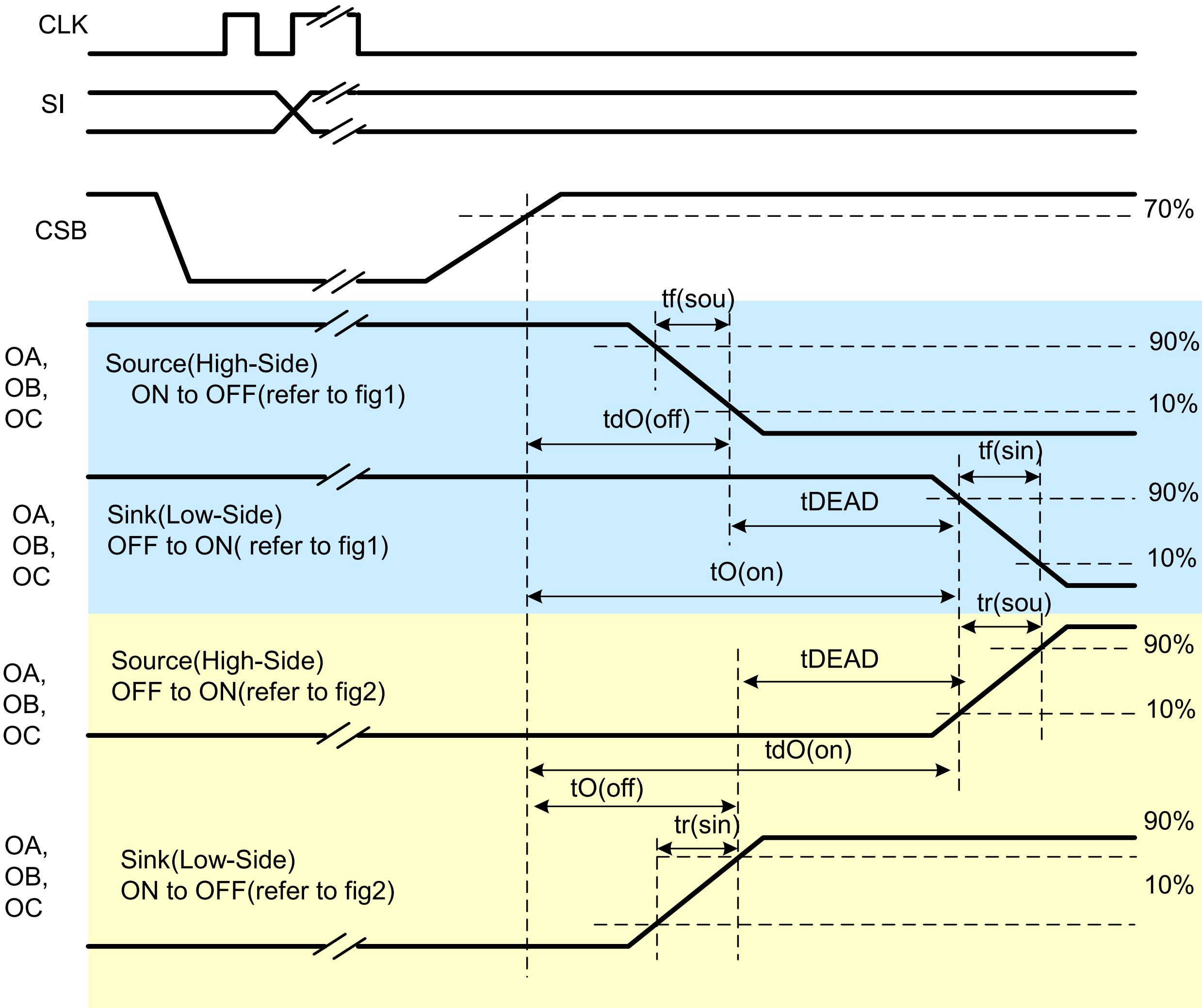
(7) Electrical Characteristics (cont.)

AC Characteristics: Motor Output Delay time

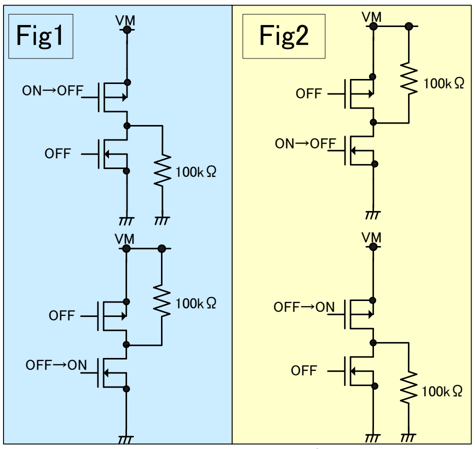
The following are under condition VMA=VMBC=7 to 18V, VDD=VCC=4.5 to 5.5V, Ta=-40 to 125°C. unless otherwise specified

ITEM	Symbol	PIN	CONDITION	MIN	TYP	MAX	UNIT
Source(High-side) ON time	tdO(on)	CSB OA1,OA2 OB1,OB2 OC1,OC2	Rload=100Ω	-	4.5	7.0	μs
Source(High-side) OFF time	tdO(off)		Rload=100Ω	-	2.5	4.0	
Sink(Low-side) ON time	tO(on)		Rload=100Ω	-	4.5	7.0	
Sink(Low-side) OFF time	tO(off)		Rload=100Ω	-	2.5	4.0	
DEAD TIME	tDEAD		-	-	2.0	-	μs
Source(High-side) Rising time	tr(sou)	OA1,OA2 OB1,OB2 OC1,OC2	Rload=100Ω	-	5.0	9.0	μs
Source(High-side) Falling time	tf(sou)		Rload=100Ω	-	0.2	0.5	
Sink(Low-side) Rising time	tr(sin)		Rload=100Ω	-	0.2	0.5	
Sink(Low-side) Falling time	tf(sin)		Rload=100Ω	-	4.0	8.0	

AC Time chart of Motor output delay time



AC timing measurement circuit



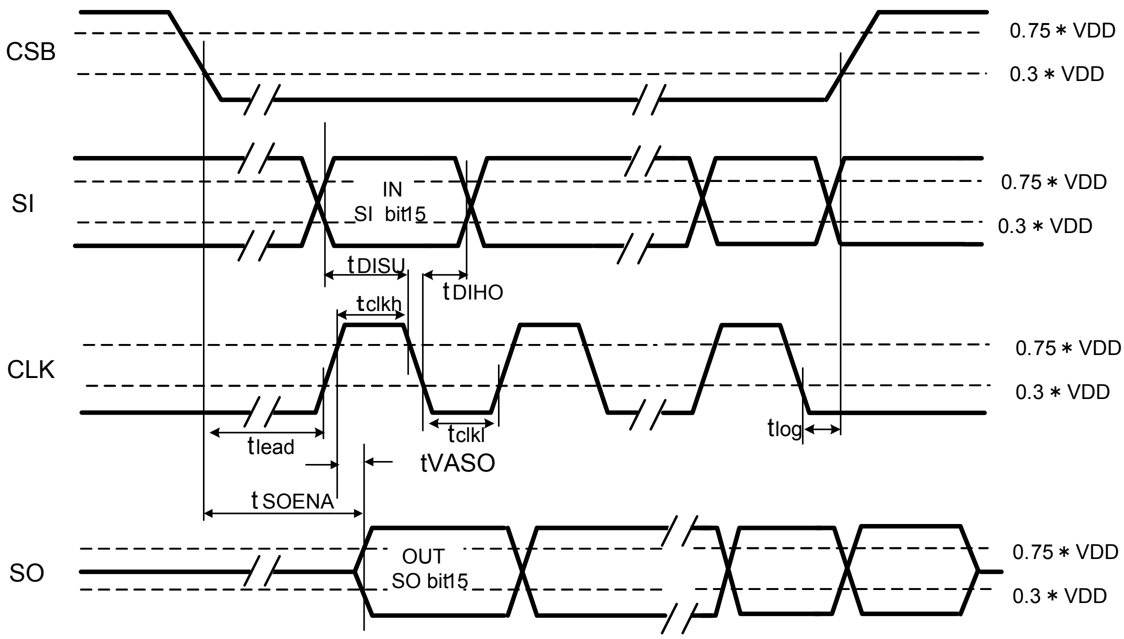
Note1: Components in the test circuits are only used to obtain and confirm the device characteristics.
These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

Note2: Timing charts may be simplified for explanatory purpose.

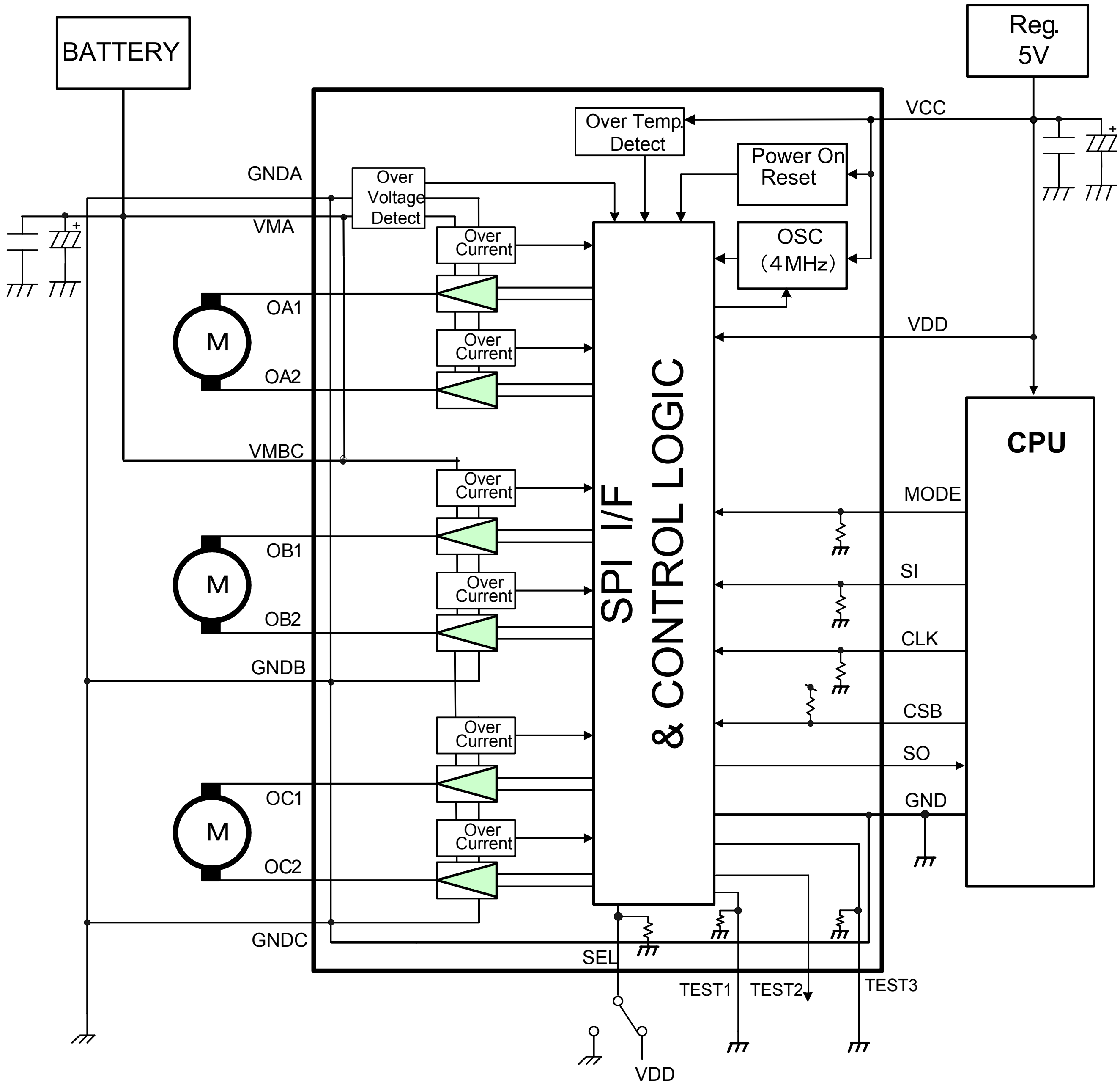
SPI Delay Time

The following are under condition VMA=VMBC=7 to 18V, VDD=VCC=4.5 to 5.5V, Ta=-40 to 125°C unless otherwise f specified

ITEM	Symbol	PIN	CONDITION	MIN	TYP	MAX	UNIT
CLK Frequency	tpclk	CLK	-	-	-	1.0	MHz
CLK High Time	tclkh		-	250	-	-	ns
CLK LOW Time	tclkl		-	250	-	-	
CSB↓-CLK↑Set Up Time	tlead	CSB,CLK	-	10	-	-	μs
CLK↓-CSB↑Set Up Time	tlag		-	100	-	-	ns
SISet Up Time	tDISU	CLK,SI	-	125	-	-	ns
SI Hold Time	tDIHO		-	125	-	-	
SO EnableTime	tSOENA	SO,CSB	CL=100pF	-	-	10	ns
SO Valid Time	tVASO	SI, SO	CL=100pF	-	-	125	ns



Application circuit diagram (1) 3ch H-bridge use



＊1: Some of the functional blocks,circuit,or constants in the block diagram may be omitted or simplified for explanatory purpose.

＊2: Install the product correctly. Otherwise, it may result in break down, damage and/or deterioration to the product or equipment.

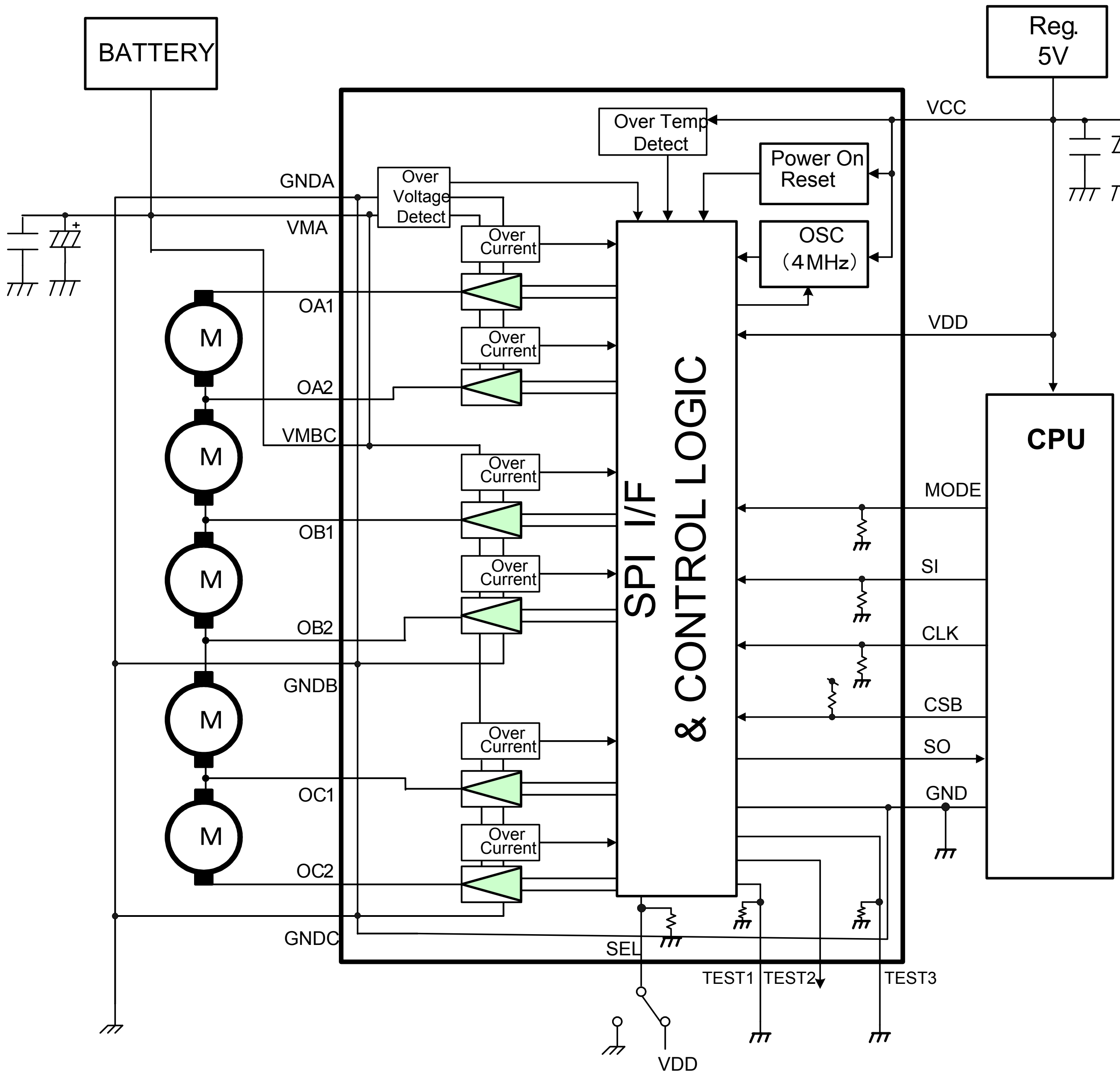
＊3: The application circuits shown in this document are provided for reference purposes only.
Especially, a thorough evaluation is required on the phase of mass production design.
Toshiba dose not grant the use of any industrial property rights with these examples of application circuits.

＊4: Short Circuit between each Output signal, Output Signal and Power line (Battery, Regulator Output, GND) may make the cause of IC destruction or Damage.

＊5: VCC and VDD should be connected externally on board to avoid voltage gap between VCC and VDD for proper operation.

＊6: Even only using 1ch/2ch H-Bride, VMA and VMBC should be connected to power supply on the board. Over Voltage is detected at VMA. Only VMBC connection cannot detect.

Application circuit diagram (2) 6ch Half-bridge use



∗1: Some of the functional blocks,circuit,or constants in the block diagram may be omitted or simplified for explanatory purpose.

∗2: Install the product correctly. Otherwise, it may result in break down, damage and/or deterioration to the product or equipment.

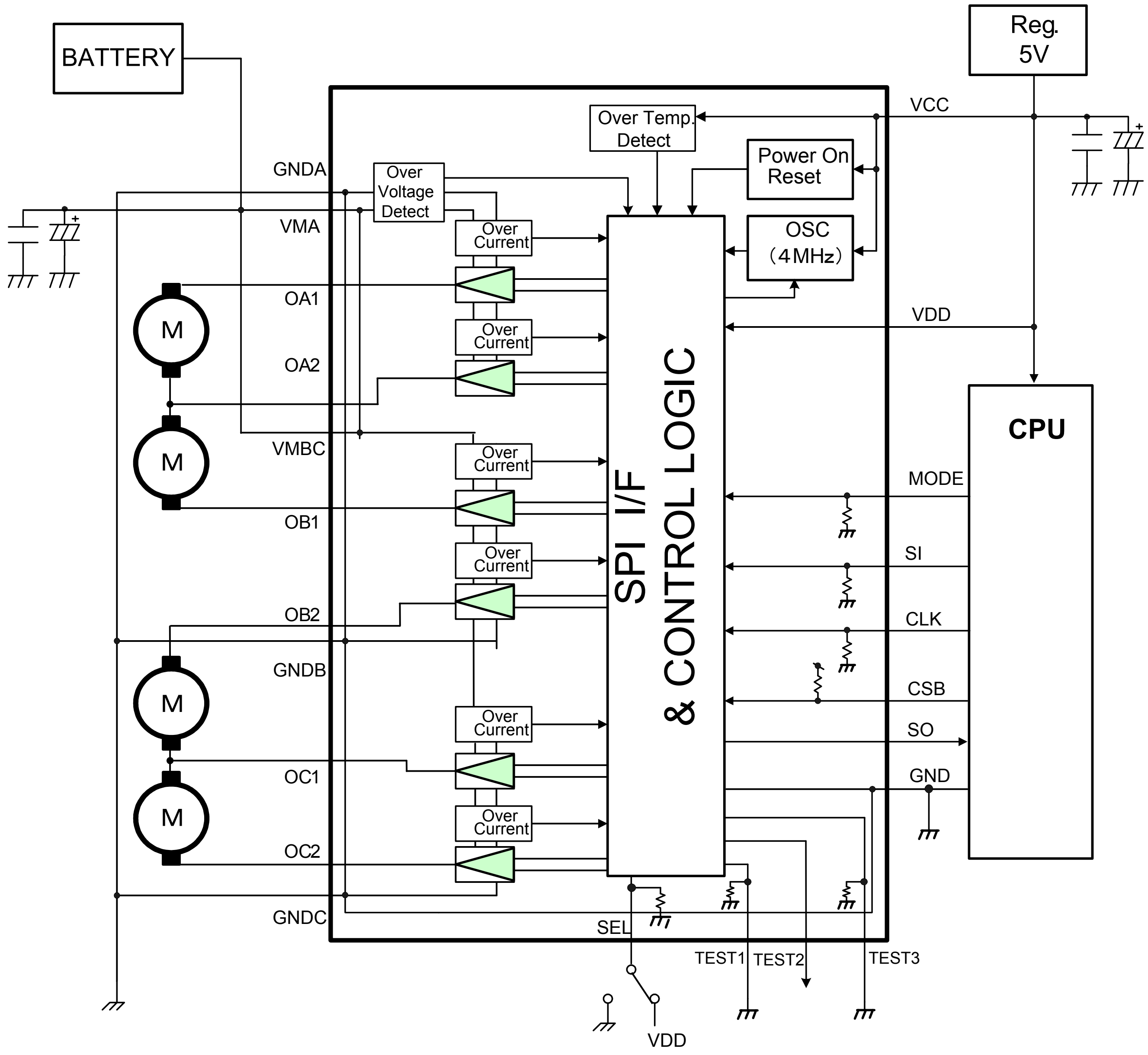
∗3: The application circuits shown in this document are provided for reference purposes only.
Especially, a thorough evaluation is required on the phase of mass production design.
Toshiba dose not grant the use of any industrial property rights with these examples of application circuits.

∗4: Short Circuit between each Output signal, Output Signal and Power line (Battery, Regulator Output, GND) may make the cause of IC destruction or Damage.

∗5: VCC and VDD should be connected each other on the board to do not make voltage gap between VCC and VDD. Otherwise, it may be cause of improper the TB9102FNG operation.

∗6: Even only using 1ch/2ch H-Bride, VMA and VMBC should be connected to power supply on the board. Over Voltage is detected at VMA. Only VMBC connection cannot detect.

Application circuit diagram (3) 6ch Half-bridge use



∗1: Some of the functional blocks, circuit, or constants in the block diagram may be omitted or simplified for explanatory purpose.

∗2: Install the product correctly. Otherwise, it may result in break down, damage and/or deterioration to the product or equipment.

∗3: The application circuits shown in this document are provided for reference purposes only.
Especially, a thorough evaluation is required on the phase of mass production design.
Toshiba dose not grant the use of any industrial property rights with these examples of application circuits.

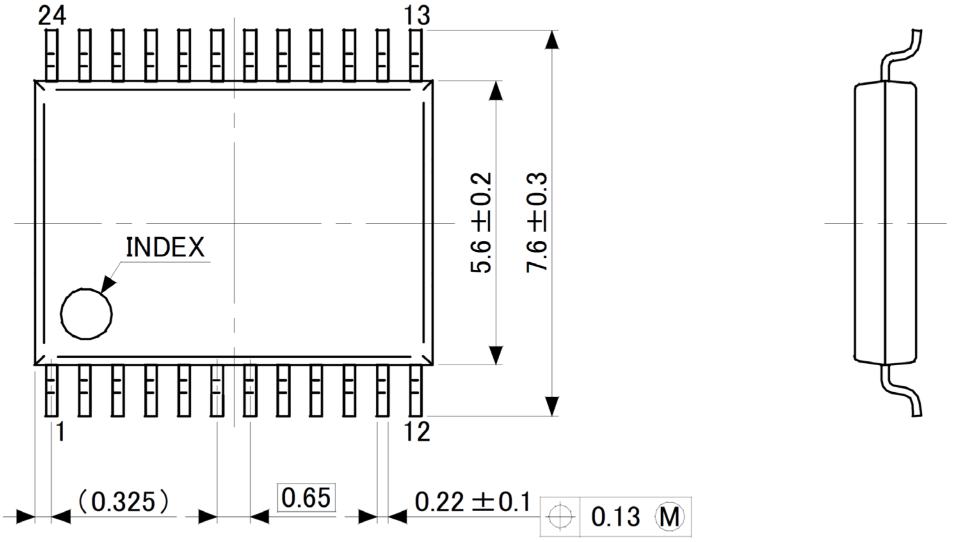
∗4: Short Circuit between each Output signal, Output Signal and Power line (Battery, Regulator Output, GND) may make the cause of IC destruction or Damage.

∗5: VCC and VDD should be connected each other on the board to do not make voltage gap between VCC and VDD. Otherwise, it may be cause of improper the TB9102FNG operation.

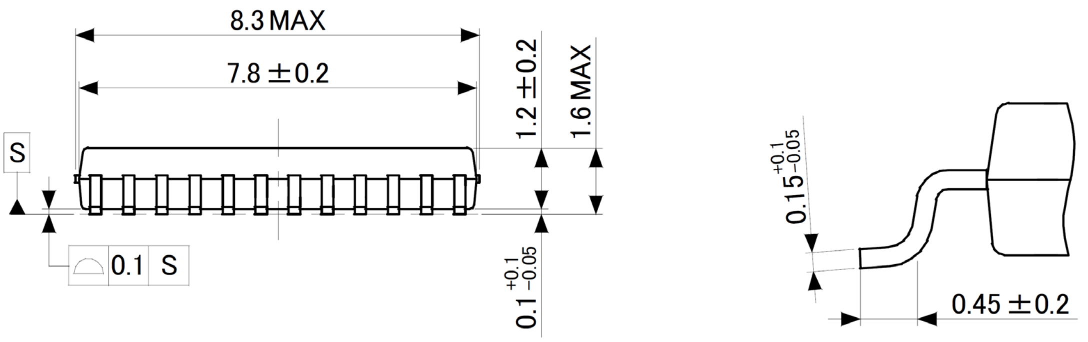
∗6: Even only using 1ch/2ch H-Bride, VMA and VMBC should be connected to power supply on the board. Over Voltage is detected at VMA. Only VMBC connection cannot detect.

Package
SSOP24-P-300-0.65A

Unit: mm



Detailed dimension of lead edge



Weight: 0.14g (typ.)

【CAUTION 】

- Some of the functional blocks, circuits, or constants in the block diagram may be omitted or Simplified for explanatory purpose.
- The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.
- Timing charts may be simplified for explanatory purpose.
- The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.
- Ensure that the IC is mounted correctly. Failing to do so may result in the IC or target equipment being damage

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