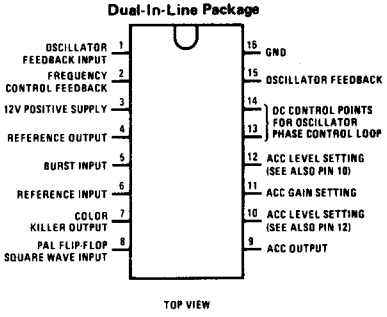
National Semiconductor

TBA540 Reference Combination

General Description

The TBA540 is an integrated 'color reference' oscillator circuit for PAL TV receivers. The oscillator employs a quartz crystal and incorporates automatic phase and amplitude control. A synchronous demodulator is used to compare the phase and amplitude of the swinging burst ripple with the PAL flip-flop waveform and generates appropriate ACC color killer and identification signals. A high standard of noise immunity has been obtained by using synchronous demodulation.

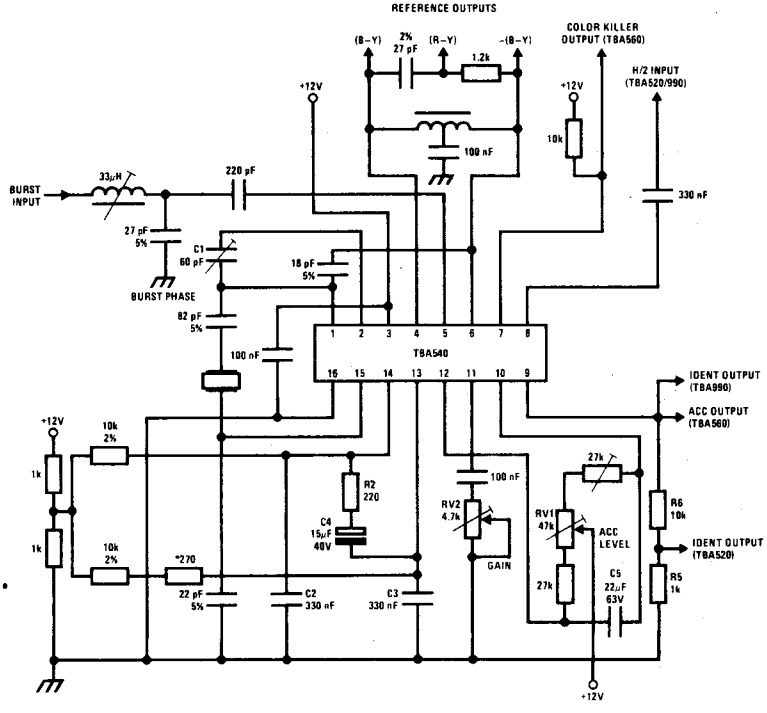
Connection Diagram



Dual-In-Line Package, Order Number TBA540
See NS Package N16A

Quad-In-Line Package, Order Number TBA540Q
See NS Package N16C

Typical Application



Absolute Maximum Ratings

V3-16	13.2V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (T_A = 60°C)	780 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	−20°C to +60°C		

Electrical Characteristics (V3-16 = 12V, T_A = 25°C as measured in typical application circuit)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Output Signals					
V4-16	B-Y Reference Signal Output		1	1.4	2	Vp-p
V7-16	Color Killer Output					
	Color "ON"			12		V
	Color "OFF"			100	250	mV
V9-16	ACC Output Signal Range					
	At Correct Phase of PAL Switch			4 to 0.2		V
	At Incorrect Phase of PAL Switch			4 to 11		V
	Oscillator Section (Amplifier)					
R15-16	Input Resistance			3.5		kΩ
C15-16	Input Capacitance			5		pF
G15-1	Voltage Gain			4.7		
	Reactance Control Section					
G15-2	Voltage Gain With Pins 13 and 14 Shorted			1.3		
$\frac{\Delta G15\text{-}2}{\Delta\phi 5\text{-}4}$	Rate of Change of Gain G15-2 With Phase Difference Between Burst and Reference Signal			5		rad^{-1}
	Burst Input					
R5-16	Input Resistance			1		kΩ
	Burst Input Level		0.7	1.5		Vp-p
	Flip-Flop Input					
V8-16	Voltage			2.5		Vp-p
R8-16	Resistance			3.3		kΩ
	Phase Lock Loop					
	Oscillator Phase Error for a Burst Signal	Crystal Frequency $f_{400\ Hz}$			±10	DEG
	Holding Range			±600		Hz
	Pull-in Range			±300		Hz
	Temperature Coefficient of Oscillator				2	Hz/°C

Application Notes

A dc connection between pins 4 and 6 is necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (B-Y) to that on pin 4. A center tap on the inductor, connected to earth via a dc blocking capacitor, is therefore necessary.

DC Control Points in Reference Control Loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of dc balancing of the reactance stage and the connection of the bandwidth–determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

Initial Adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1.

(c) Set the ACC level adjustment RV1, to give +4V on pin 9. Remove short circuit.

(d) Apply burst signal.

(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5Vp-p on pin 5.

Pin Function Description

1. Oscillator feedback output. The crystal receives its energy from this pin. The output impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback. This pin is fed internally with a sinewave derived from the reference output (pin 4) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance, therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12V supply. The maximum voltage must not exceed 13.2V.

4. Reference waveform output. This pin is driven internally by the regenerated subcarrier waveform in B-Y phase. (The output is in B-Y rather than R-Y phase as the burst phase network produces a lag of 90° of the burst applied to pin 5). An output amplitude of nominally 1.4Vp-p is produced at low impedance. No dc load to earth is required. A dc connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (−(B-Y)) to that on pin 4. A center tap on the inductor, connected to earth via a dc blocking capacitor, is therefore necessary.

5. Burst waveform input. A burst waveform amplitude of 1.5Vp-p is required to be ac-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7V must be exceeded before the burst signal becomes effective. A dc bias of 400 mV is internally derived for pin 5.

The absolute level of the tip of the burst at pin 5 will normally reach 1.5V (1.5Vp-p burst amplitude).

6. Reference waveform input. This pin requires a reference waveform in the −(B-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A dc connection between pins 4 and 6 must be made via the transformer.

7. Color killer output. This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typically 10 kΩ) connected to +12V. The unkilled and killed voltages on this pin are then +12V and < 250 mV respectively. (The voltage range on pin 9 over which switching of the color killed output on pin 7 occurs is nominally +2.5V.)

8. PAL flip-flop square wave input. A 2.5Vp-p square wave derived from the PAL flip-flop (in the TBA520 or TBA990 demodulator IC) is required at this pin, ac-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. ACC output. An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero burst input signal the dc potential produced at pin 9 is set to be +4V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at pin 9 is determined by the control characteristic of the ACC amplifier, i.e., for the TBA560 from 0.8 to 1V. The potential on pin 9 will fall to a value within this range as the burst input signal is stabilized to an amplitude of 1.5Vp-p. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cut-off function in the TBA520 demodulator IC.

10. ACC level setting. The network connected between pins 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. ACC gain control. RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 Vp-p) under ACC control.

12. See pin 10.

13. See pin 14.

14. DC control points in reference control loop. Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of dc balancing of the reactance stage and the connection of the bandwidth-determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

The filter network consists of R2, C2, C3 and C4. The dc potentials on these pins are nominally +6V.

Schematic Diagram