Complementary Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS\ (ON)}$ Max $Q_1 + Q_2$ or $Q_3 + Q_4$	Order Number / Package SOW-20*
40V	3.0Ω	TC0604WG

* Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Telecom switches
- ☐ Logic level interfaces
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Solid state relays
- ☐ Motor controls

Electrical Characteristics

Refer to TN0604WG and TP0604WG data sheet for detailed characteristics of N- and P-channel devices.

Thermal Characteristics

Package	Plastic SOW-20	
I_D continuous & I_{DR} (single die)	N-Channel	1.0A
	P-Channel	-0.6A
I_D pulsed⁺ & I_{DRM}⁺	N-Channel	4.0A
	P-Channel	-2.0A
Power Dissipation @ T_C = 25°C‡		1.5W
θ_{ja} (°C/W)‡		85
θ_{jc} (°C/W)		—

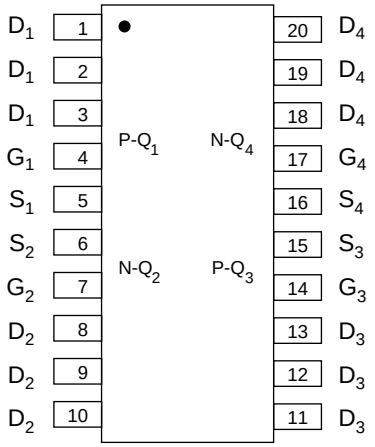
⁺ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view
SOW - 20

Note: See Package Outline section for dimensions.