TC1321

10-Bit Digital-to-Analog Converter with Two-Wire Interface

Features

- 10-Bit Digital-to-Analog Converter
- 2.7-5.5V Single Supply Operation
- Simple SMBus/I^{2}C™ Serial Interface
- Low Power: 350µA Operation, 0.5µA Shutdown
- 8-Pin SOIC and 8-Pin MSOP Packages

Applications

- Programmable Voltage Sources
- Digital Controlled Amplifiers/Attenuators
- Process Monitoring and Control

Device Selection Table

Part Number	Package	Temperature Range
TC1321EOA	8-Pin SOIC (Narrow)	-40°C to +85°C
TC1321EUA	8-Pin MSOP	-40°C to +85°C

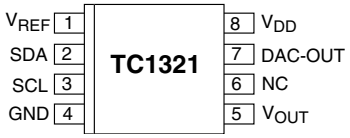
General Description

The TC1321 is a serially accessible 10-bit voltage output digital-to-analog converter (DAC). The DAC produces an output voltage that ranges from ground to an externally supplied reference voltage. It operates from a single power supply that can range from 2.7V to 5.5V, making it ideal for a wide range of applications. Built into the part is a Power-on Reset function that ensures that the device starts at a known condition.

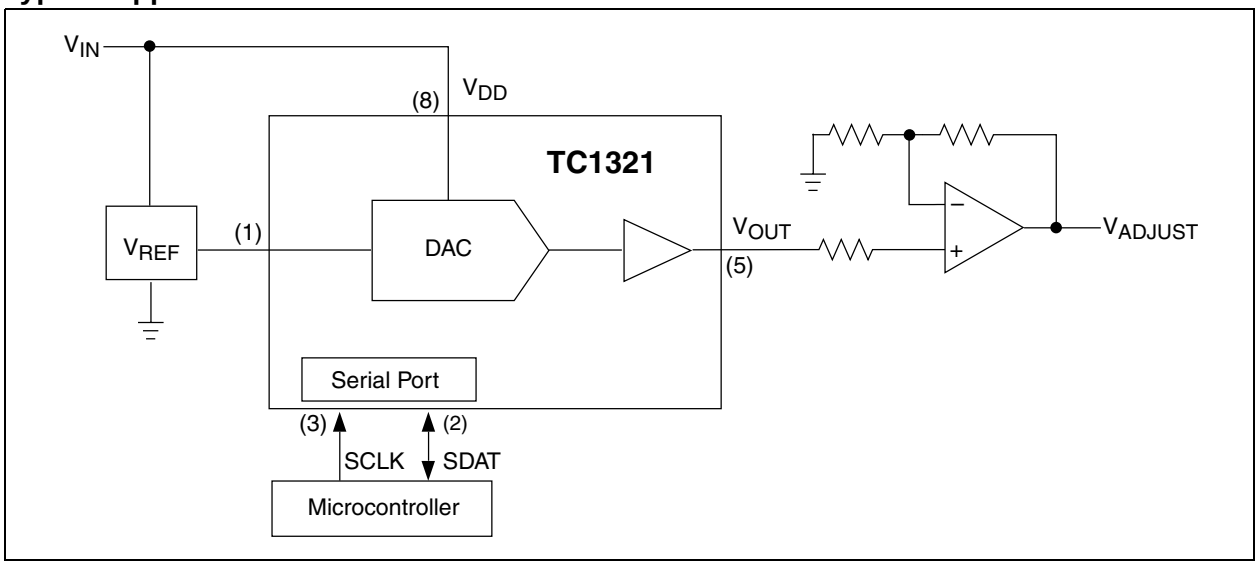
Communication with the TC1321 is accomplished via a simple 2-wire SMBus/I^{2}C compatible serial port, with the TC1321 acting as a slave only device. The host can enable the SHDN bit in the CONFIG register to activate the Low Power Standby mode.

Package Type

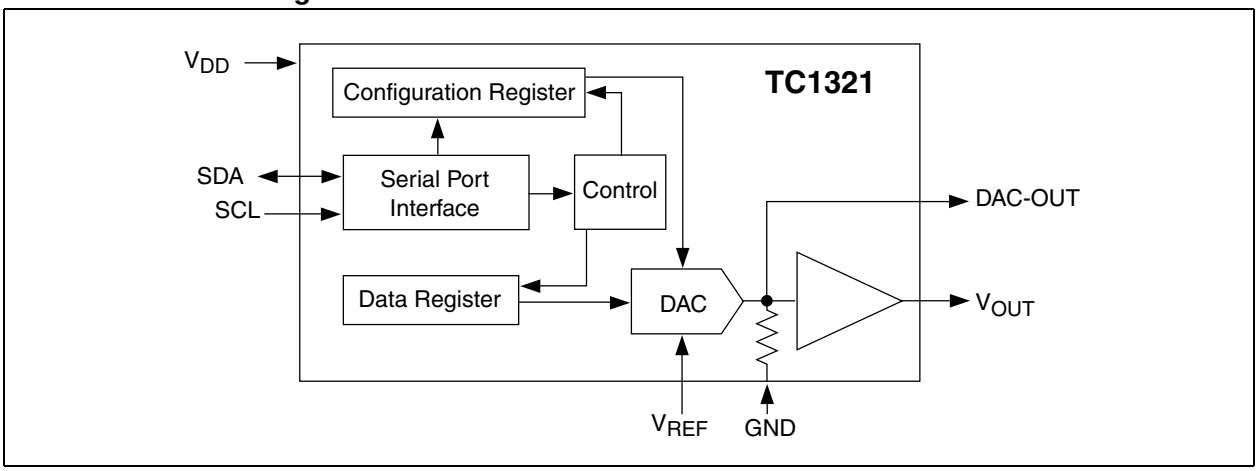
8-Pin MSOP and 8-Pin SOIC (Narrow)



Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD}) ..... +6V
Voltage on any Pin ... (GND – 0.3V) to (V_{DD} + 0.3V)
Current on any Pin ..... ±50mA
Package Thermal Resistance (θ_{JA})..... 330°C C/W
Operating Temperature (T_A)..... See Below
Storage Temperature (T_{STG})..... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1321 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 2.7V to 5.5V, -40°C ≤ T_A ≤ +85°C, V_{REF} = 1.2 unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power Supply						
V_{DD}	Supply Voltage	2.7	—	5.5	V	
I_{DD}	Operating Current	—	350	500	mA	V_{DD} = 5.5V, V_{REF} = 1.2V Serial Port Inactive **(Note 1)**
$I_{DD-STANDBY}$	Standby Supply Current	—	0.1	1	µA	V_{DD} = 3.3V Serial Port Inactive **(Note 1)**
Static Performance - Analog Section						
	Resolution	—	—	10	Bits	
INL	Integral Non-Linearity at FS, T_A = +25°C	—	—	±4.0	LSB	**(Note 2)**
FSE	Full Scale Error	—	—	±3	%FS	
DNL	Differential Non-Linearity, T_A = +25°C	-1	—	+2	LSB	All Codes **(Note 2)**
V_{OS}	Offset Error at V_{OUT}	—	±0.3	±8	mV	**(Note 2)**
TCV_{OS}	Offset Error Tempco at V_{OUT}	—	10	—	µv/°C	
PSRR	Power Supply Rejection Ratio	—	80	—	dB	V_{DD} at DC
V_{REF}	Voltage Reference Range	0	—	V_{DD} – 1.2	V	
I_{REF}	Reference Input Leakage Current	—	—	±1.0	µA	
V_{SW}	Voltage Swing	0	—	V_{REF}	V	V_{REF} ≤ (V_{DD} – 1.2V)
R_{OUT}	Output Resistance @ V_{OUT}	—	5.0	—	Ω	R_{OUT} (Ω)
I_{OUT}	Output Current (Source or Sink)	—	2	—	mA	
I_{SC}	Output Short-Circuit Current V_{DD} = 5.5V	— —	30 20	50 50	mA mA	Source Sink
Dynamic Performance						
SR	Voltage Output Slew Rate	—	0.8	—	V/µs	
t_{SETTLE}	Output Voltage Full Scale Settling Time	—	10	—	µsec	
t_{WU}	Wake-up Time	—	20	—	µs	
	Digital Feed Through and Crosstalk	—	5	—	nV-s	SDA = V_{DD}, SCL = 100kHz
Serial Port Interface						
V_{IH}	Logic Input High	2.4	—	V_{DD}	V	
V_{IL}	Logic Input Low	—	—	0.6	—	
V_{OL}	SDA Output Low	— —	— —	0.4 0.6	V V	I_{OL} = 3mA (Sinking Current) I_{OL} = 6mA
C_{IN}	Input Capacitance SDA, SCL	—	5	0.4	pF	
I_{LEAK}	I/O Leakage	—	—	±1.0	µA	

Note 1: SDA and SCL must be connected to V_{DD} or GND.
2: Measured at V_{OUT} ≥ 50mV referred to GND to avoid output buffer clipping.

TC1321 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.7V to 5.5V, -40°C ≤ T_A ≤ +85°C, V_{REF} = 1.2 unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Serial Port AC Timing						
f_{SMB}	SMBus Clock Frequency	10	—	100	kHz	
t_{IDLE}	Bus Free Time Prior to New Transition	4.7	—	—	µsec	
$t_{H(START)}$	START Condition Hold Time	4.0	—	—	µsec	
$t_{SU(START)}$	START Condition Setup Time	4.7	—	—	µsec	90% SCL to 10% SDA (for Repeated START Condition)
$t_{SU(STOP)}$	STOP Condition Setup Time	4.0	—	—	µsec	
$t_{H\text{-}DATA}$	Data In Hold Time	100	—	—	nsec	
$t_{SU\text{-}DATA}$	Data In Setup Time	100	—	—	nsec	
t_{LOW}	Low Clock Period	4.7	—	—	µsec	10% to 10%
t_{HIGH}	High Clock Period	4	—	—	µsec	90% to 90%
t_F	SMBus Fall Time	—	—	300	nsec	90% to 10%
t_R	SMBus Rise Time	—	—	1000	nsec	10% to 90%
t_{POR}	Power-on Reset Delay	—	500	—	µsec	$V_{DD} \geq V_{POR}$ (Rising Edge)

Note 1: SDA and SCL must be connected to V_{DD} or GND.

2: Measured at $V_{OUT} \geq 50mV$ referred to GND to avoid output buffer clipping.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Type	Description
1	V_{REF}	Input	Input. Voltage Reference Input can range from 0V to 1.2V below V_{DD}.
2	SDA	Bi-Directional	Bi-directional. Serial data is transferred on the SMBus in both directions using this pin.
3	SCL	Input	Input. SMBus serial clock. Clocks data into and out of the TC1321.
4	GND	Power	Ground.
5	V_{OUT}	Output	Output. Buffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register.
6	NC	None	No connection.
7	DAC-OUT	Output	Output. Unbuffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. This output is unbuffered and care must be taken that the pin is connected only to a high-impedance node.
8	V_{DD}	Power	Positive power supply input. See electrical specifications.

3.0 DETAILED DESCRIPTION

The TC1321 is a monolithic 10-bit digital-to-analog converter that is designed to operate from a single supply that can range from 2.7V to 5.5V. The DAC consists of a data register (DATA), a configuration register (CONF), and a current output amplifier. The TC1321 uses an external reference which also determines the maximum output voltage.

The TC1321 uses a current steering DAC based on an array of matched current sources. This current, along with a precision resistor, converts the contents of the Data Register and V_{REF} into an output voltage, V_{OUT} given by:

$$V_{OUT} = V_{REF} (DATA/1024)$$

3.1 Reference Input

The reference pin, V_{REF}, is a buffered high-impedance input and because of this, the load regulation of the reference source needs only to be able to tolerate leakage levels of current (less than 1µA). V_{REF} accepts a voltage range from 0 to (V_{DD} – 1.2V). Input capacitance is typically 10pF.

3.2 Output Amplifier

The TC1321 DAC output is buffered with an internal unity gain rail-to-rail input/output amplifier with a typical slew rate of 0.8V/µsec. Maximum full scale transition settling time is 10µsec to within ±1/2LSB when loaded with 1kΩ in parallel with 100pF.

3.3 Standby Mode

The TC1321 allows the host to put it into a Low Power (I_{DD} = 0.5µA, typical) Standby mode. In this mode, the D/A conversion is halted. The SMBus port operates normally. Standby mode is enabled by setting the SHDN bit in the CONFIG register. The table below summarizes this operation.

TABLE 3-1: STANDBY MODE OPERATION

SHDN Bit	Operating Mode
0	Normal
1	Standby

3.4 SMBus Slave Address

The TC1321 is internally programmed to have a default SMBus address value of 1001 000b. Seven other addresses are available by custom order (contact factory). See Figure 3-1 for location of address bits in SMBus protocol.

FIGURE 3-1: SMBus PROTOCOLS

Write 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	Data	ACK	P
	7-Bits	0		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Write 2-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	Data	ACK	Data	ACK	P
	7-Bits	0		8-Bits		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Read 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	S	Address	R/$\overline{W}$	ACK	Data	NACK	P
	7-Bits	0		8-Bits			7-Bits	1		8-Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data flow direction.

Data Byte: reads from the register set by the command byte.

Read 2-Byte Format

S	Address	R/$\overline{W}$	ACK	Command	ACK	S	Address	R/$\overline{W}$	ACK	Data	ACK	Data	NACK	P
	7-Bits	0		8-Bits			7-Bits	1		8-Bits		8-Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data flow direction.

Data Byte: reads from the register set by the command byte.

Receive 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Data	NACK	P
	7-Bits	1		8-Bits		

S = START Condition
P = STOP Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last read byte or write byte transmission.

Receive 1-Byte Format

S	Address	R/$\overline{W}$	ACK	Data	ACK	Data	NACK	P
	7-Bits	1		8-Bits		8-Bits		

S = START Condition
P = STOP Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last read byte or write byte transmission.

4.0 SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi-directional data port (SDA) form a 2-wire bi-directional serial port for programming and interrogating the TC1321. The following conventions are used in this bus architecture.

TABLE 4-1: TC1321 SERIAL BUS CONVENTIONS

Term	Explanation
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (START), generating the clock, and terminating transfers (STOP).
Slave	The device addressed by the master.
START	A unique condition signaling the beginning of a transfer indicated by SDA falling (High - Low) while SCL is high.
STOP	A unique condition signaling the end of a transfer indicated by SDA rising (Low - High) while SCL is high.
ACK	A Receiver Acknowledges the receipt of each byte with this unique condition. The Receiver drives SDA low during SCL high of the ACK clock pulse. The Master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
Not Busy	When the bus is IDLE, both SDA and SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers. (See START and STOP conditions.)

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The TC1321 *always* operates as a Slave. The serial protocol is illustrated in Figure 3-1. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a START condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a STOP Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is HIGH are reserved for START and STOP conditions).

4.1 START Condition (START)

The TC1321 continuously monitors the SDA and SCL lines for a START condition (a HIGH to LOW transition of SDA while SCL is HIGH), and will not respond until this condition is met.

4.2 Address Byte

Immediately following the START condition, the host must transmit the address byte to the TC1321. The 7-bit SMBus address for the TC1321 is `1001000`. The 7-bit address transmitted in the serial bit stream must match for the TC1321 to respond with an Acknowledge (indicating the TC1321 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write bit. This bit is a 1 for a read operation or 0 for a write operation. During the first phase of any transfer, this bit will be set = 0 to indicate that the command byte is being written.

4.3 Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TC1321. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the TC1321 to pull the SDA line LOW to Acknowledge that it successfully received the previous eight bits of data or address.

4.4 Data Byte

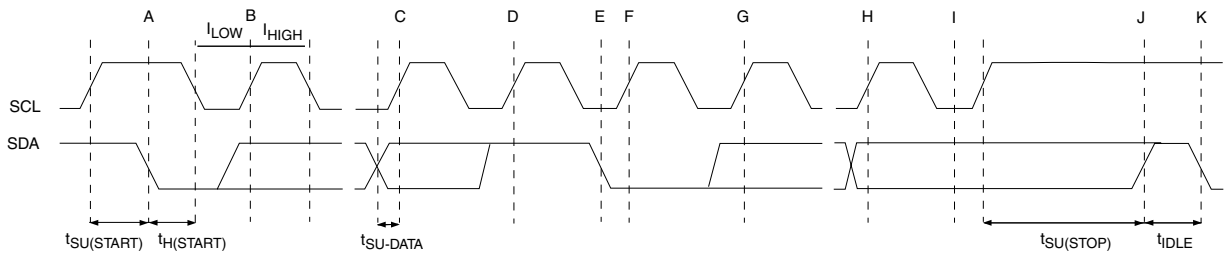
After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TC1321.

4.5 Stop Condition (STOP)

Communications must be terminated by a STOP condition (a LOW to HIGH transition of SDA while SCL is HIGH). The STOP condition must be communicated by the transmitter to the TC1321. Refer to Figure 4-1, Timing Diagrams for serial bus timing.

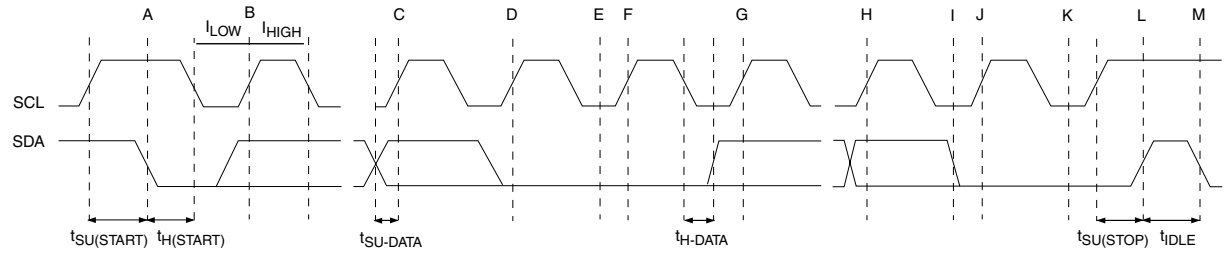
FIGURE 4-1: TIMING DIAGRAMS

SMBus Write Timing Diagram



A = START Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Master
H = LSB of Data Clocked into Master
I = Acknowledge Clock Pulse
J = STOP Condition
K = New START Condition

SMBus Read Timing Diagram



A = START Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Slave
H = LSB of Data Clocked into Slave
I = Slave Pulls SDA Line Low
J = Acknowledge Clocked into Master
K = Acknowledge Clock Pulse
L = STOP Condition, Data Executed by Slave
M = New START Condition

4.6 Register Set and Programmer's Model

TABLE 4-2: TC1321 COMMAND SET (SMBus READ_BYTE AND WRITE_BYTE)

Command Byte Description		
Command	**Code**	**Function**
RWD	00h	Read/$\overline{\text{Write}}$ Data (DATA)
RWCR	01h	Read/$\overline{\text{Write}}$ Configuration (CONFIG)

TABLE 4-3: CONFIGURATION REGISTER (CONFIG), 8-BIT, READ/WRITE

Configuration Register (CONFIG)							
D[7]	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**
Reserved							SHDN
Bit	**POR**	**Function**			**Type**	**Operation**	
D[0]	0	Standby Switch			Read/$\overline{\text{Write}}$	1 = Standby 0 = Normal	
D[7]-D[1]	0	Reserved; Always returns Zero when Read			N/A	N/A	

TABLE 4-4: DATA REGISTER (DATA), 10-BIT, READ/WRITE

Data Register (DATA) for 1st Byte							
D[9]	**D[8]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**
MSB	X	X	X	X	X	X	X
Data Register (DATA) for 2nd Byte							
D[1]	**D[0]**	X	X	X	X	X	X
X	LSB	X	X	X	X	X	X

The DAC output voltage is a function of reference voltage and the binary value of the contents of the register DATA. The transfer function is given by the expression:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left[\frac{DATA}{1024}\right]$$

4.7 Register Set Summary

The TC1321's register set is summarized in Table 4-5 below. All registers are 10-bits wide.

TABLE 4-5: TC1321 REGISTER SET SUMMARY

Name	Description	POR State	Read	Write
Data	DATA Register (2-Byte Format)	0000000000b	X	X
Config	CONFIG Register	0000 0000b	X	X

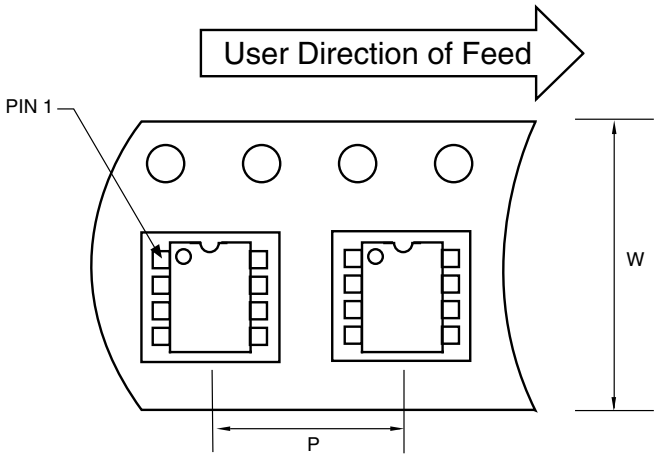
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Forms

Component Taping Orientation for 8-Pin MSOP Devices

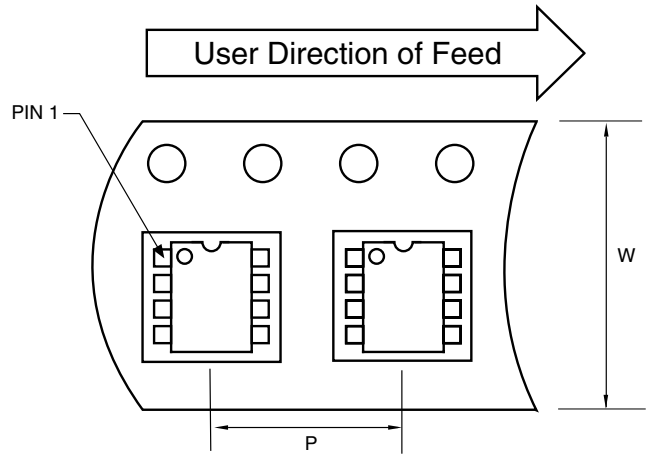


Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



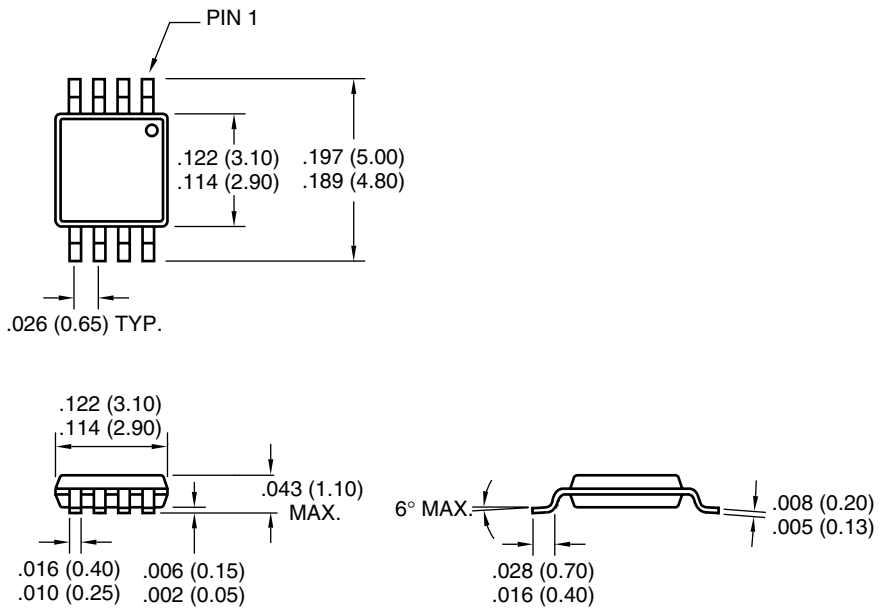
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

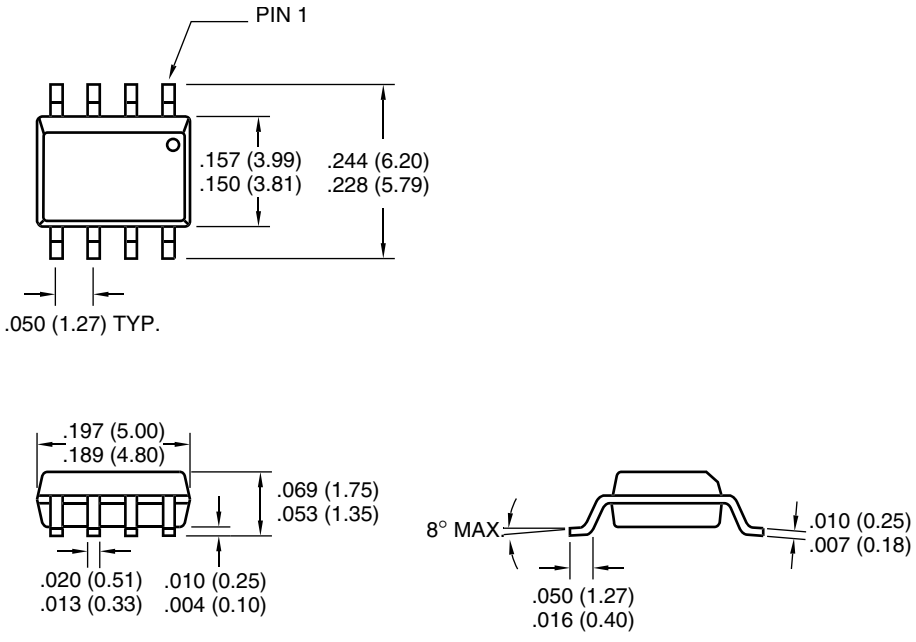
5.3 Package Dimensions

8-Pin MSOP



Dimensions: inches (mm)

8-Pin SOIC



Dimensions: inches (mm)

NOTES:

SALES AND SUPPORT

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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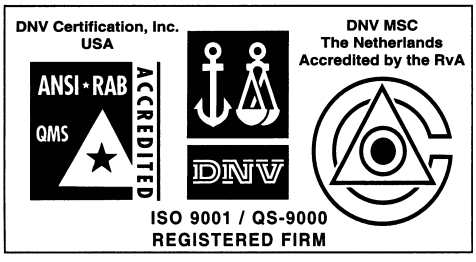

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