TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC

TC140G CMOS Gate Array

1.0 micron

Description

The TC140G series of 1.0 micron gate arrays has a 0.4ns gate speed and up to 172K raw gates.

— Provides a 35% reduction in delay times compared to 1.5 micron gate arrays

The TC140G is formed with a sea of gates architecture that uses a multilayer wiring technology and thus makes efficient use of silicon.

The TC140G is supported by the Toshiba Design Environment which embraces popular EWS and CAE systems. Toshiba has ASIC design centers around the United States and Canada to provide in-depth technical support.

Features

- Process: 1.0 micron drawn HC²MOS Si-gate double layer metal
- Raw gates: 2K to 172K
- Usable gates: up to 68K
- Gate speed: 0.4ns (2-input NAND gate, fanout - 2, tpd.) equivalent to 100K ECL
- Maximum toggle frequency: 200 MHz
- I/O pads: up to 360
- Output drive: up to 24mA
- Advanced packaging techniques: I/O cells are TAB compatible
- More flexible utilization of I/O: so even a high current driver only takes one bonding position
- Programmable I/O cells: with slew rate control
- Functional blocks of megacells and megafunctions
  - — Multiplier, barrelshifter, ALU, CLA
  - — LSI/VLSI CPU peripheral
- Building-block memory (32 to 16K bit)
  - — RAMs
  - — ROMs

Product Lines

Part Number	Gate [1] Complexity	Estimated [2] Usable Gates	Maximum I/O [3] Pads
TC140GH2	172,000	68,000	360 [4]
TC140GC8	128,000	51,000	312 [4]
TC140G89	89,000	35,000	260 [4]
TC140G68	68,000	27,000	228
TC140G54	54,000	21000	204
TC140G44	44,000	17,000	184
TC140G37	37,000	15,000	168
TC140G27	27,000	11,000	144
TC140G18	18,000	7,500	120
TC140G12	12,000	5,100	100
TC140G09	8,900	3,600	84
TC140G06	5,800	2,300	68
TC140G04	4,400	1,800	60
TC140G02	2,300	1,000	44

Notes: 1. Raw-gates.
2. Based on 40% array utilization. Actual utilization varies, depending on cell types used.
3. Additional I/O pads may be configured as V_{DD}/V_{SS}, subject to number and drive of output buffers.
4. I/O signals presently limited to 256 by tester capability.

TAEC

Absolute Maximum Ratings (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	− 0.3 to +7.0	V
V_{IN}	DC input voltage	− 0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	± 10	mA
T_{stg}	Storage temperature	− 40 to +125	°C

Recommended Commercial Operating Conditions (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	4.75 to 5.25	V
T_a	Ambient temperature	0 to +70	°C

DC Electrical Characteristics

Specified at V_{DD} = 5V ±5%, ambient temperature 0 to +70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage					V
	TTL level		2.2			
	TTL level SCHMITT trigger		2.2			
	CMOS level		3.5			
	CMOS level SCHMITT trigger		4.0			
V_{IL}	Low level input voltage					V
	TTL level				0.8	
	TTL level SCHMITT trigger				0.8	
	CMOS level				1.5	
	CMOS level SCHMITT trigger				1.0	
I_{IH}	High level input current	$V_{IN} = V_{DD}$	− 10		10	µA
	Input buffer with pull-down	$V_{IN} = V_{DD}$	10		200	
I_{IL}	Low level input current	$V_{IN} = V_{SS}$	− 10		10	µA
	Input buffer with pull-up	$V_{IN} = V_{SS}$	− 200		− 10	
V_{OH}	High level output voltage					V
	Type B1	I_{OH} = − 1mA	2.4			
	Type B2	I_{OH} = − 2mA	2.4			
	Type B4	I_{OH} = − 4mA	2.4			
	Type B6	I_{OH} = − 6mA	2.4			
	Type B8	I_{OH} = − 8mA	2.4			
	Type B12	I_{OH} = − 12mA	2.4			
	Type B18	I_{OH} = − 18mA	2.4			
	Type B24	I_{OH} = − 24mA	2.4			
		I_{OH} = − 1µA	V_{DD} − 0.05			
V_{OL}	Low level output voltage					V
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA			0.4	
	Type B4	I_{OL} = 4mA			0.4	
	Type B6	I_{OL} = 6mA			0.4	
	Type B8	I_{OL} = 8mA			0.4	
	Type B12	I_{OL} = 12mA			0.4	
	Type B18	I_{OL} = 18mA			0.4	
	Type B24	I_{OL} = 24mA			0.4	
		I_{OL} = 1µA			0.05	
I_{OZ}	High impedance leakage current		− 10		10	µA
	Output buffer with pull-up	$V_{OUT} = V_{DD}$ or V_{SS}	− 200		− 10	
	Output buffer with pull-down	$V_{OUT} = V_{DD}$ or V_{SS}	10		200	
VH	SCHMITT trigger hysteresis voltage					V
	TTL level			0.3		
	CMOS level			1.4		
I_{DD}	Quiescent supply current	$V_{IN} = V_{DD}$ or V_{SS}			100(1)	µA

Note: (1) Customer-design dependent.

TC140G Series Library

TC110G series-compatible macrocells and macrofunctions
- Macrocell performance optimization (standard/high drive)
- Macrocell equivalent to SSI/MSI

Functional blocks of Megacells, Megafunctions
- Multiplier, Barrelshifter, ALU, CLA
- LSI/VLSI CPU peripheral
- 2900 family

Building-block memory (32 to 16K bit)
- RAM cell
- ROM cell
- Customer-defined architecture

RAM

RAM-C single port RAM
- Asynchronous
- Separated I/O, 3 state output
- Max. 4608 bit/block (8 ~ 256 word × 4 ~ 36 bit)
- Read access time (t_{ACC}) 10ns typ.

RAM-E triple port RAM
- Asynchronous
- 2 read 1 write
- Max. 2304 bit/block (16 ~ 64 word × 4 ~ 36 bit)
- Read access time (t_{ACC}) 8ns typ.

ROM

ROM-A/B single port ROM
- Asynchronous
- Max. 16384 bit/block (64 ~ 1024 word × 2 ~ 32 bit)
- Read access time (t_{ACC}) 14ns/19ns typ.

Macrocells

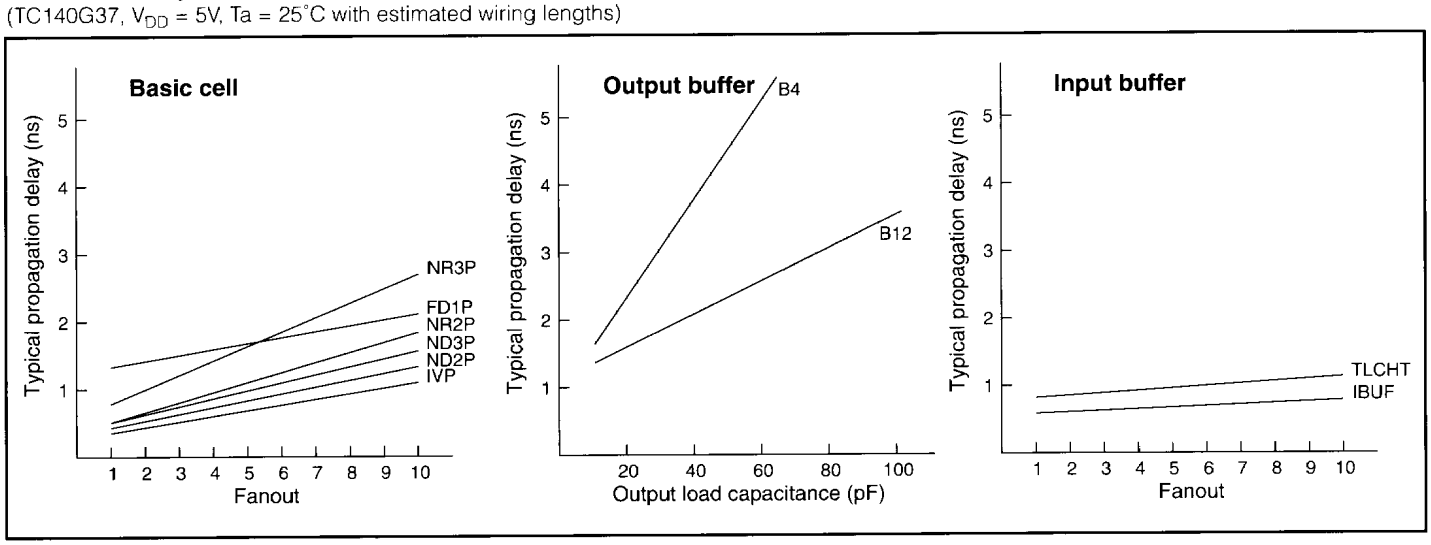
Logic gate	62
Inverter/internal buffer	23
Tri-state internal buffer	6
Delay buffer	6
Latch	21
Flip-flop	50
Decoder	8
Multiplexer	14
Adder	6
Input buffer	63
Output buffer	44
Bidirectional buffer	638
Oscillator	8
Total	**949**

Macrofunction List

Function	Types	
	74HC Series Compatible	Other
Adders	1	4
Comparators	2	6
Counters	11	19
Decoders	4	10
Flip-Flops	6	—
Gates	16	—
Multiplexers	10	11
Registers	16	19
Others	7	8
Total	**73**	**77**

Basic Cell Delay vs Fanout

(TC140G37, V_{DD} = 5V, Ta = 25°C with estimated wiring lengths)



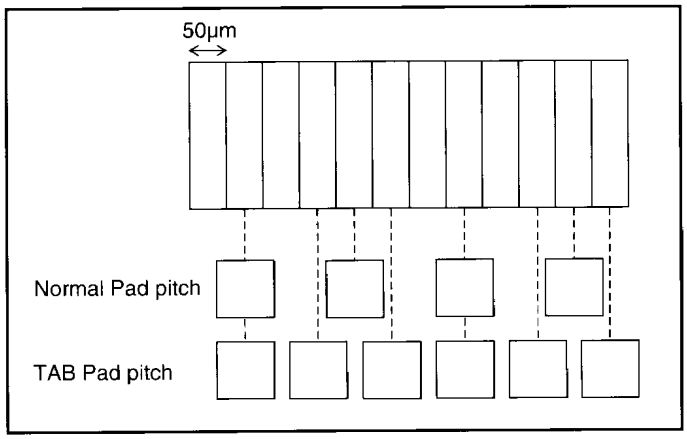
More efficient I/O utilization so you can optimize the use of bonding pads

How it works. In previous technologies the I/O slots were on the same 150µm pitch as the bonding pads.

However, in the TC140G and TC150G technology, the I/O slots are on 50µm centers, which enhances the available I/O slot options for the bonding pads. For normal bonding there are three I/O slots available for each bonding pad, allowing for a 24mA output buffer.

Even with a high current driver you only take one bonding position. With careful planning, unused I/O slots can be "borrowed" from adjacent bonding pads. For example, an 18mA bidirectional cell which requires four I/O slots (three for output and one for the input) could be placed next to an output that requires a 12mA drive capability which uses only two of its three allotted I/O slots.

Well suited for tab. This architecture is well suited for tab technology. The bonding pads for tab can be placed on 100µm centers with two I/O slots allocated to each pad. By doing so, drive currents are restricted to 12mA for outputs and 6mA for bidirectionals, but the number of bonding locations is increased by 50%.



Pad layout of I/O cell showing I/O structure for normal bonding (150µm pad pitch) and tab packaging (100µm pad pitch).

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