N- and P-Channel Enhancement-Mode Dual MOSFET

Features

- 500V breakdown voltage
- Independent N- and P-channels
- Electrically isolated N- and P-channels
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdowns
- Low input and output leakage

Applications

- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers

General Description

The Supertex TC1550 consists of a high voltage N-channel and P-channel MOSFET in an 8-Lead SOIC package. This is an enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS}		$R_{DS(ON)}$ (Max)	
	8-Lead SOIC *4.90x3.90mm body 1.75mm height (max) 1.27mm pitch*	N-Channel (V)	P-Channel (V)	N-Channel (Ω)	P-Channel (Ω)
TC1550	TC1550TG-G	500	-500	60	125

-G indicates package is RoHS compliant ('Green')

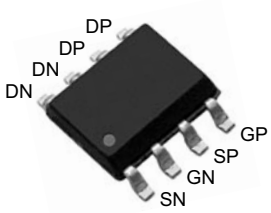
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to + 150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



8-Lead SOIC (TG)
(top view)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC (TG)

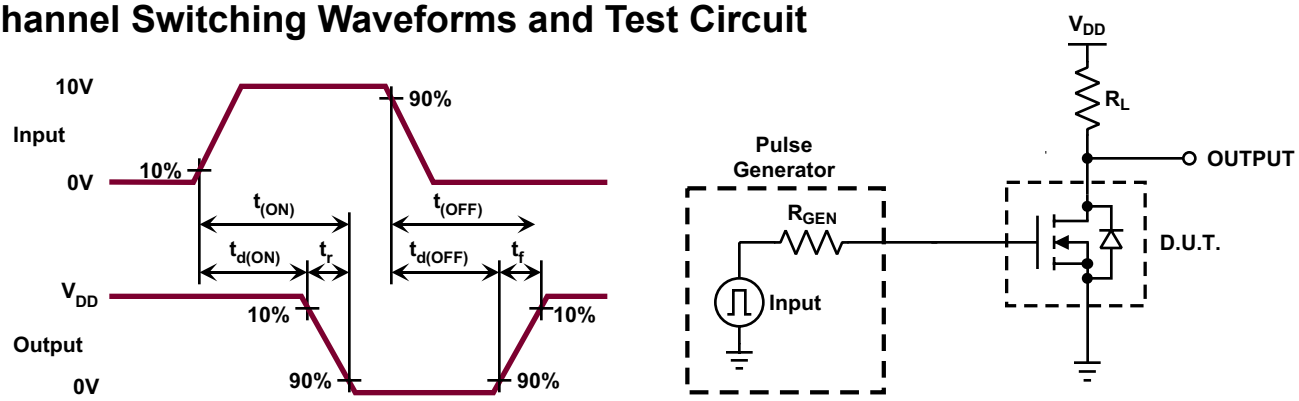
N-Channel Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	500	-	-	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate threshold voltage	2.0	-	4.0	V	V_{GS} = V_{DS}, I_D =1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-	100	-	mA	V_{GS} = 5.0V, V_{DS} = 25V
		150	350	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	45	-	Ω	V_{GS} = 5.0V, I_D = 50mA
		-	40	60		V_{GS} = 10V, I_D = 50mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	1.0	1.7	%/°C	V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward transconductance	50	100	-	mmho	V_{DS} = 25V, I_D =50mA
C_{ISS}	Input capacitance	-	45	55	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	8.0	10		
C_{RSS}	Reverse transfer capacitance	-	2.0	5.0		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	10		
t_f	Fall time	-	-	10		
V_{SD}	Diode forward voltage drop	-	0.8	-	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 500mA

Notes:

1. *All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse at 2% duty cycle.)*
2. *All AC parameters sample tested.*

N-Channel Switching Waveforms and Test Circuit



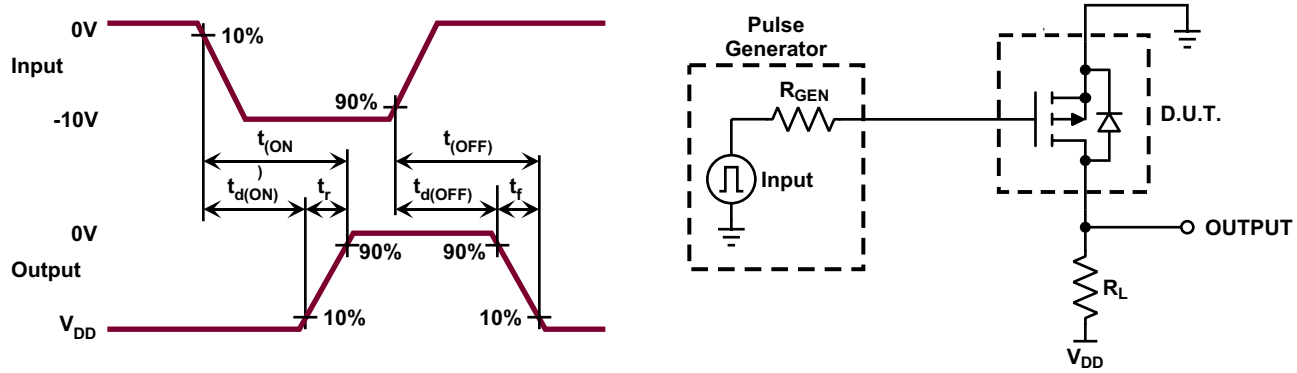
P-Channel Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-500	-	-	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate threshold voltage	-2.0	-	-4.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	3.5	6.0	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-	-90	-	mA	V_{GS} = -5.0V, V_{DS} = -25V
		-100	-240	-		V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	85	-	Ω	V_{GS} = -5.0V, I_D = -5.0mA
		-	80	125		V_{GS} = -10V, I_D = -10mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.85	-	%/°C	V_{GS} = -10V, I_D = -10mA
G_{FS}	Forward transconductance	25	40	-	mmho	V_{DS} = -25V, I_D = -10mA
C_{ISS}	Input capacitance	-	40	70	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	10	20		
C_{RSS}	Reverse transfer capacitance	-	3.0	10		
$t_{d(ON)}$	Turn-on delay time	-	5.0	10	ns	V_{DD} = -25V, I_D = -100mA, R_{GEN} = 25Ω
t_r	Rise time	-	8.0	10		
$t_{d(OFF)}$	Turn-off delay time	-	8.0	15		
t_f	Fall time	-	5.0	16		
V_{SD}	Diode forward voltage drop	-	-0.8	-1.5	V	V_{GS} = 0V, I_{SD} = -100mA
t_{rr}	Reverse recovery time	-	200	-	ns	V_{GS} = 0V, I_{SD} = -100mA

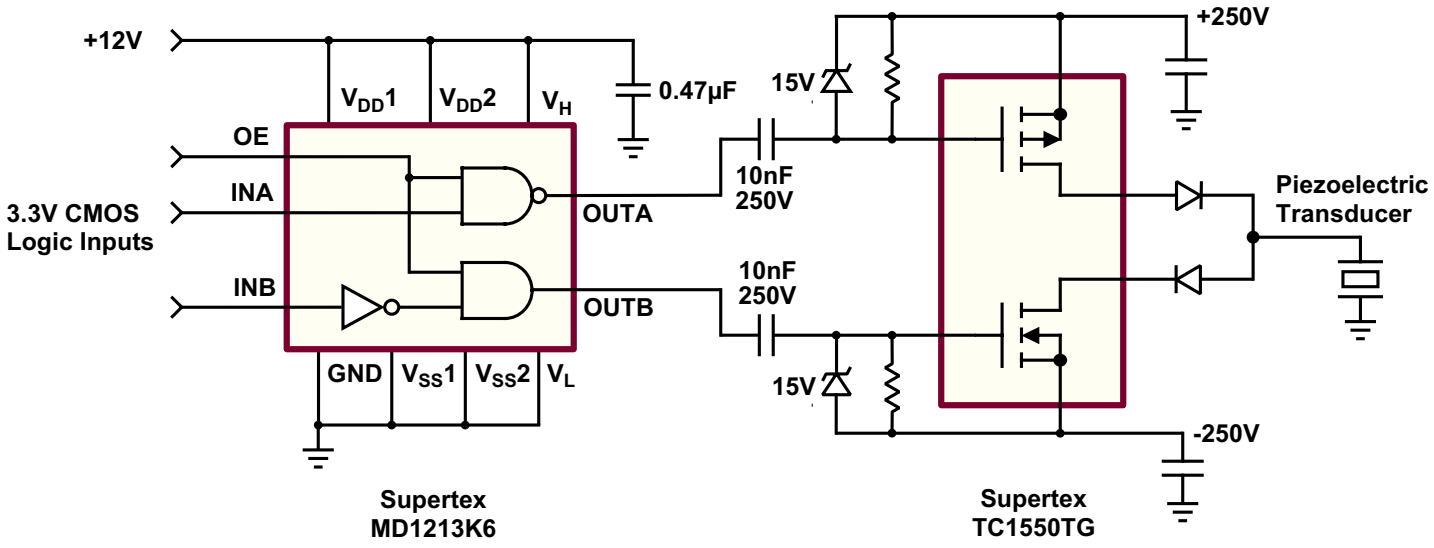
Notes:

1. *All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse at 2% duty cycle.)*
2. *All AC parameters sample tested.*

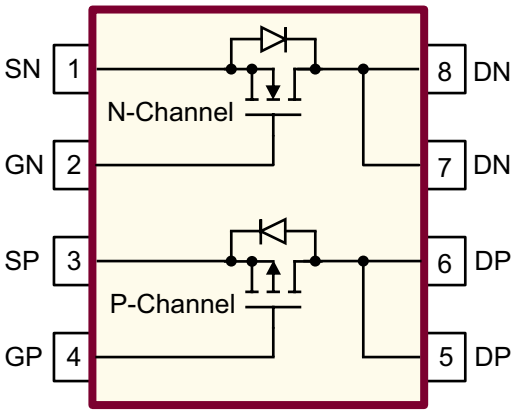
P-Channel Switching Waveforms and Test Circuit



Typical Application Circuit

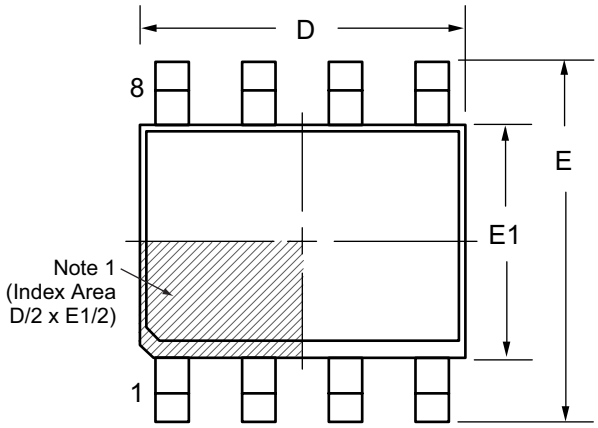


Block Diagram

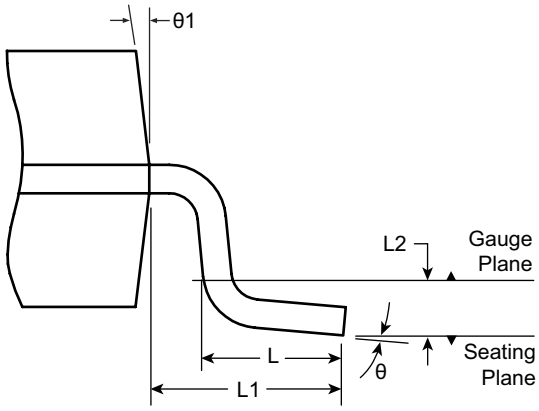


8-Lead SOIC (Narrow Body) Package Outline (TG)

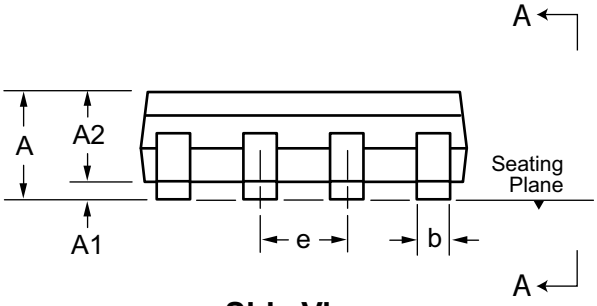
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



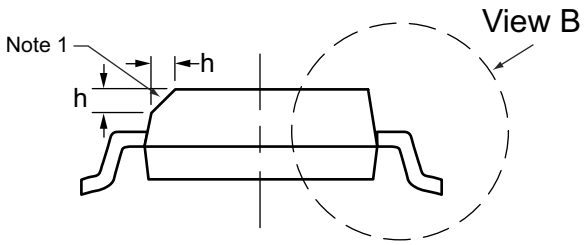
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-8SOLGTG, Version G090808.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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