CMOS CURRENT MODE PWM CONTROLLER

FEATURES

- **Isolated Output Drive**
- **Low Power CMOS Construction**
- **Low Supply Current ..... 2mA Typ.**
- **Wide Supply Voltage Operation ..... 8V to 18V**
- **Latch-Up Immunity ..... 500mA on Outputs**
- **Above and Below Rail Input Protection 6V**
- **High Output Drive ..... 500mA Peak**
- **Current Mode Control**
- **Fast Rise/Fall Time ..... 50nsec @ 1000pF**
- **High Frequency Operation 500kHz**
- **UV Hysteresis Guaranteed**
- **Programmable Current Limit**
- **Shutdown Pin Available**
- **Double Ended**
- **Soft Start**
- **Low Prop Delay Current Amp to Output ..... < 350nsec Typ.**
- **Low Prop Delay Shutdown to Output ..... < 400nsec Typ.**
- **TC38C46Pin Compatible with Unitrode UC3846**
- **ESD Protected ..... ±2 kV**

GENERAL DESCRIPTION

The TC38C46 is a current mode CMOS PWM control IC. It draws only 2 mA supply current, so it can be driven without a costly 50-60 Hz transformer. The output drive stage is capable of high drive currents, 300mA typical.

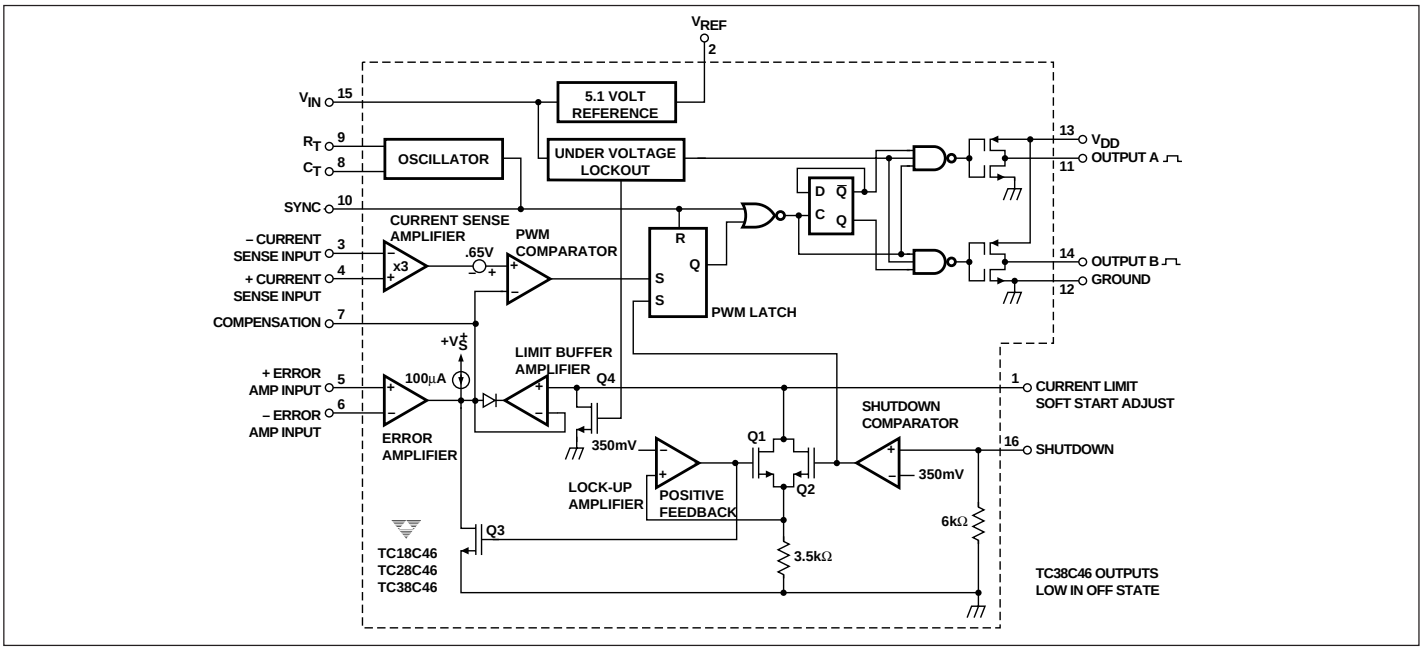
The TC38C46 is pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added.

This second generation part has been designed with an isolated drive stage. Unlike its cousin, the TC170, the output stage of the TC38C46 can be run from a separate power supply such as a secondary winding on an output transformer. This allows for bootstrap start-up of the power supply.

ORDERING INFORMATION

Part No.	Configuration	Pkg./Temperature
TC18C46MJE	Non-Inverting	16-Pin CerDIP – 55°C to +125°C
TC28C46EOE	Non-Inverting	16-Pin SOIC (Wide) – 40 °C to +85°C
TC28C46EPE	Non-Inverting	16-Pin Plastic DIP (Narrow) – 40°C to +85°C
TC38C46COE	Non-Inverting	16-Pin SOIC (Wide) 0°C to +70°C
TC38C46CPE	Non-Inverting	16-Pin Plastic DIP (Narrow) 0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



TC18C46
TC28C46
TC38C46

ABSOLUTE MAXIMUM RATINGS

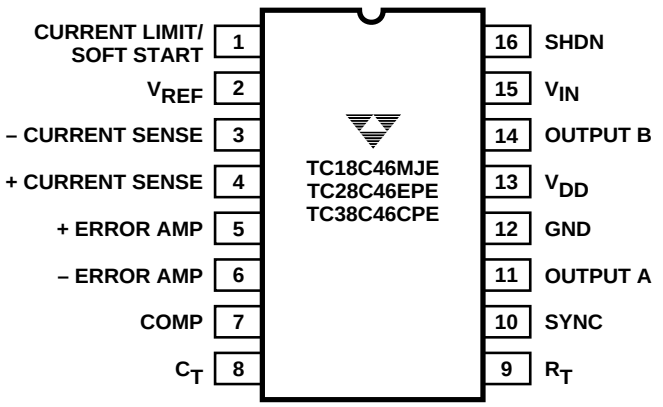
Output Current, Source or Sink (Pins 1, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... – 0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... – 30 mA
Sync Output Current (Pin 10) ..... – 5mA
Error Amplifier Output Current (Pin 7) ..... – 5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Supply Voltage 18V
Maximum Chip Temperature ..... 150°C
Storage Temperature ..... – 65°C to +150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C
Package Thermal Resistance
CerDIP $R_{\theta J-A}$ ..... 150°C/W
CerDIP $R_{\theta J-C}$ ..... 55°C/W
PDIP $R_{\theta J-A}$ ..... 125°C/W
PDIP $R_{\theta J-C}$ ..... 45°C/W
SOIC $R_{\theta J-A}$ ..... 250°C/W
SOIC $R_{\theta J-C}$ ..... 75°C/W

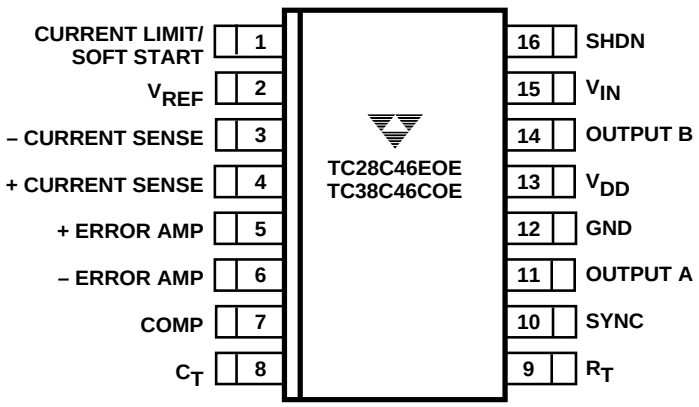
NOTES:
1. All voltages are with respect to Ground, Pin 12. Currents are positive into, negative out of the specified terminal.
2. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

16-Pin Plastic DIP (Narrow)
16-Pin CerDIP



16-Pin SOIC (Wide)



ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply for T_A = – 55°C to +125°C for TC18C46; – 40°C to +85°C for the TC28C46; and 0°C to +70°C for the TC38C46; $V_{IN} = V_{DD}$ = 16V; R_T = 30.1k; C_T = 270pF.

		TC18C46 TC28C46			TC38C46			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	T_f = 25°C, I_O = 1mA	5.0	5.1	5.2	5.0	5.1	5.2	V
Line Regulation	V_{IN} = 8V to 16V	—	±4	±20	—	±4	±20	mV
Load Regulation	I_O = 1mA to 10mA	—	±4	±20	—	±4	±20	mV
Temp Coefficient	Over Operating Range, (Note 1)	—	±0.2	±0.5	—	±0.2	±0.5	mV/°C
Total Output Range	Line, Load, and Temperature (Note 1)	4.97	—	5.24	4.94	—	5.26	V
Long Term Drift	T_f = 125°C, 1000 Hrs (Note 1)	—	±50	—	—	±50	—	mV
Short Circuit Output Current	V_{REF} = 0V	20	—	70	20	—	70	mA
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, Tf = 25°C (Note 1)	—	22	—	—	22	—	µV(rms)
Oscillator Section								
Initial Accuracy	T_f = 25°C	96.5	102	106.5	96.5	101	106.5	kHz
Voltage Coefficient	V_{IN} = 8V to 16V	—	±.1	2.0	—	±.1	±1.5	%/V
Temp Coefficient	Over Operating Range (Note 1)	—	±.04	±0.06	—	±.04	±0.06	%/°C
Clock Ramp Reset Current		1.2	2	3	1.2	2	3	mA
Osc Ramp Amplitude		3.6	3.8	4	3.6	3.8	4	V
Sync Output High Level	(Note 1)	V_{DD} –0.5	—	—	V_{DD} –0.5	—	—	V
Sync Output Low Level	(Note 1)	—	—	0.5	—	—	0.5	V
Sync Input High Level	Pin 8 = 0V, (Note 1)	—	8.5	—	—	8.5	—	V
Sync Input Low Level	Pin 8 = 0V, (Note 1)	—	8.5	5	—	8.5	5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	—	±5	±50	—	±5	±50	nA
Error Amp Section								
Input Offset Voltage		—	±5	±25	—	±5	±25	mV
Input Bias Current		—	±10	±100	—	±0.1	±0.5	nA
Input Offset Current		—	±10	±100	—	±0.1	±0.5	nA
Open Loop Voltage Gain	ΔV_O = 1V to 6V, R_L = 100k	70	90	—	70	90	—	dB
Gain Bandwidth Product	T_f = 25°C (Note 1)	0.7	1	—	0.7	1	—	MHz
CMRR	V_{CM} = 0V to 11V	70	90	—	70	90	—	dB
PSRR	V_{IN} = 8V to 16V	70	90	—	70	90	—	dB
Output Sink Current	V(EA –) = 5V, V(EA+) = 4.9V, V(CMPTR) = 1.2V	2	4	—	2	4	—	mA
Output Source Current	V(EA –) = 5V, V(EA+) = 5.1V, V(CMPTR) = 2.5V	5	10	—	5	10	—	mA
High Level Output Volt	R_L = (CMPTR) 5kΩ to GND, A_{CL} = 300	4.75	4.9	5.1	4.75	4.9	5.1	V
Low Level Output Volt	R_L = (CMPTR) 5kΩ to GND, A_{CL} = 300	—	0.4	0.9	—	0.4	0.9	V
Slew Rate		1.3	2	—	1.3	2	—	V/µsec

ELECTRICAL CHARACTERISTICS (Cont)**:** Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46; – 40°C to +85°C for the TC28C46; and 0°C to +70°C for the TC38C46; $V_{IN} = V_{DD}$ = 16V; R_T = 30.1k; C_T = 270pF.

		TC18C46 TC28C46			TC38C46			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Current Sense Section								
Amplifier Gain	(Notes 2, 3)	2.7	3	3.6	2.7	3	3.4	V/V
Max Differential Input Signal ($V_{Pin\ 4}$-$V_{Pin\ 3}$)	(Note 2)	1.1	1.5	1.8	1.1	1.5	1.8	V
Input Offset Voltage	(Note 2)	0.4	0.65	0.85	0.4	0.65	0.85	V
CMRR	V_{CM} = 1V to 12V, (Note 2)	40	60	—	40	60	—	dB
PSRR	V_{IN} = 8V to 16V, (Note 2)	40	60	—	40	60	—	dB
Input Bias Current	(Note 1)	—	±1	±100	—	±1	±100	nA
Input Offset Current	(Note 1)	—	±0.1	±2	—	±0.1	±2	nA
Input Common Mode Range	(Note 1)	0	—	11	0	—	11	V
Delay to Outputs	T_f = 25°C, (Note 1)	150	225	400	150	225	400	nsec
Current Limit Adjust Section								
Current Limit Voltage Offset	—	±1	±25	—	±1	±25	mV	
Input Impedance	(Shutdown Unlatched)	3	3.5	4	3	3.5	4	kΩ
Shutdown Terminal Section								
Threshold Voltage		320	360	400	320	360	400	mV
Input Voltage Range	(Note 1)	0	—	V_{IN}	0	—	V_{IN}	V
Min Latching Current ($I_{Pin\ 1}$)	(Note 4)	140	—	—	140	—	—	µA
Max Non-Latching Current (I_{Pin1})	(Note 5)	—	—	60	—	—	65	µA
Min Pulse Width	(Note 1)	100	50	—	100	50	—	nsec
Delay to Outputs	(Note 1)	125	250	400	125	250	400	nsec
Output Section								
Output Low Level $r_{DS\ (ON)}$	I_{SINK} = 20mA	—	10	20	—	10	20	Ω
Output High Level $r_{DS\ (ON)}$	I_{SOURCE} = 20mA	—	20	35	—	20	35	Ω
Output Rise Time	C_L = 1 µF	—	55	90	—	55	90	nsec
Output Fall Time	C_L = 1 µF	—	55	90	—	55	90	nsec
Undervoltage Lockout Section								
Undervoltage Threshold		6.5	7	7.3	6.5	7	7.3	V
Start Threshold		7.4	7.8	8	7.4	7.8	8	V
Threshold Hysteresis		0.6	0.8	1	0.6	0.8	1	V
Total Standby Current								
Supply Current		—	1.2	2.5	—	1.2	2	mA
Start-Up Current		—	250	350	—	250	350	µA

NOTES: 1. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.
2. Parameter measured at trip point of latch with $V_{Pin\ 6} = V_{REF}$, $V_{Pin\ 16}$ = 0V.
3. Amplifier gain is defined as:

$$G = \frac{\Delta VPin\ 7}{\Delta VPin\ 4};\ \Delta VPin\ 4 = 0V \text{ to } 1V$$

4. Current into Pin 1 guaranteed to latch circuit in shutdown state.
5. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

Peak Current Limit Setup

Resistors R1 and R2 at the CURRENT LIMIT input (pin 1) set the peak current limit (Figure 1). The potential at pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for $(V_{REF} – 0.35)/R1 < 65\mu A$ and is latched for currents greater than 140µA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.

I_{PCL}, the peak current limit, is the current that causes the PWM comparator noninverting input to exceed V1, the potential at the inverting input. Once the comparator trip point is exceeded, both outputs are disabled.

I_{PCL} is easily calculated:

$$I_{PCL} = \frac{V1 – 0.65V}{3\ (RS)}$$

where:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

V_{REF} = Internal voltage reference = 5.1V

3 = Gain of current-sense amplifier

0.65V = Current limit offset

Both driver OUTPUTs (pins 11 and 14) are OFF (LOW) when the peak current limit is exceeded. When the sensed current goes below I_{PCL}, the circuit operates normally.

Output Shutdown

The outputs can be turned OFF quickly through the SHUTDOWN input (pin 16). A signal greater than 360 mV at pin 16 forces the shutdown comparator output HIGH. The PWM latch is held set, disabling the outputs.

Q2 is also turned ON. If $V_{REF}/R1$ is greater than 140µA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.65V. Q3 remains ON even after the shutdown input signal is removed. This is because the lock-up amplifier is in latched mode driving Q3 ON. This state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at pin 1 is below 0.65V.

The shutdown terminal gives a fast, direct way to disable the PWM controller output transistors. System protection and remote shutdown applications are possible.

The input pulse to pin 16 should be at least 100nsec wide and have an amplitude of at least 1V in order to get the minimum propagation delay from input to output. If these parameters are met, the delay should be less than 400nsec at 25°C; however, the delay time will increase as the device temperature rises.

Soft Restart From Shutdown

A soft restart can be programmed if nonlatched shutdown operation is used.

A capacitor at pin 1 will cause a gradual increase in potential toward V1. When the voltage at pin 1 reaches 0.75V, the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it is necessary to insert a capacitor between pin 1 and ground if the current I_L is greater than 140µA. This capacitor will prevent "noise triggering" of the latch, yet minimize the soft-start effect.

Soft-Start Power-Up

During power-up, a capacitor at R1, R2 initiates a soft-start cycle. As the input voltage (pin 15) exceeds the under-voltage lockout potential (7V), Q4 is turned OFF, ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.65V, both outputs are disabled.

When the undervoltage lockout start threshold is exceeded, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current-Sense Amplifier

The current-sense amplifier operates at a fixed gain of 3. Maximum differential input voltage ($V_{PIN4}–V_{PIN3}$) is 1.1V. Common-mode input voltage range is 0V to $V_{IN} – 3V$.

Resistive-sensing methods are shown in Figure 2. In Figure 2(A), a simple RC filter limits transient voltage spikes at pin 4, caused by external output transistor-collector capacitance. Transformer coupling (Figure 3) offers isolation and better power efficiency, but cost and complexity increase.

In order to minimize the propagation delay from the input to the current amplifier to the output terminals, the current ramp should be in the order of 1µsec in width (min). Typical time delay values are in the 225nsec region at 25°C. The delay time increases with device temperature so that at 50°C, the delay times may be increased by as much as 100nsec.

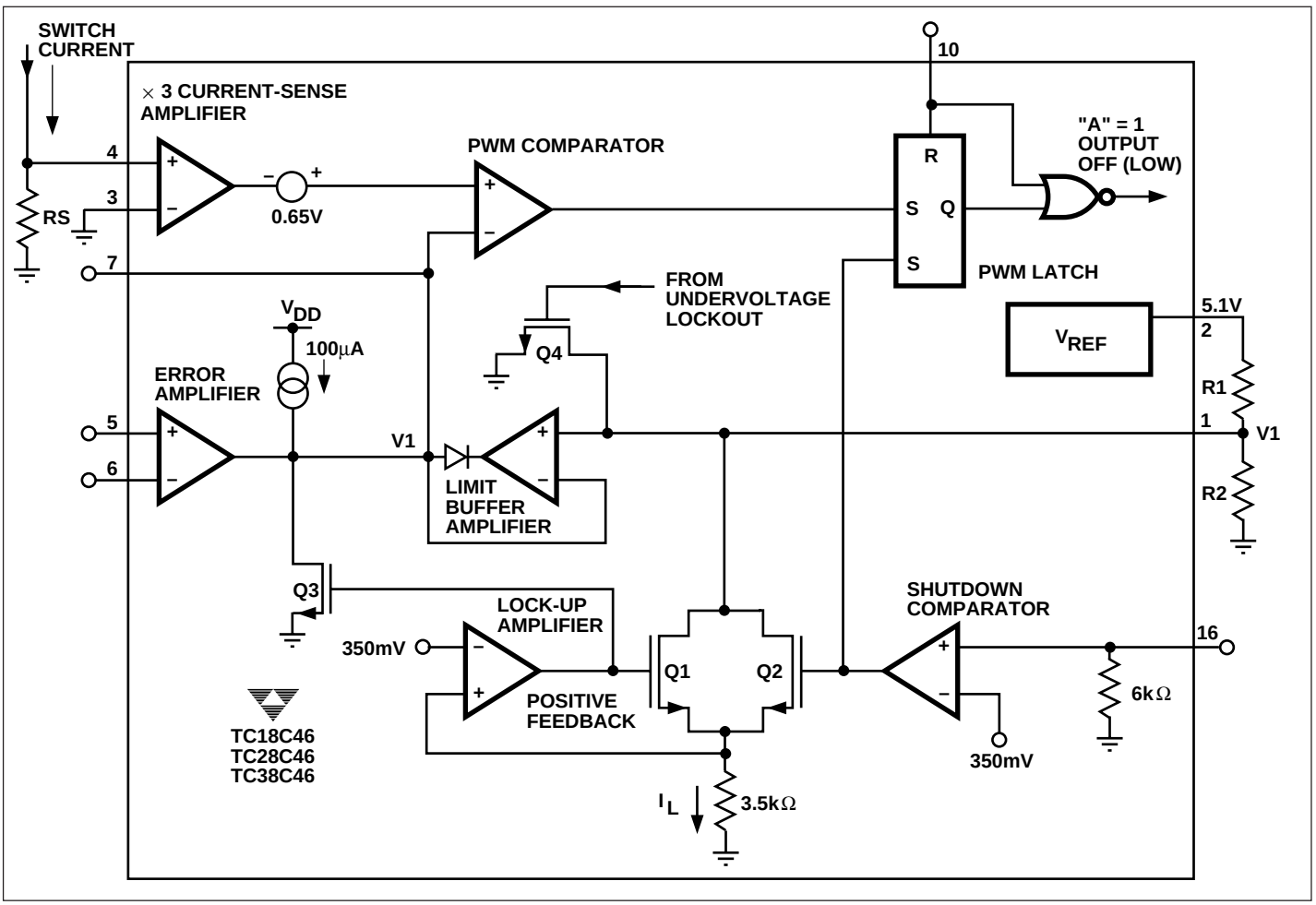


Figure 1. R1 and R2 Set Maximum Peak Output Current

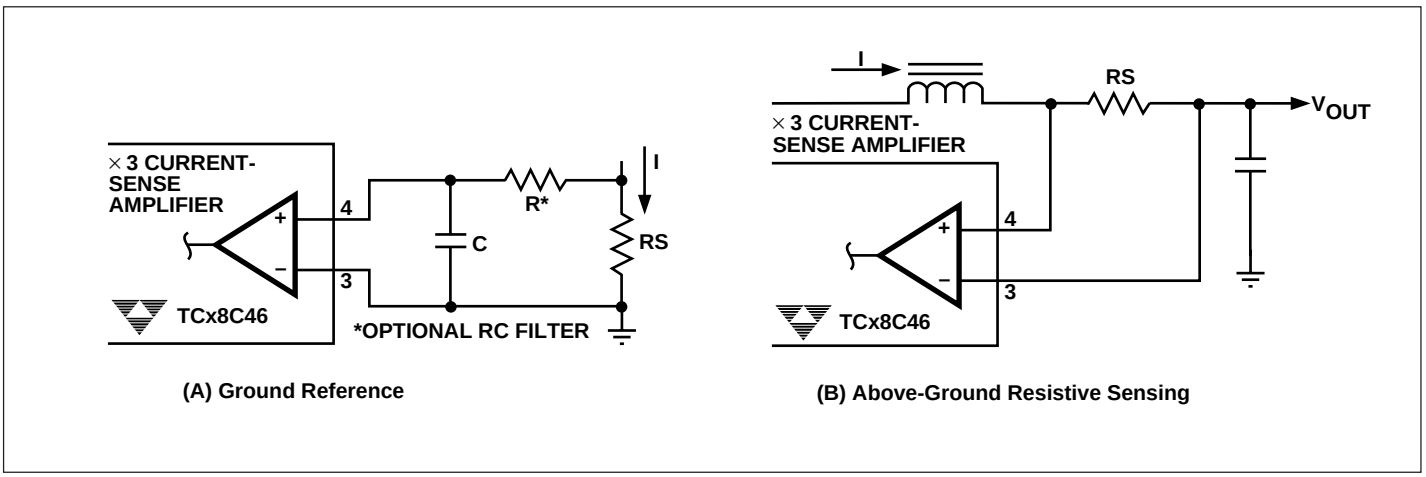


Figure 2. Resistive Sensing

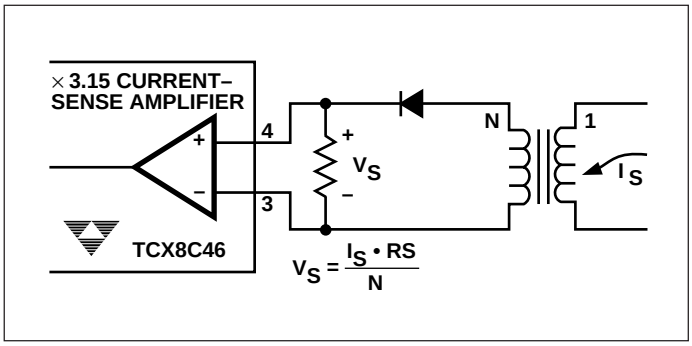


Figure 3. Transformer Isolated Current Sense

Under Voltage Lockout

The under voltage lockout circuit forces the PWM controller outputs OFF (LOW) if the supply voltage is below 7V. Threshold hysteresis is 0.8V and guarantees clean, jitter-free turn-ON and turn-OFF points. The hysteresis also reduces capacitive filtering requirements at the PWM controller supply input (pin 15).

Circuit Synchronization

Current-mode-controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage-mode controllers unequally share the load current, decreasing system reliability.

Two or more of these PWM controllers can be slaved together for parallel operation. Circuits can operate from a master PWM controller internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding pin 8. Slave controllers derive an oscillator from the bidirectional synchronization output signal at pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver, a buffer is required (Figure 4). In order to use pin 10 as a sync input, it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_S. Since V_S must be above 7V for the undervoltage lockout to be disabled, a CMOS or open-collector TTL driver should be used.

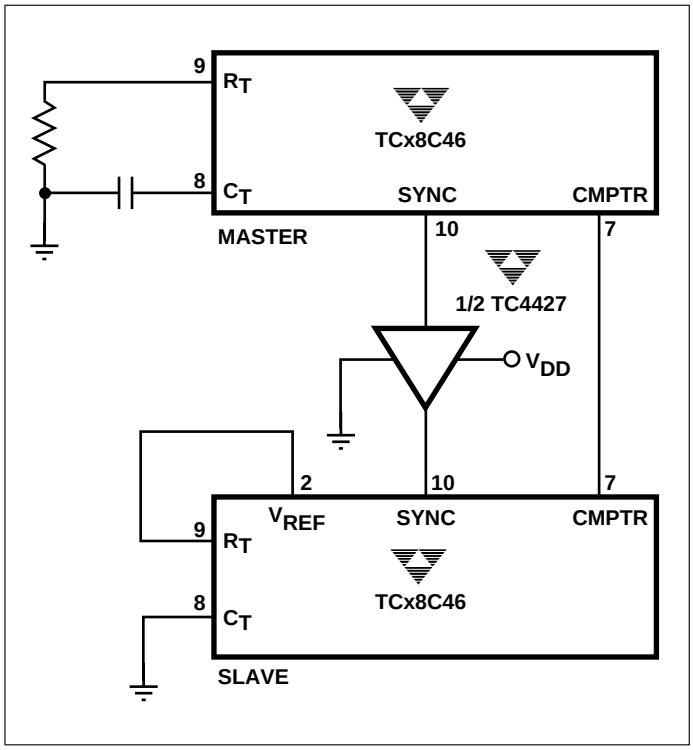


Figure 4. Master/Slave Parallel Operation

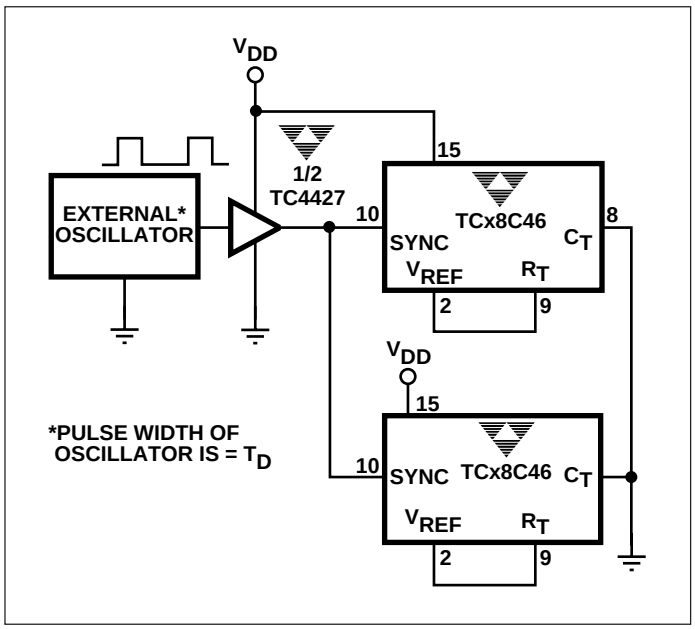


Figure 5. External Clock Synchronization

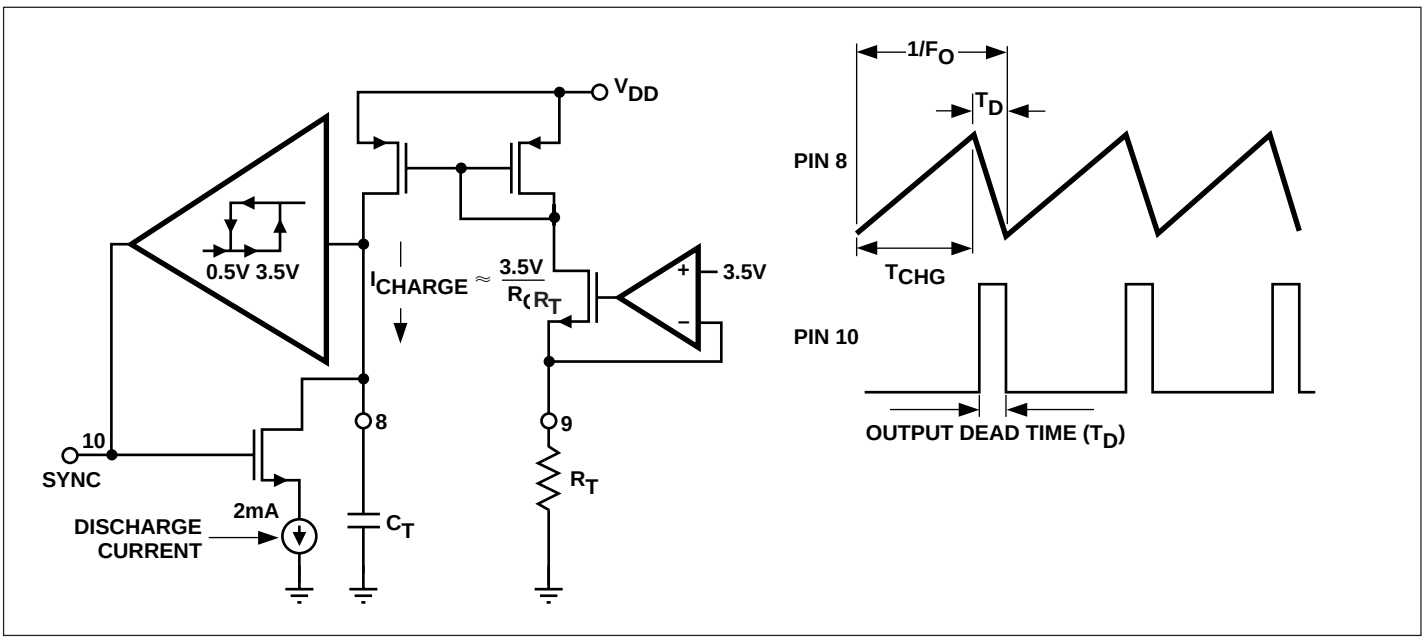


Figure 6. Oscillator Circuit

Selection of Timing Capacitor and Resistor (C_T & R_T)

1) First determine the frequency of operation F_O and the desired " dead" time", T_D (see Fig.6 graph).

We need to choose R_T and C_T.

2) The current mirror in Fig. 6 , shows:

$$I_{CHG} = \frac{3.5\ V}{R_T} \quad . \quad \text{Also,}$$

$$I_{CHG} = C_T \frac{\Delta V}{\Delta T} \quad \text{Where,} \quad \Delta V = 3.5 - 0.5 = 3.0 \text{ Volts}$$

and $\Delta T = T_{CHG}$

3) During discharge (T_D), the discharge current pulls 2 m A out of C_T, minus the I_{CHG} that keeps trying to charge it:

$$2\text{ m A} - I_{CHG} = C_T \frac{\Delta V}{\Delta T} \text{ ,where } \Delta V = 3.0 \text{ Volts}, \quad \Delta T = T_D$$

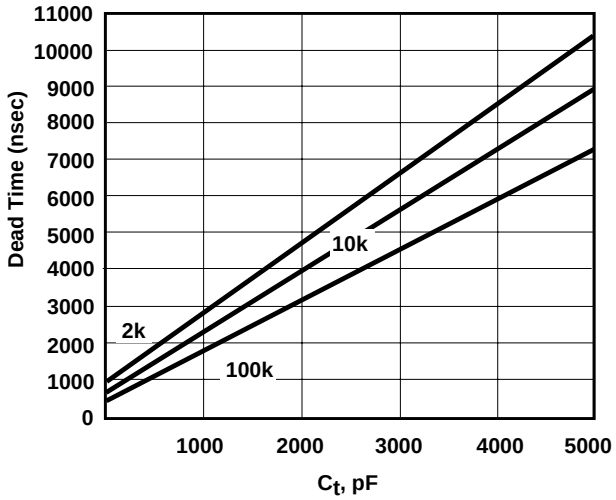
Substituting and rearranging,

$$C_T = \frac{T_D}{3} \quad \frac{(.002 - 3.5)}{R_T}$$

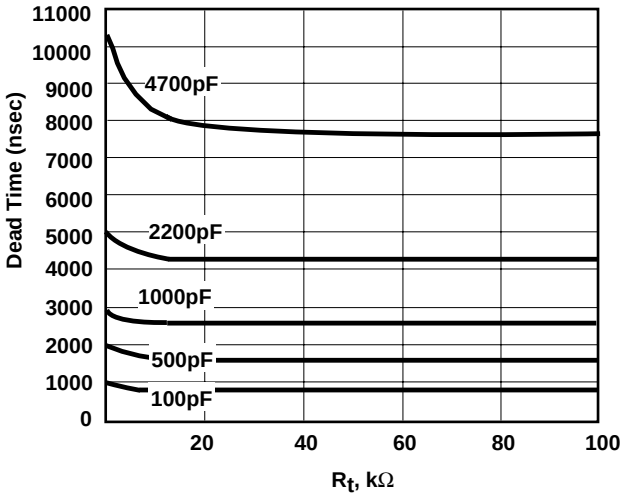
Knowing T_D choosing R_T permits calculation of C_T .

TYPICAL CHARACTERISTICS

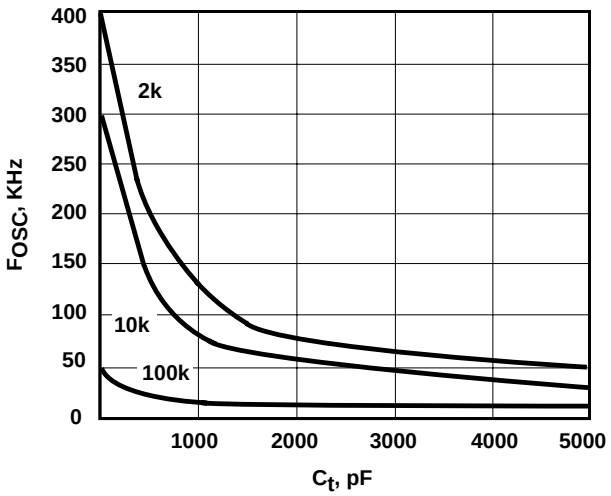
18C46 Dead Time vs. C_t



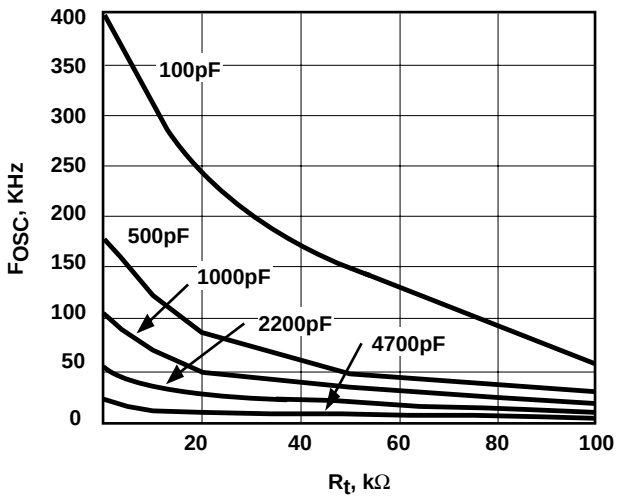
18C46 Dead Time vs. R_t



18C46 OSC Frequency vs. C_t



18C46 OSC Frequency vs. R_t



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PIN DESCRIPTION

Pin No.	Symbol	Description
1	CURRENT LIMIT, SOFT START	Pin for setting the peak current limit threshold of sense inputs pin 3 and pin 4. A second function of this pin is for Soft-Start programming with a capacitor between this pin and ground, pin 12.
2	V_{REF}	Pin is an output for the reference supply voltage of 5.1 volts. This reference can supply a minimum of 20mA of output current.
3	– CURRENT SENSE	Pin is the current sense inverting input for sensing peak current of the pass transistor through the series current monitor resistor.
4	+ CURRENT SENSE	Pin is the non-inverting input for sensing peak current of the pass transistor. The positive end of the current sense resistor is connected here.
5	+ ERROR AMP	Pin is the non-inverting input for sensing voltage feedback from output for voltage regulation.
6	– ERROR AMP	Pin is the inverting input for sensing the reference voltage to regulate the output.
7	COMPENSATION	Pin for compensating the feedback loop response.
8	C_T	Pin is the input for timing capacitor, C_T, to set oscillator frequency in conjunction with 9 resistor R_T, input. A second function is for setting the crossover dead time of the outputs, pins 11 and 14.
9	R_T	Pin is the input for the timing resistor, R_T, to set oscillator frequency by setting the (constant) current charge rate for capacitor C_T.
10	SYNC	Pin is the input or output for the oscillator synchronization pulse.
11	OUT_A	Pin is the output drive of phase A to drive push pull transistor A.
12	GND	Pin is the ground return path for all input and output signals.
13	V_{DD}	Pin is the supply power input terminal for the output drivers.
14	OUT_B	Pin is the output drive of phase B to drive push pull transistor B.
15	V_{IN}	Pin is voltage bias supply input for all circuits except the output drivers
16	SHUT	Pin is an input for shutdown when a 350mV threshold is exceeded: both output drives will then be terminated.