

Toshiba's 1 Mbit embedded DRAM core is available for the TC220C and TC220E product families. Each DRAM cell is based on a three transistor structure as shown in Figure 1. This multi-feature DRAM core is easily integrated into a broad range of applications through utilization of different core configurations.

DRAM Core Features

- Power supply: 3.3V ±0.3V
- Memory configurations
 - 128K x 8 bit
 - 64K x 16 bit
 - 32K x 32 bit
 - 16K x 64 bit
- Full address without multiplex
- Separate data input and output
- Read access modes
 - Random access
 - EDO/Hyper page mode
- Refresh scheme
 - $\overline{\text{RAS}}$ only refresh
 - CBR ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) refresh
- Performance specification
 - trc random read cycle: 50 ns
 - tpc page mode read cycle: 25 ns
 - Refresh cycle: 256 cycles/ms (@T_j = 85°C)

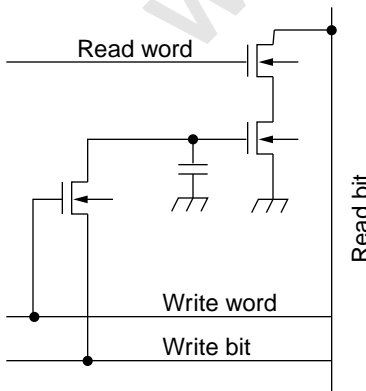


Figure 1. Three-Transistor DRAM Cell

Embedded DRAM Benefits

Benefits derived from integration of DRAM with logic are:

- Flexibility in utilizing different DRAM core configurations based on the application requirement
- Memory access time lower than discrete packaged devices
- Elimination of a large number of pins and associated packages, effectively reducing circuit board area
- Lower power consumption since systems with fast and wide memory busses will dissipate significantly less power due to lower capacitance on-chip connections
- Lower switching noise on data bus between memory and logic

Target Applications

Applications for 3T dRAMASIC™ include hard disk drive controllers, buffer memory for hubs and switches and printers.

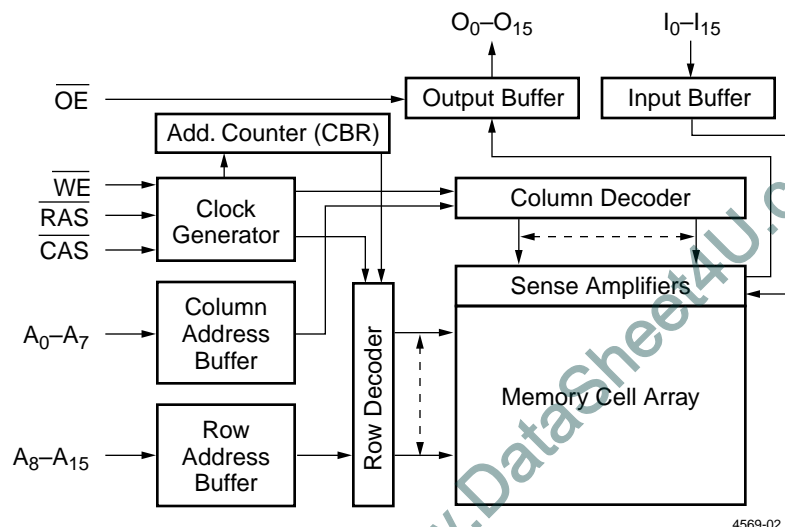


Figure 2. DRAM Core Block Diagram

Timing Diagrams

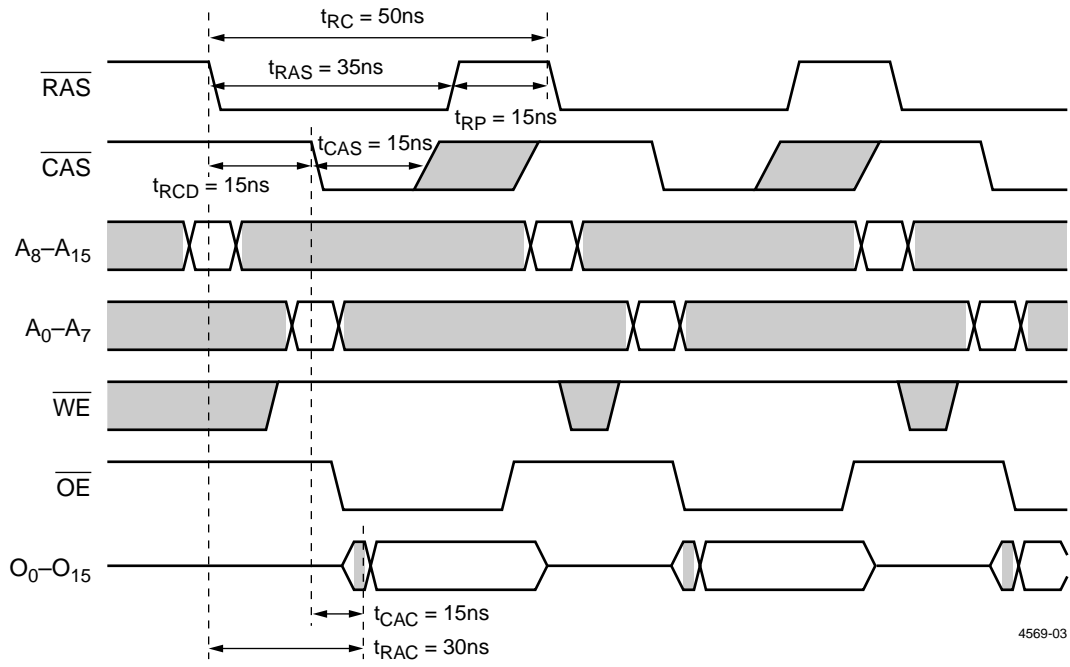


Figure 3. Random Mode Read Cycle

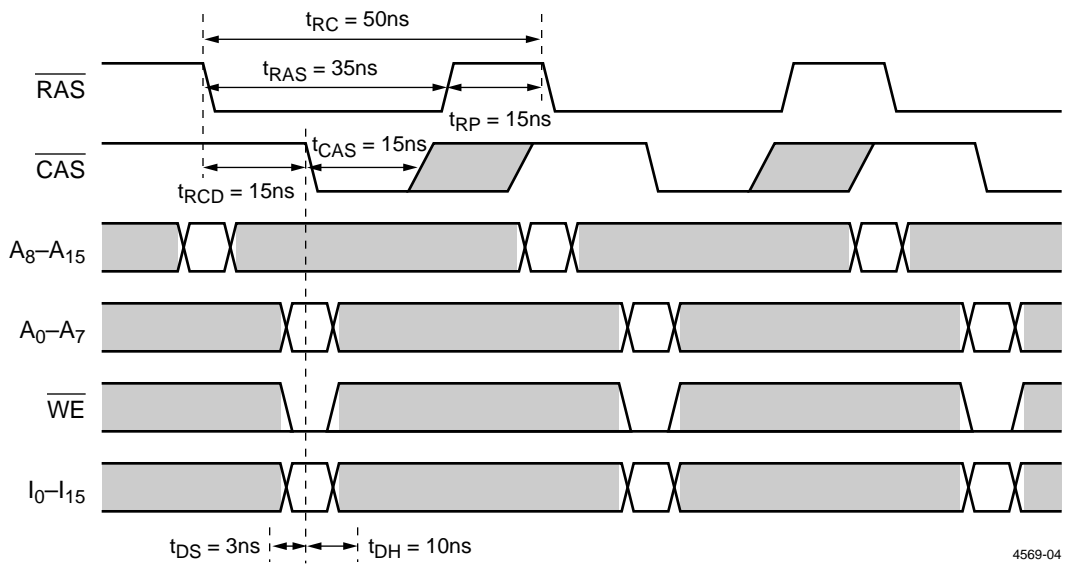


Figure 4. Random Mode Write Cycle

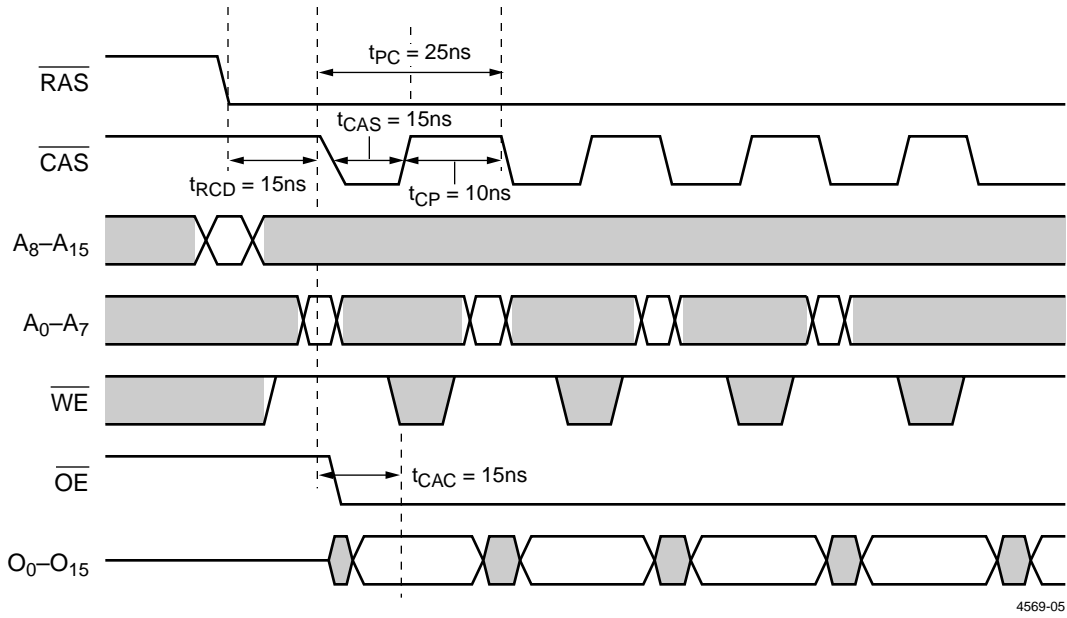


Figure 5. Hyper Page Mode Read Cycle

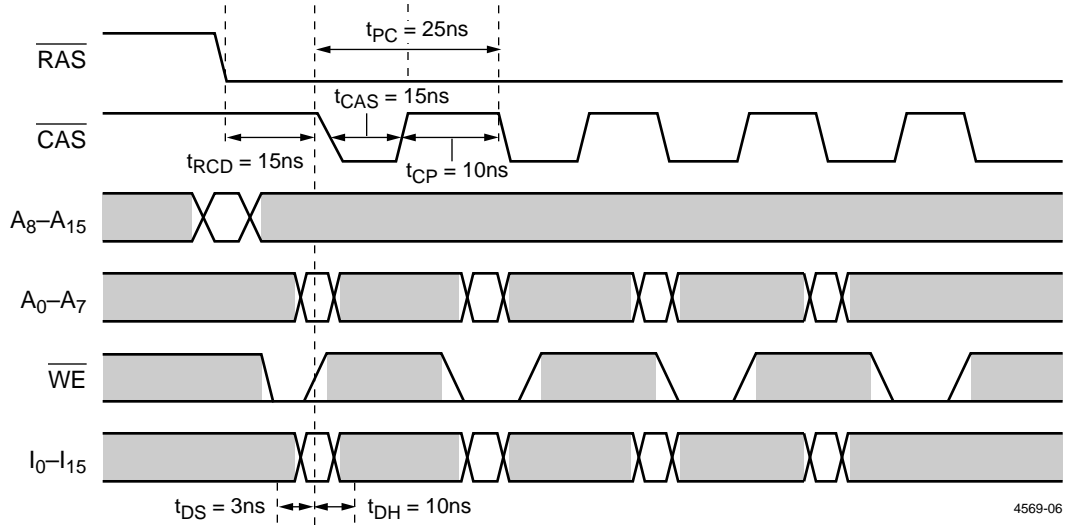


Figure 6. Hyper Page Mode Write Cycle

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