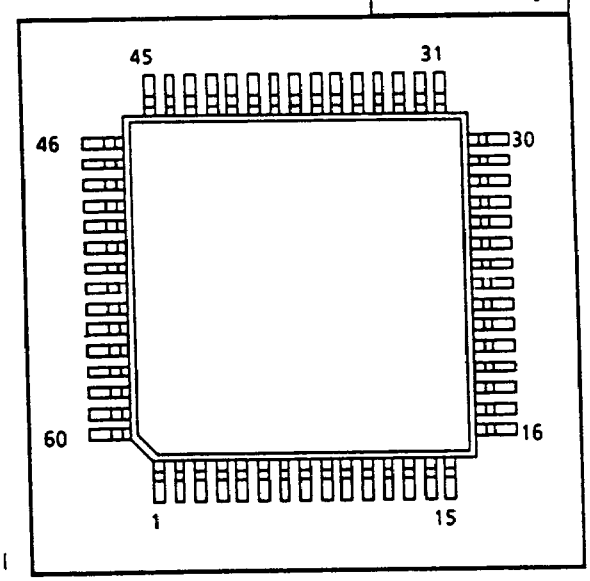
TC35103F

(MODEM Analog Front End)

1. GENERAL DESCRIPTION

Preliminary



The TC35103F is a Modem Analog Front-end LSI designed for use in G3 and G2 Facsimile machines and data modems using with TOSHIBA Modem Processor LSI, TC35108F. The devices compose a 2-wire half-duplex modem and a 4-wire full-duplex modem, which satisfy CCITT Recommendation V.29 (9600bps), V.27ter. (4800bps), V.21 (300bps, chan.2), T3. and T4.

The TC35103F includes receiving and transmission SCF filters, Cable Equalizers, a Group Delay Equalizer, A-D and D-A converters, a digital controlled Programmable Gain Amplifier, a transmission Attenuator, and a transmission Mute switch.

The attenuation ratio, the response of the Cable Equlizers, the Group Delay Equalizer, and the MUTE switch are controlled by the Analog Front End Register (AFER) of the TC35108F through a 8-bit MPU bus.

The products described in this document are strategic products subject to COCOM regulations. They should not be exported without authorization from the appropriate governmental authorities.
TOSHIBA CORPORATION

2. FEATURES

2.1 FEATURES

- ☐ Receiving band-pass filter
- ☐ Transmission low-pass filter
- ☐ Transmission and receiving cable equalizers
  (4 steps characteristic selectable)
- ☐ 1 link fix compromised group delay equalizer
- ☐ Transmission attenuator (Transmission level varies from 0 to −15dBm 1dBm Step)
- ☐ Digital controlled programmable gain amplifier
- ☐ A-D and D-A converters
- ☐ Minimum external parts
- ☐ 2 power supply of +5V and −5V operations
- ☐ CMOS low power consumption 75mW Typ.
- ☐ 60pin flat package

2.2 MODEM STRUCTURE AND FUNCTION

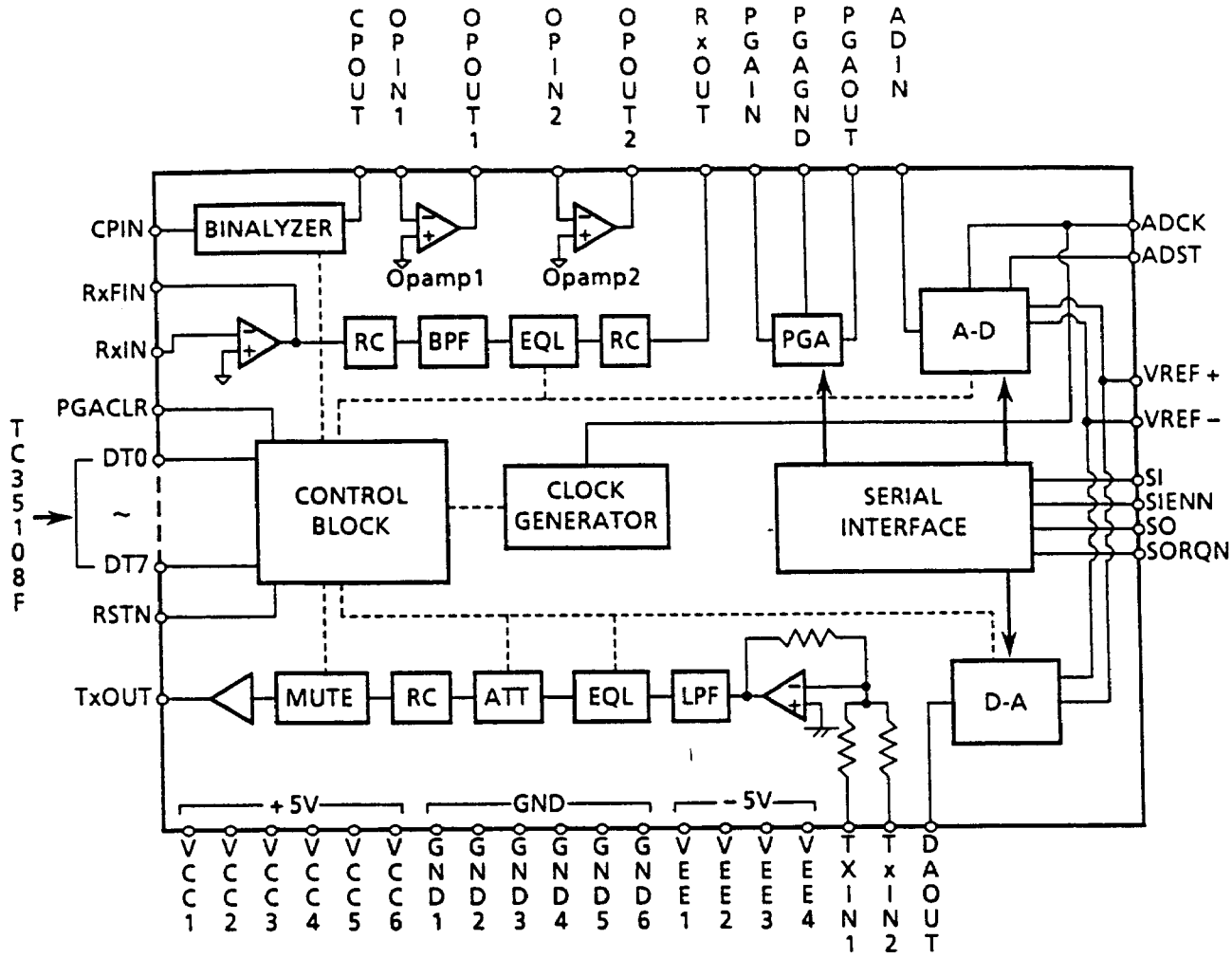
TC35108F, TC35103F

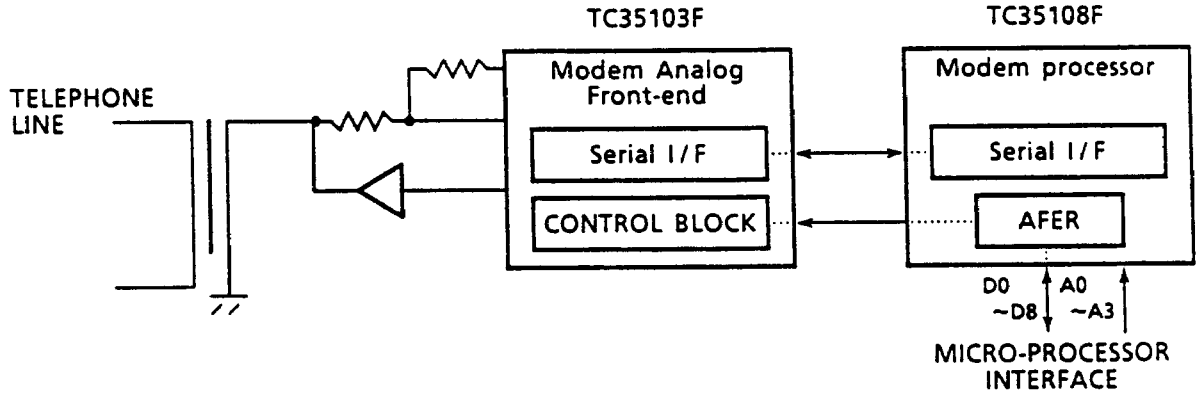
- ☐ Clock frequency 6.2208MHz (±5ppm for G2)
- ☐ G3: CCITT Recommendation
  V.29 (9600 / 7200 / 4800bps)
  V.27ter (4800 / 2400bps)
  V.21 (300bps, CH2 Binary Procedure)
- ☐ G2 : CCITT Recommendation T.3
- ☐ HDLC framing / deframing
- ☐ DTMF dialing
- ☐ Programable tone transmission (Tonal Procedure)
- ☐ Programable tone detection (Tonal Procedure)
- ☐ Equalization
  - Automatic adaptive (TC35108F)
  - Compromised 1 link group dalay
  - Compromised cable
- ☐ V.24 serial Interface (RS-232-D)
- ☐ MPU 8bit parallel Interface

2.3 APPLICATION

- ☐ G3 Facsimile machines
- ☐ Data communication terminals

3. TC35103F BLOCK DIAGRAM





4. PIN DESCRIPTION

PIN NO.	PIN NAME	A/D	I/O	FUNCTION
1	RXOUT	A	O	Receiving filter output.
2	GND1	–	–	ANALOG GROUND
3	RXIN	A	I	Receiving filter input. Vertual short point of pre-amplifier.
4	RXFIN	A	O	Receiving pre-amplifier output.
5	RSTN	D	I	Reset input. Low active, High normal
6	TS1	D	I	Test input. Connect to VCC level.
7	PGACLR	D	I	Make the PGA minimum gain. Low active, High normal
8	TS3	D	I	Test input. Connect to GND level.
9	GND2	–	–	ANALOG GROUND
10	TXIN1	A	I	Transmission filter input 1 for external input.
11	TXIN2	A	I	Transmission filter input 2. Connect to DA converter output (DAOUT). TXIN1 and TXIN2 signal are mixed and flowed out from TXOUT.
12	VCC1	–	–	+5V Power supply
13	TXOUT	A	O	Transmission filter output.
14	VEE1	–	–	−5V Power supply
15	GND3	–	–	ANALOG GROUND
16	SORQN	D	O	Serial output data enable. Connect to TC35108F (-AFIE).
17	SO	D	O	Serial output data. Connect to TC35108F (AFDI)
18	VCC2	–	–	+5V Rower supply
19	VEE2	–	–	−5V Power supply
20	GND4	–	–	ANALOG GROUND
21	ADST	D	I	AD converter start conversion input Connect to TC35108F (SC).
22	VCC3	–	–	+5V Power supply
23	ADCK	D	I	AD converter clock input. Connect to TC35108F (ADCK).
24	TS2	D	I	Test input. Connect to GND level
25	DT0	D	I	ATT0. Att. ratio control input
26	DT1	D	I	ATT1. Att. ratio control input
27	DT2	D	I	ATT2. Att. ratio control input
28	DT3	D	I	ATT3. Att. ratio control input
29	DT4	D	I	CEQL1 Cable equalizer control input

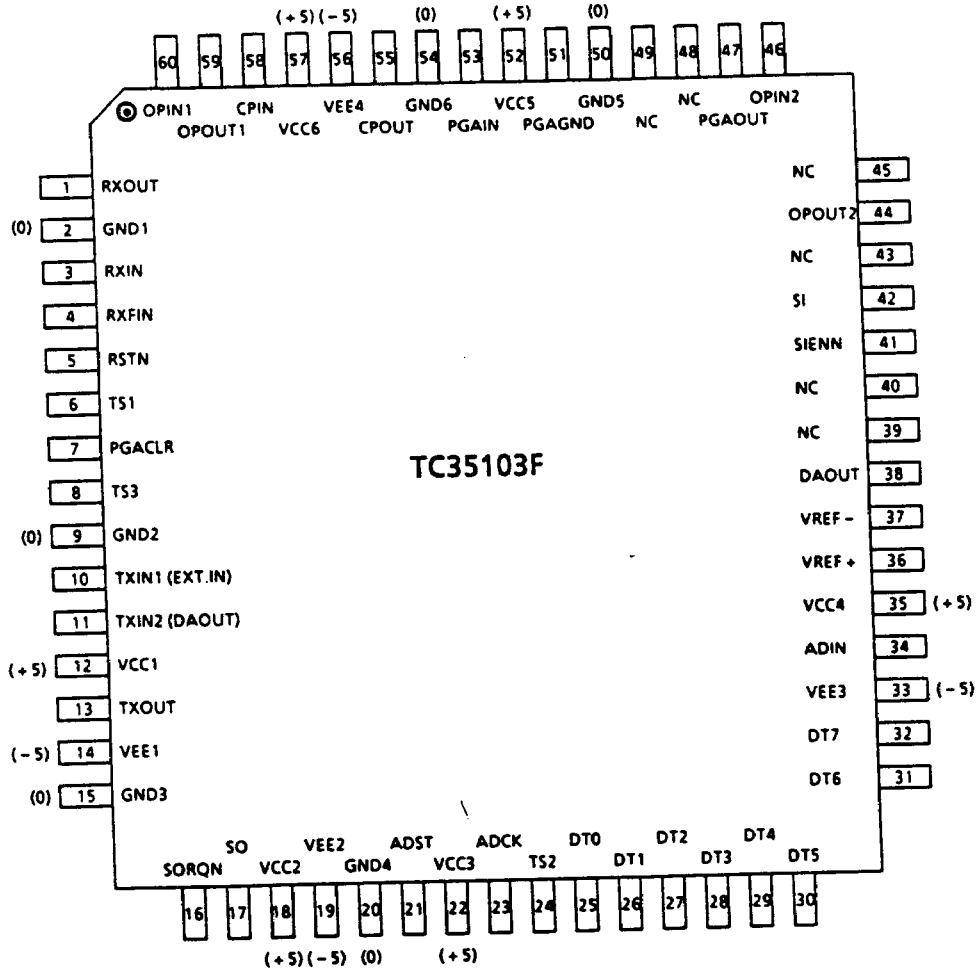
A/D : A = Analog, D = Digital

(Continued)

PIN NO.	PIN NAME	A/D	I/O	FUNCTION
30	DT5	D	I	CEQL2 Cable equalizer control input
31	DT6	D	I	LEQL Delay equalizer control input
32	DT7	D	I	MUTE Transmission mute control input
33	VEE3	–	–	–5V Power supply
34	ADIN	A	I	AD converter analog input. Input voltage range is from VREF+/2 to VREF–/2.
35	VCC4	–	–	+5V Power supply
36	VREF+	A	I	Reference voltage supplying input. Connect to VCC level
37	VREF–	A	I	Reference voltage supplying input. Connect to VEE level
38	DAOUT	A	O	DA converter analog output
39	NC	–	–	No-connect terminal. Leave it open
40	NC	–	–	No-connect terminal.. Leave it open
41	SIENN	D	I	Serial input data enable. Connect to TC35108F (-AFOE)
42	SI	D	I	Serial input data. Connect to TC35108F (AFDO)
43	NC	–	–	No-connect terminal. Leave it open
44	OPOUT2	A	O	OPAMP. 2 output
45	NC	–	–	No-connect terminal. Leave it open
46	OPIN2	A	I	OPAMP. 2 input. Vertual short point
47	PGAOUT	A	O	Programmable gain amp. output
48	NC	–	–	No-connect terminal. Leave it open
49	NC	–	–	No-connect terminal. Leave it open
50	GND5	–	–	ANALOG GROUND
51	PGAGND	A	I	PGA ground input. Connect to 0.1uF capacitor
52	VCC5	–	–	+5V Power supply
53	PAGIN	A	I	Programmable gain amp. input
54	GND6	–	–	ANALOG GROUND
55	CPOUT	D	O	Binalyzed comparator digital data output
56	VEE4	–	–	–5V Power supply
57	VCC6	–	–	+5V Power supply
58	CPIN	A	I	Binalyzing comparator Analog input
59	OPOUT1	A	O	OPAMP. 1 output
60	OPIN1	A	I	OPAMP. 1 input

A/D : A = Analog, D = Digital

4.1 PIN ASSIGNMENT



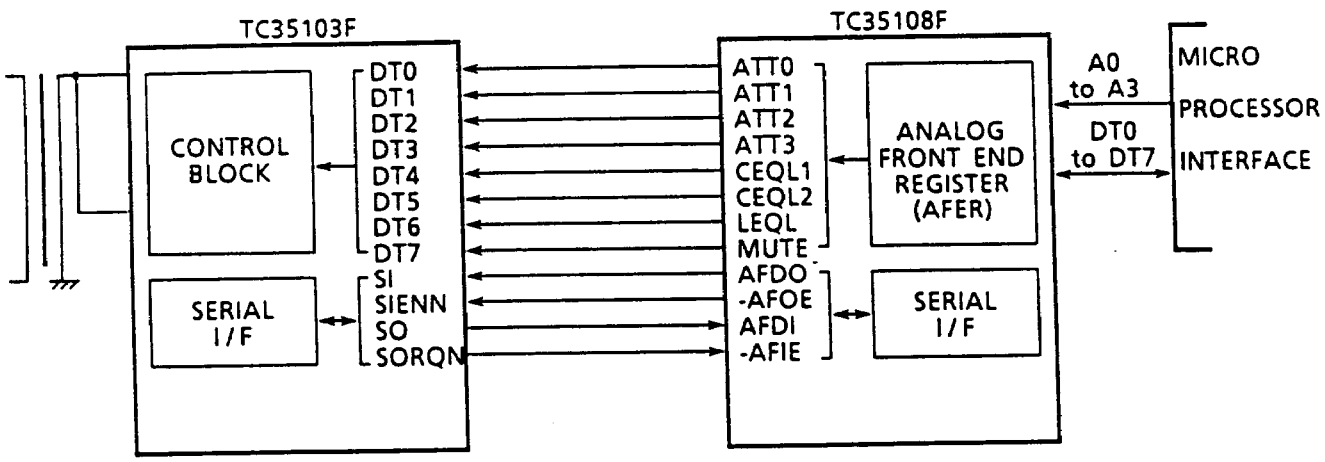
[TOP VIEW]

5. MODE SELECTION

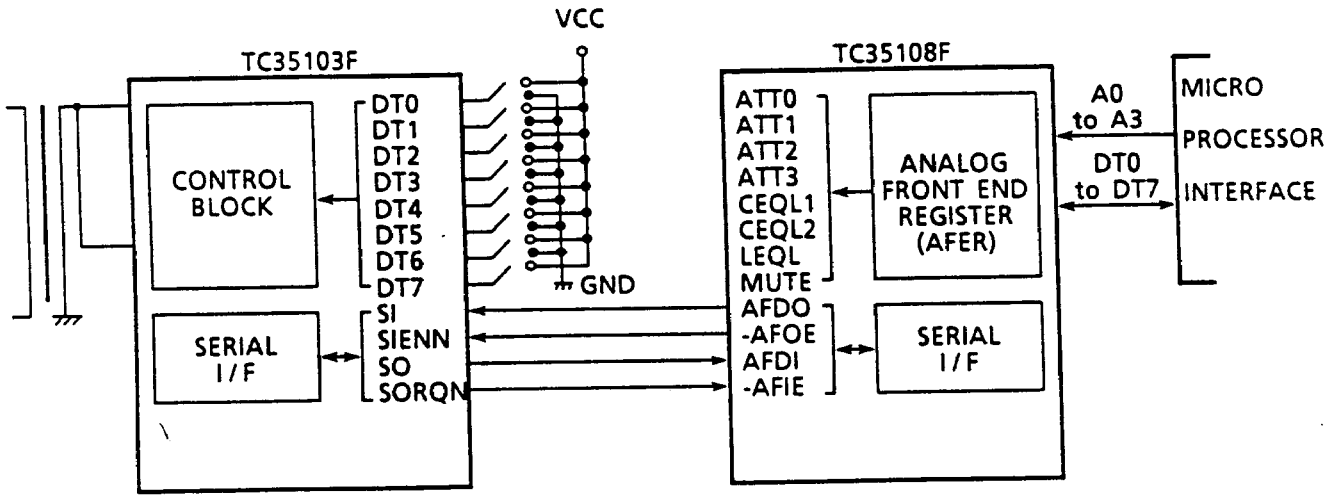
Control terminals from DT0 to DT7 allow to change the characteristic of a transmission Attenuation Ratio (Transmission level varies from 0 dBm to −15dBm 1dBm step) and a Mute Switch, transmission and receiving Cable Equalizers (4 response), and a receiving Group Delay Equalizer.

5.1 SYSTEM DIAGRAM

(1) CPU CONTROL



(2) SWITCH CONTROL



5.2 TRANSMISSION ATTENUATION RATIO

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

(MSB) DT3 (ATT3)	DT2 (ATT2)	DT1 (ATT1)	(LSB) DT0 (ATT0)	TRANSMISSION LEVEL
0	0	0	0	0dBm
0	0	0	1	−1dBm
0	0	1	0	−2dBm
0	1	0	0	−4dBm
1	0	0	0	−8dBm
1	1	1	1	−15dBm

The attenuation ratio shall be set to control the transmission level from 0dBm to −15dBm by 1dBm step using the DT0 to DT3 which is weighed in binary.

5.3 TRANSMISSION AND RECEIVING COMPROMISED CABLE EQUALIZER (FOR THE NON-LOADED CABLE)

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

(MSB) DT5 (CEQL2)	(LSB) DT4 (CEQL1)	RESPONCE
0	0	CABLE1
0	1	CABLE2
1	0	CABLE3
1	1	CABLE4

4 selectable cable equalizing characteristics are decided by the DT4 and DT5.

The filters equalize the non-loaded telephone cable distorsion whose response is high frequency signal is redused than lower frequency's. It depends upon where the Facsimile is located.

A suggested cable equalizer sellection according to a distance between a Exchange and a Facsimile machine is listed below.

Radius (mm)	Cable eql.	DT4	DT5	Distance (km)
0.4	CABLE1	0	0	0
	CABLE2	0	1	1.8
	CABLE3	1	0	3.6
	CABLE4	1	1	5.6
0.5	CABLE1	0	0	0
	CABLE2	0	1	2.3
	CABLE3	1	0	4.6
	CABLE4	1	1	6.9

5.4 RECEIVING GROUP DELAY EQUALIZER

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

DT6 (LEQL)	RESPONCE
0	NO EQUALIZER
1	JAPAN 1LINK COMPROMISED EQUALIZER

The TC35103F has a group delay equaling responce in receiving filter which is set using DT6 (LEQL).

We recommend to use NO-EQUALIZER mode (DT6=0) in G3 communication and 1link EQUALIZER in G2 mode.

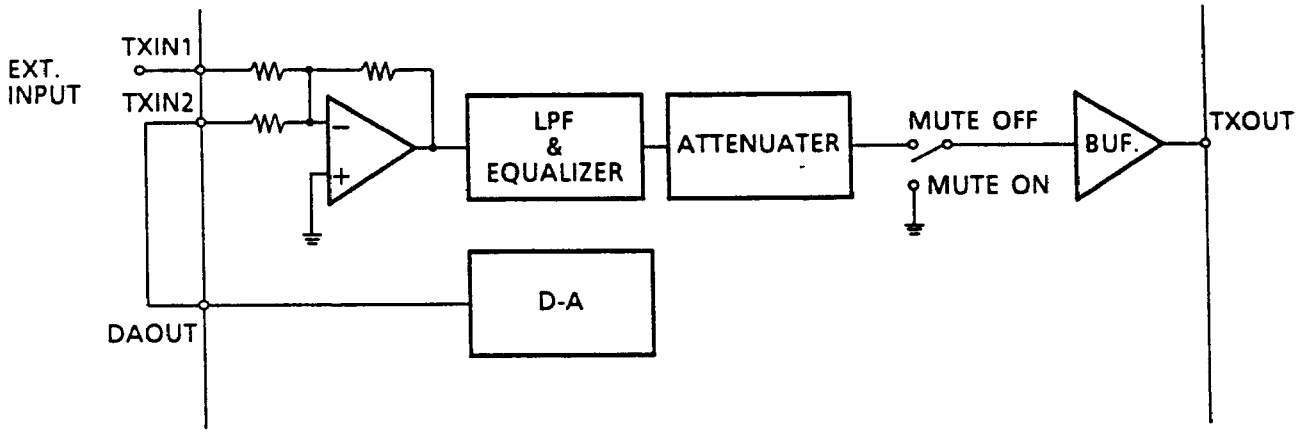
5.5 TRANSMISSION MUTE SWITCH

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

DT7 (MUTE)	MUTE FUNCTION
0	MUTE OFF (Transmission enable)
1	MUTE ON (Transmission disale)

A built-in MUTE SWITCH is placed just before TXOUT terminal in order to prevent noise in the transmission side from flowing to the receiving side and interfaring with the receiving signal, and make the bit error rate better.

The MUTE SWITCH is controlled using DT7 (MUTE).



TRANSMISSION SIDE

6. ELECTRICAL CHARACTERISTICS (Preliminary)

6.1 MAXIMUM RATINGS

Item	Symbol	RATING		UNIT
		MIN.	MAX.	
Supply Voltage	VCC	−0.5	7.0	V
Supply Voltage	VEE	−0.7	0.5	V
Analog Input Voltage	VIN	VEE−0.5	VCC+0.5	V
Digital Input Voltage	VIN	−0.5	VCC+0.5	V
Analog Output Voltage	VOUT	VEE−0.5	VCC+0.5	V
Digital Output Voltage	VOUT	−0.5	VCC+0.5	V
Input Current	IIN	−20	20	mA
Operation Temparature	Tope	−10	70	°C
Strage Temparature	Tstg	−55	150	°C
Power Dissipation	PD		600	mW
Lead Temparature / time	Tsol	260°C · 10sec		

GND = 0V

6.2 DC CHARACTERISTICS

(Ta = −10~70°C VSS = AGND = 0V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Voltage	VCC		4.5	5.0	5.5	V
Operation Voltage	VEE		−5.5	−5.0	−4.5	V
Operation Current	ICC			12	30	mA
Operation Current	IEE			−12	−30	mA
H level output current	IOH	TERMINAL−1, Ta = 25°C	0.1			mA
L level output current	IOL	TERMINAL−1, Ta = 25°C	0.4			mA
H level input current	IIH	Except PGAIN, CPIN, Ta = 25°C	−10		10	μA
		PGAIN, CPIN, Ta = 25°C	25		120	μA
L level input current	IIL	Except PGAIN, CPIN, Ta = 25°C	−10		10	μA
		PGAIN, CPIN, Ta = 25°C	−120		−25	μA

TERMINAL−1 ; CPOUT, SO, SORQN

6.3 RECEIVING FILTER

Item	CONDITION		MIN.	TYP.	MAX.	UNIT
GAIN CHAR.	VDD = 4.5V VEE = −4.5V Rxout Rxin = 0dBm	fin = 80Hz		−33	−30	dB
		fin = 300Hz		−2.5	−2	dB
		fin = 1000Hz	−0.3	0	0.7	dB
		fin = 3200Hz	−0.7	0	0.7	dB
		fin = 5000Hz		−25	−22	dB
		fin = 8000Hz		−60	−57	dB
GROUP DELAY DIST. DIFF.	VDD = 4.5, VEE = −4.5V Rxin = 0dBm, Rxout, NO EQUALIZING(DT6 = 0)	fin = 800~3000Hz DIFF.		120		μs
	VDD = 4.5V, VEE = −4.5V Rxin = 0dBm, Rxout, JAPAN 1LINK COMP. EQUALIZING (DT6 = 1)	600 − 2000Hz DIFF.	166	266	366	μs
		3200 − 2000Hz DIFF.	368	468	568	μs
INPUT LEVEL	VDD = 4.5V, VEE = −4.5V, Rxin, Opin1, OPin2		−48		6	dBm
OFFSET VOLTAGE	VDD = 5.5V, VEE = −5.5V, Rxout, Opout1, 2		−200		+200	mV
DISTORTION	VDD = 4.5V, VEE = −4.5V RL = 30KΩ, CL = 80PF fin = 1000Hz	Rxout (10dBm)		−47	−35	dB
		Opout1, 2 (0dBm)		−85	−55	dB
OUTPUT IMPEDANCE	VDD = 4.5V, VEE = −4.5V fin = 1000Hz, RL = 10KΩ	Rxout			600	Ω
		Rxfin, Opout1, 2			150	Ω

6.4 TRANSMISSION FILTER

ITEM	CONDITION					MIN.	TYP.	MAX.	UNIT
GAIN CHAR.	AT3, AT2, AT1, AT0 = 0, 0, 0, 0, VDD = 4.5V, VEE = −4.5V, Txout, Txin = 0dBm	fin = 300Hz				3.8	4.3	4.8	dB
		fin = 1000Hz				3.8	4.3	4.8	dB
		fin = 3200Hz				3.5	4.3	4.9	dB
		fin = 5000Hz					−29	−24	dB
		fin = 7000Hz					−64	−54	dB
		fin = 9000Hz					−64	−54	dB
		fin = 20000Hz					−60	−50	dB
GROUP DELAY DIST.	VDD = 4.5, VEE = −4.5V, Txin = 0dBm, Txout	fin = 300~3000Hz					70		μs
INPUT LEVEL	VDD = 4.5V, VEE = −4.5V, TXin							6	dBm
OFFSET VOLTAGE	VDD = 5.5V, VEE = −5.5V, TXout					−300		300	mV
DISTORTION	VDD = 4.5V, VEE = −4.5VMAX GAIN, TXout, fin = 1000Hz, 0dBm						−47	−40	dB
ATT. RATIO	VDD = 4.5V, VEE = −4.5V TXout, 1dB step	ATT3	ATT2	ATT1	ATT0				
		0	0	0	0	3.8	4.3	4.8	dB
		0	0	0	1	2.8	3.3	3.8	dB
		0	0	1	0	1.8	2.3	2.8	dB
		0	1	0	0	−0.2	0.3	0.8	dB
		1	0	0	0	−4.2	−3.7	−3.2	dB
		1	1	1	1	−11.2	−10.7	−10.2	dB
ATT. STEP	VDD = 4.5V, VEE = −4.5V, Txout, fin = 1000Hz					−0.75	1.0	1.25	dB
OUTPUT IMPEDANCE	VDD = 4.5V, VEE = −4.5V, fin = 1KHz, RL = 10KΩ, Txout							600	Ω

6.5 AGC (Programable Gain Amp.)

ITEM	CONDITION						GAIN			UNIT
	PGA5	PGA4	PGA3	PGA2	PGA1	PGA0	MIN.	TYP.	MAX.	
GAIN CHAR. VDD = 4.5V VEE = −4.5V 0.75dB STEP Gain = −7.8 +0.75×I (I = 0, 1, ···, 63) GAIN DIFF ±0.30	0	0	0	0	0	0	−8.05	−7.8	−7.55	dB
	0	0	0	0	0	1	−7.3	−7.05	−6.8	dB
	0	0	0	0	1	0	−6.55	−6.3	−6.05	dB
	0	0	0	1	0	0	−5.05	−4.8	−4.55	dB
	0	0	1	0	0	0	−2.05	−1.8	−1.55	dB
	0	1	0	0	0	0	3.95	4.2	4.45	dB
	1	0	0	0	0	0	15.95	16.2	16.45	dB
	1	1	1	1	1	1	39.2	39.45	39.7	dB
STEP DIFF.							0.5	0.75	1.0	dB

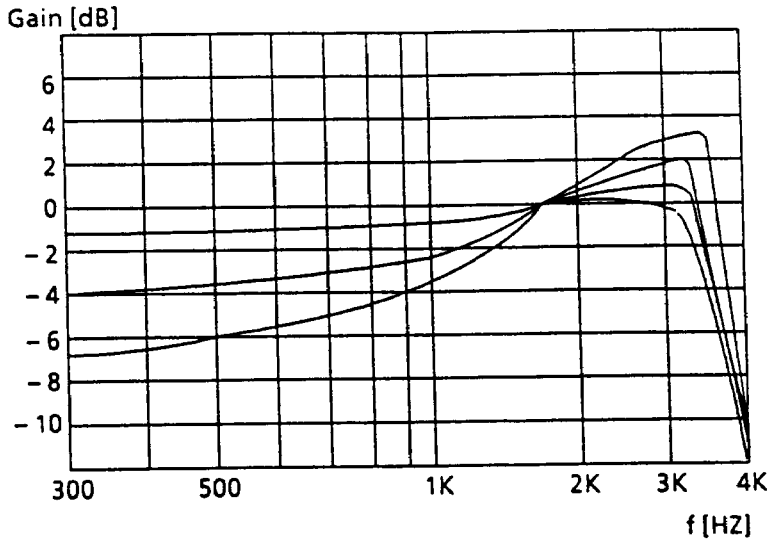
6.6 A-D CONVERTER

ITEM	CONDITION	MIN.	TYP.	MAX.	UNIT
RESOLUTION			8		bit
CONVERSION RANGE	VDD = 5.0V VRef+ = 5.0V AD7~AD0 = 00 (H) VRef− = −5.0V AD7~AD0 = FF (H) $1LSB = \frac{VFF - V00}{255}$		−2.5 +2.5		V

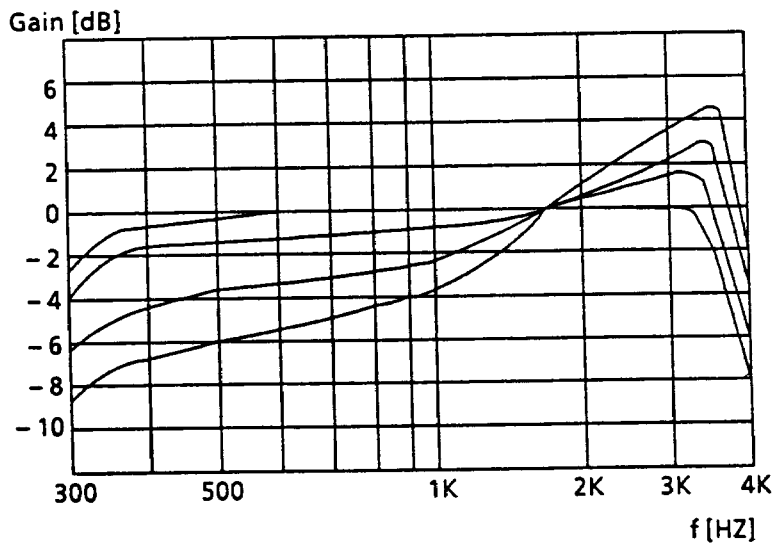
6.7 D-A CONVERTER

ITEM	CONDITION	MIN.	TYP.	MAX.	UNIT
RESOLUTION			8		bit
CONVERSION RANGE	VDD = 5.0V VRef+ = 5.0V AD7~DA0 = 00 (H) VRef− = −5.0V AD7~DA0 = FF (H) $1LSB = \frac{VFF - V00}{255}$		−2.5 +2.5		V

6.8 CABLE EQUALIZER RESPONSE



Typical transmission cable equalizer response

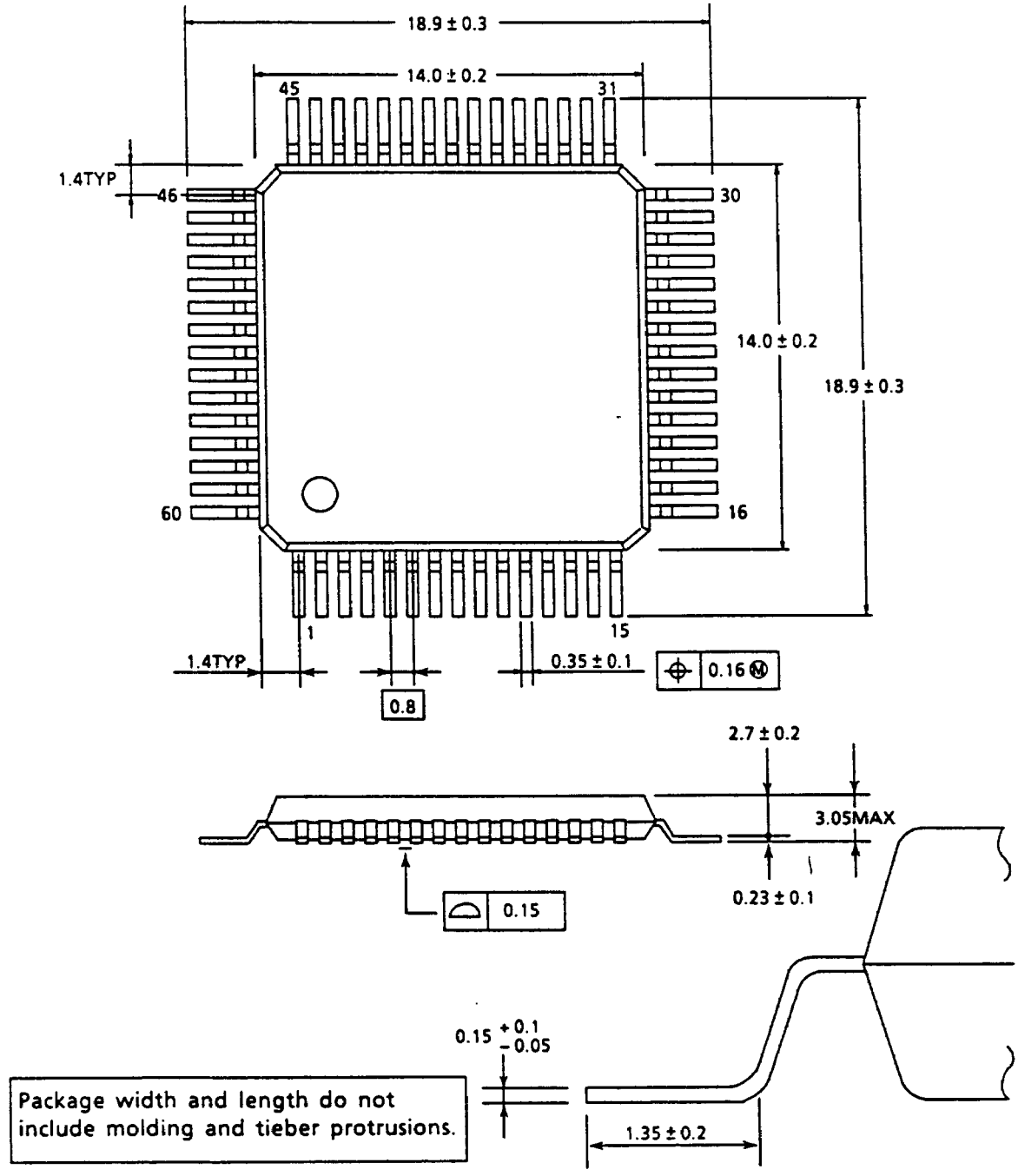


Typical receiving cable equalizer response

7. LSI LAYOUT

QFP60-P-1414D

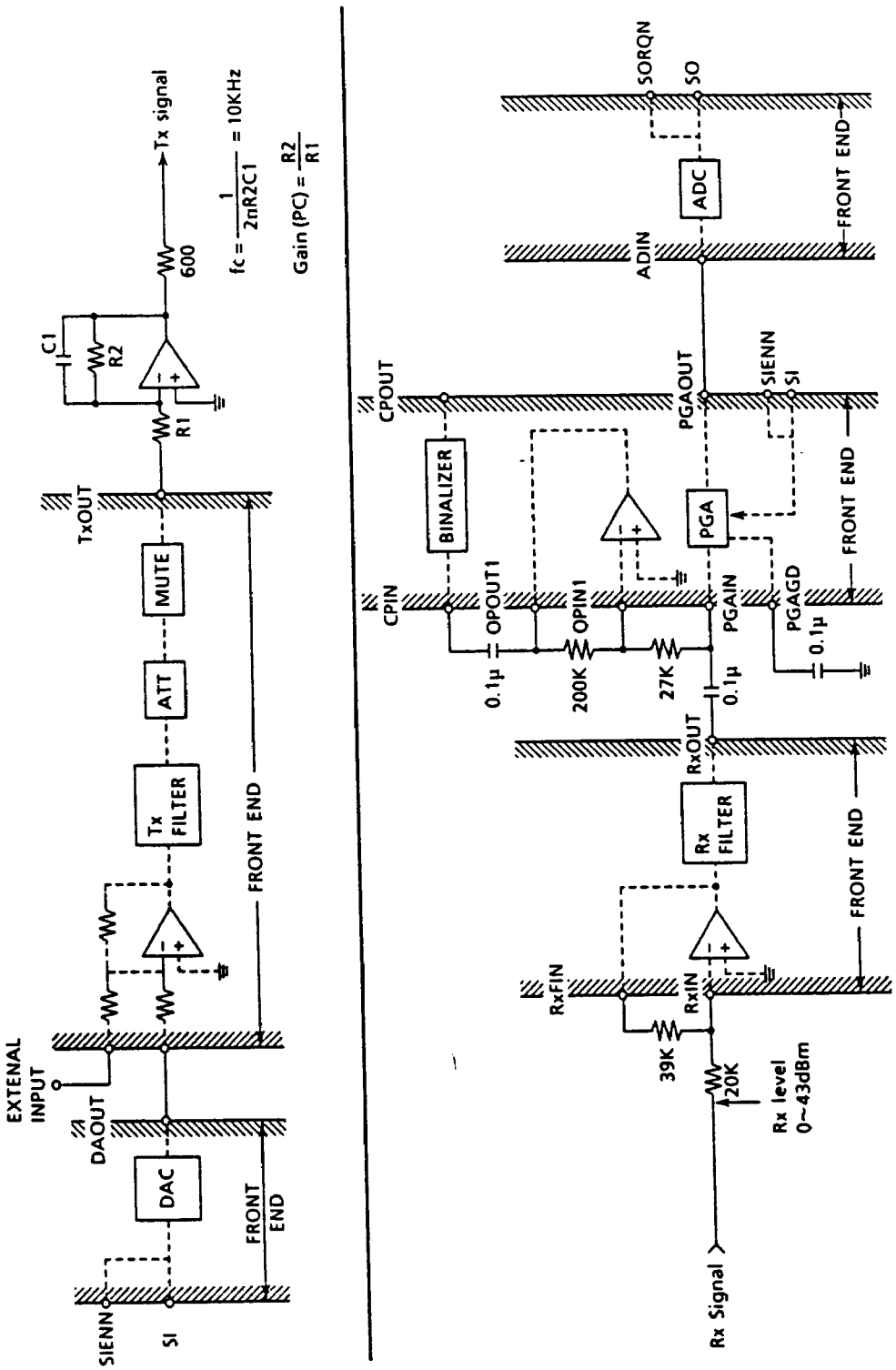
単位 : mm



Package width and length do not include molding and tieber protrusions.

8. APPLICATION

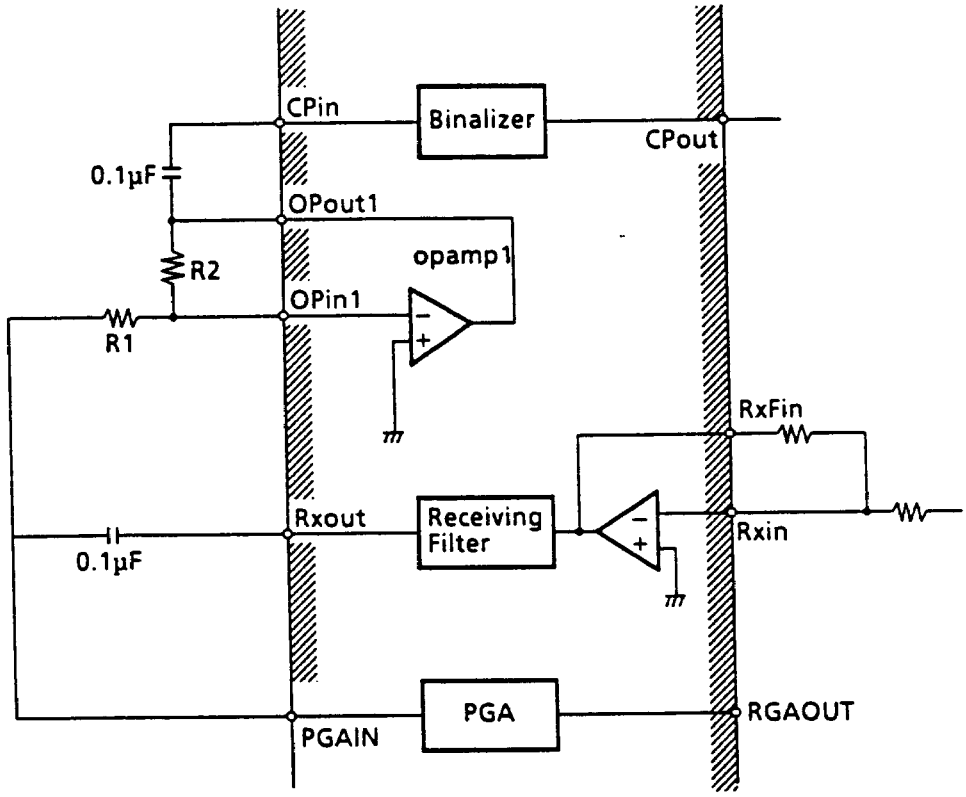
8.1 EXTERNAL PARTS



8.2 Setting of binarised detection level

The TC35103F converts inputed tone signal from CPin above −20.8±2dBm in range of ±5.0±10% supply voltage to TTL level. Binarized detection level of tone signal is determined by R1 and R2 which is added to binarized circuit and opamp1.

(ex) detection level above −43dBm (supply voltage ±5.0±10%V)
43dBm*18.8dBm=24.2dB
R2/R1=17.7(25dB)
R1027kohm (select R1≧15kohm)
R2=480kohm



EJC-TC35103F-18
10-SEP.-1989
TOSHIBA CORPORATIO

8.3 APPLICATION CIRCUIT