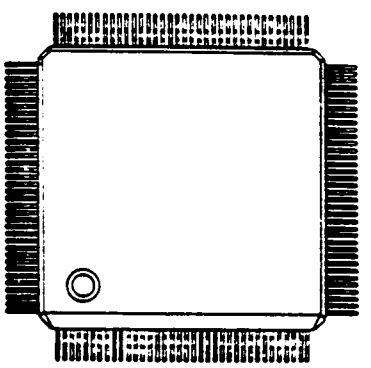
TC35107F
CMOS INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC35107F

9600BPS MODEM

The TOSHIBA TC35107F is a modem LSI designed for use in Group 3 facsimile machines. The modem is capable of operating over the public switched telephone network through the net work control unit (NCU). The modem satisfies CCITT Recommendations V.29, V.27ter, V.21, T.30 and T.3. The TC35107F can transfer data at 9600, 7200, 4800, 2400, and 300bps. This modem processor emploies advanced digital signal processing techniques.

The TC35107F allows DTMF generation and tone detection. Operation and status monitoring is performed via bus interface. This modem processor supports V.24 compatible serial interface and microprocessor bus interface for data transferring.



FP 144 pin

FEATURES

- o G III CCITT Recommendation
  - V.29, V.27ter
- o G II CCITT Recommendation
  NTT mini-fax mode
- o G I NTT VF mode
  FSK mode (transmission only)
- o T.30
  - V.21 (ch2) for Binary Procedure
  - Tone Generation for Tonal Procedure
- o DTMF Generation for Dialing
- o Generation and Detection for various tones
- o DTE Interface (parallel/serial)
  - Microprocessor bus
  - RS-232-C (CCITT V.24 Compatible)
- o CMOS Low Power
- o +5V Single Power Supply

APPLICATIONS

- o Group III Facsimile
- o Data Communication Equipment

The products described in this document are strategic products subject to COCOM regulations. They should not be exported without authorization from the appropriate governental authorities.

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SEPT-1st-1988
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1 ABSTRUCT

1. 1 INTRODUCTION

The TC35107F is a modem processor suitable for use in Group III facsimile machines. This modem processor can operate speed at 9600, 7200, 4800, 2400 and 300bps for digital data transferring and supports Group II and Group I transmission/reception mode.

BY means of externally connecting the analog front-end LSI TC35102F (under development) the Half-Duplex modem required for the facsimile can easily be realized.

TC35107F allows DTMF generation suitable not only for dialing but also user's applications and tone detection for T.30 Tonal Procedure.

Setting various configuration, monitoring its status and parallel transmission/reception data transfer are performed via microprocessor bus. The modem processor provides two address terminals, Read/Write control and 8-bit bus for microprocessor interface.

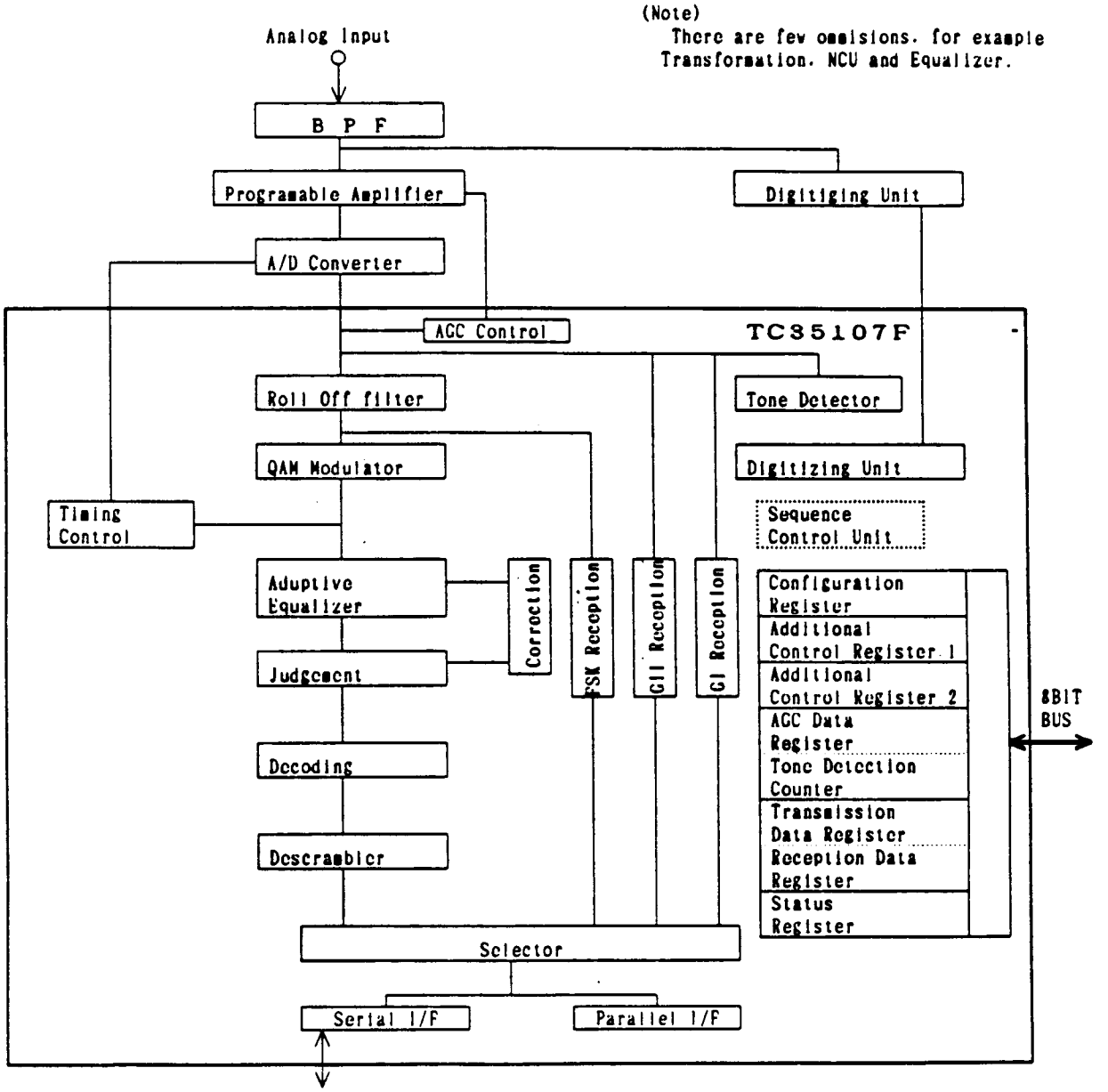
The CB (Control Bit assigned to bit-6 of additional control register 1.) defines the most significant configuration that modem signal processing and other functions such as DTMF,tone detection. CB must be written during the term of hardware reset. After the reset sequence, configuration register defines its operation.

Data transfer mode is defined by the HPLS bit of the additional data register 2. This bit means the selection of the serial interface or the parallel interface with DTE side.

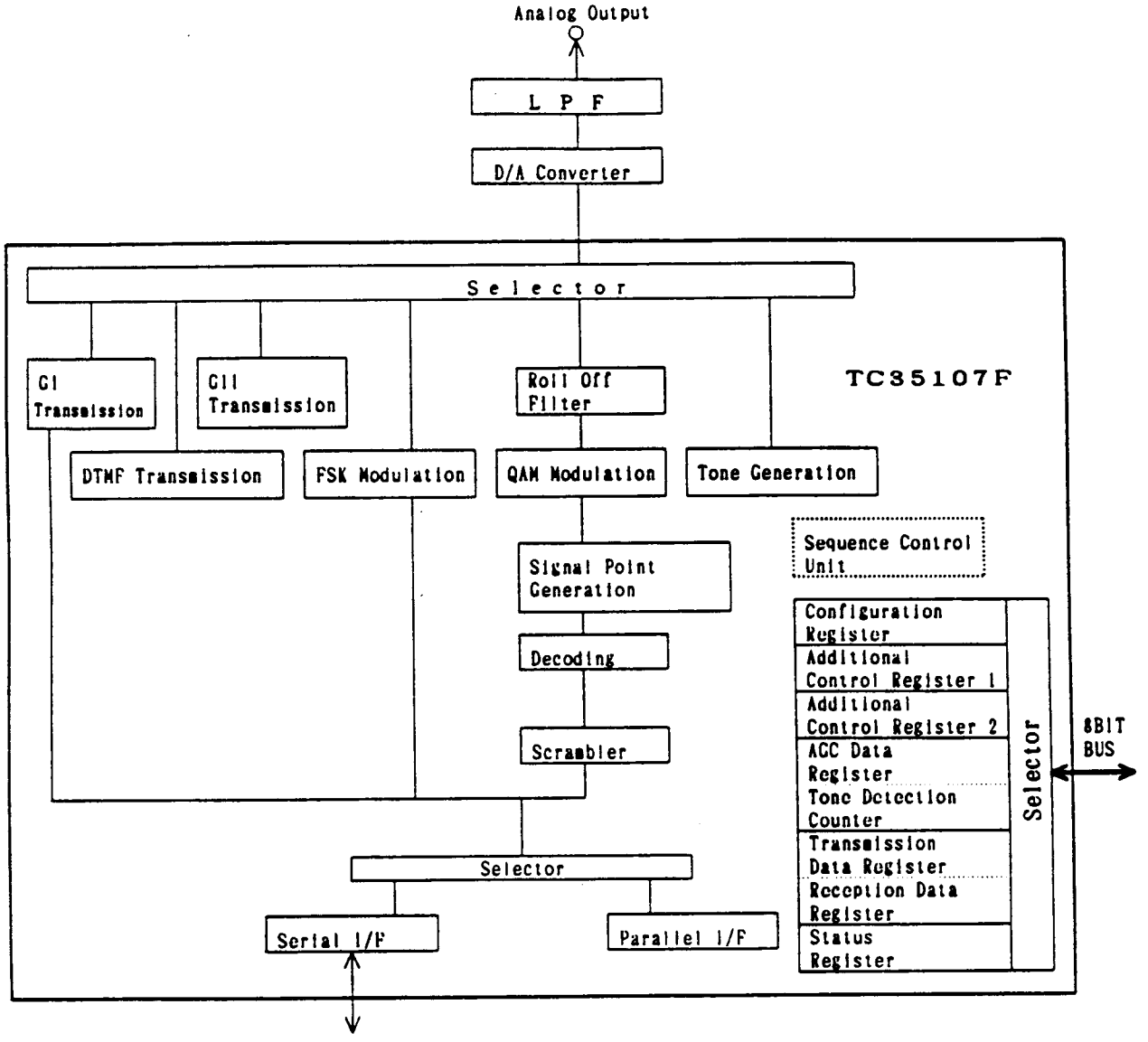
For DTMF generation and tone detection, the TC35107F allows coefficients rewriting as alternative coefficients provided in modem processor. Coefficients writing contributes more flexible usage for users.

1. 2 FUNCTIONAL BLOCK DIAGRAM

(1) RECEIVER PART



(2) TRANSMITTER PART



1. 3 CONFIGURATION TABLE

Group III	Bit Rate		ECHO PROTECTION	CODE (HEX)
V.27ter	4800	LONG	NO	C0
			YES	C1
		SHORT	NO	C2
			YES	C3
	2400	LONG	NO	C4
			YES	C5
		SHORT	NO	C6
			YES	C7
V.29	9600		NO	C8
			YES	C9
	7200		NO	CA
			YES	CB
	4800		NO	CC
			YES	CD

Group II	PHASE CONTROL (PHS)	CODE (HEX)
	NO	D0
	YES	D1

Group I			CODE (HEX)
AM	NTT VF Mode		E0
FSK	USA SPEC. TxD	0: 2400Hz 1: 1500Hz	E4
	CCITT SPEC. TxD	0: 2100Hz 1: 1300Hz	E6

V.21	TxD	0: 1850Hz 1: 1650Hz	E8

	FREQUENCY	CODE (HEX)
Tone Generation	462 Hz	F0
	540Hz	F1
	1080Hz	F2
	1100Hz	F3
	1250Hz	F4
	1300Hz	F5
	1500Hz	F6
	1650Hz	F7
	1700Hz	F8
	1800Hz	F9
	1850Hz	FA
	1900Hz	FB
	2100Hz	FC
	2400Hz	FD
	3240Hz	FE
	1600Hz	FF

OTHER FUNCTIONS
- Parallel or Serial (V.24 interface) data transfer - Interrupt signal 'INT' generation in parallel mode - Output AGC gain to Microprocessor bus - Frequency detection using binary counter

2 HARDWARE CONSTRUCTION

2. 1 TERMINALS AND THEIR FUNCTIONS

PIN NAME	PIN No.	I/O	FUNCTION
AQ0 (LSB) AQ1 AQ2 AQ3 AQ4 AQ5 AQ6 AQ7 (MSB)	137 136 134 133 132 131 130 129	O	Transmission signal digital output. Connect to D/A Converter.
ACLK TXCK	128 62	I O	Transmission synchronous clock input Transmission synchronous clock output — Connect
$\overline{APDO}$ $\overline{APDI}$ $\overline{BPDO}$ $\overline{BPDI}$	4 5 106 105	I/O	Connect to Modem processor control terminal $\overline{PDO1}$. " $\overline{PDI1}$. " $\overline{PDO2}$. " $\overline{PDI2}$.
$\overline{PDO1}$ $\overline{PDI1}$ $\overline{PDO2}$ $\overline{PDI2}$	63 64 67 68	O	Modem processor control terminal
CLK	17	I	System clock input fin=6.2208 MHz
$\overline{SIEN}$ SI SICK	20 21 89	I I I	Serial input enable (LOW active) Serial data input Serial input clock Serial data is input at the rising edge of serial input clock.
$\overline{BSORQ}$ BSO BSOCK	87 88 114	O O I	Serial output request (Open DRAIN terminal) Serial data output (for EYE-PATTERN monitor) Serial output clock
DB0 (LSB) DB1 DB2 DB3 DB4 DB5 DB6 DB7 (MSB)	34 33 30 29 28 27 26 25	I/O	Microprocessor bus interface

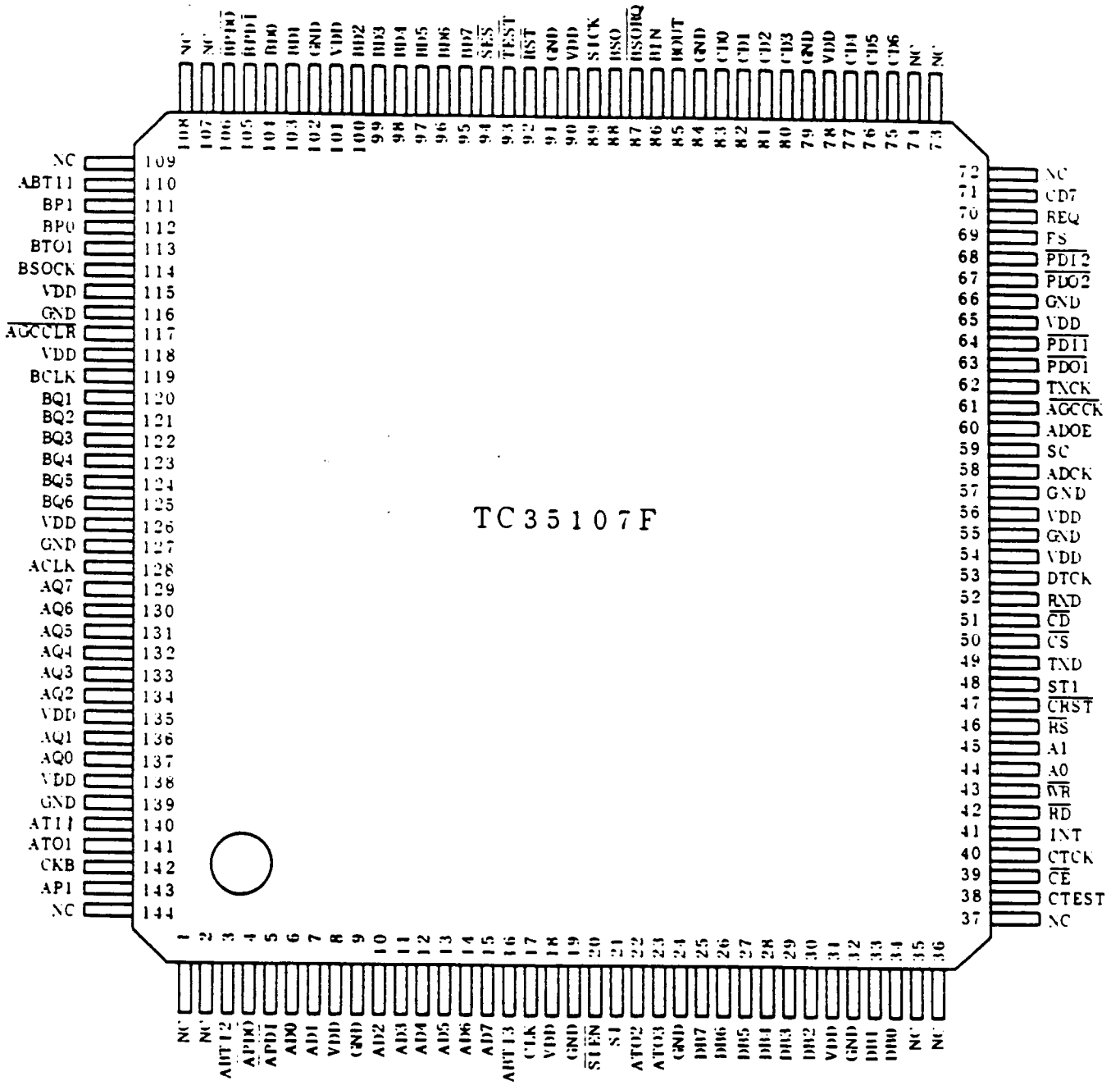
PIN NAME	PIN No.	I/O	FUNCTION
$\overline{CE}$	39	I	Chip Enable
A0	44	I	Address bit 0
A1	45	I	Address bit 1
$\overline{WR}$	43	I	Write enable
$\overline{RD}$	42	I	Read enable
$\overline{RST}$	92	I	Reset input (LOW active). Connect to CRST.
$\overline{CRST}$	47	I	Reset input (LOW active). Connect to RST.
$\overline{SES}$	94	I	Control input
FS	69	O	Control output — Connect.
REQ	70	I	Control input
AP1	143	O	Control output — Connect.
AD0 (LSB)	6	I/O	Modem processor internal bus A
AD1	7		
AD2	10		
AD3	11		
AD4	12		
AD5	13		
AD6	14		
AD7 (MSB)	15		
BD0 (LSB)	104	I/O	Modem processor internal bus B
BD1	103		
BD2	100		
BD3	99		
BD4	98		
BD5	97		
BD6	96		
BD7 (MSB)	95		
CD0 (LSB)	83	I/O	Modem processor internal bus C Internal bus A,B and C should respectively be connected outside of the TC35107F.
CD1	82		
CD2	81		
CD3	80		
CD4	77		
CD5	76		
CD6	75		
CD7 (MSB)	71		

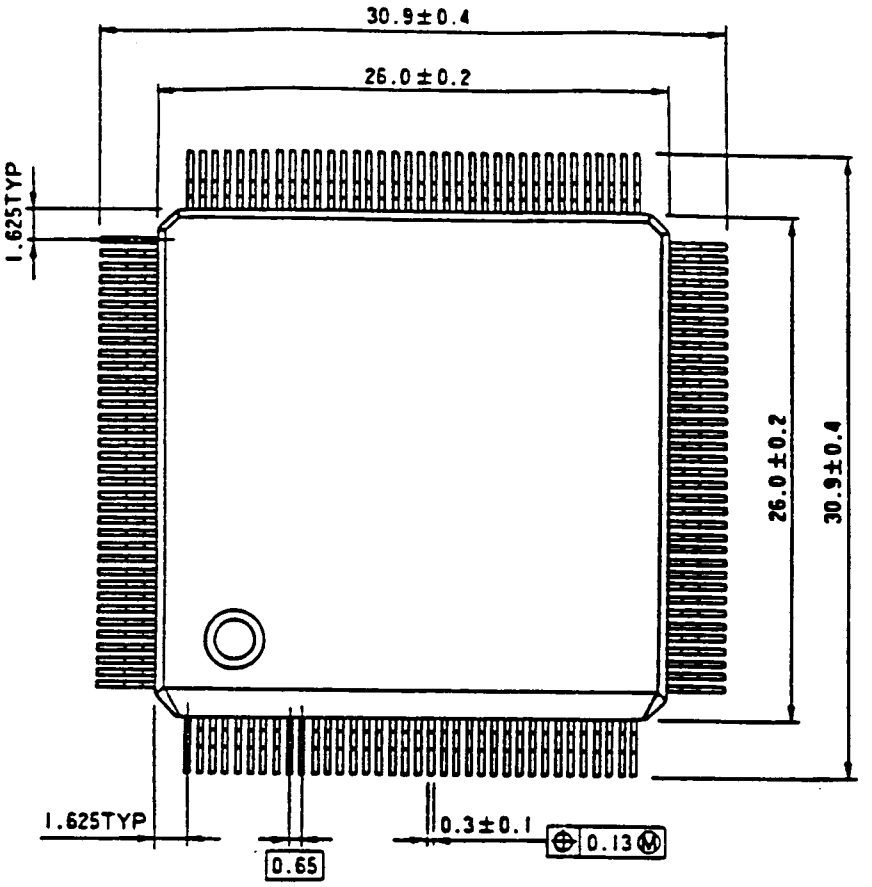
PIN NAME	PIN No.	I/O	FUNCTION
BQ1 (LSB) BQ2 BQ3 BQ4 BQ5 BQ6 (MSB)	120 121 122 123 124 125	O	AGC gain output terminals. Connect to the programmable amplifier.
BCKL AGCCK	119 61	I O	AGC synchronous clock input AGC synchronous clock output Connect.
AGCCLR	117	I	AGC gain reset input. (LOW active)
BIN BOUT	86 85	I O	Control input Control output Connect.
CKB DTCK RXD TXD	142 53 52 49	O O O I	Baud rate clock output Data clock output (for both transmission and reception) Reception data serial output. Output synchronize to the DTCK falling edge. Transmission data serial input. Input data synchronizing to DTCK rising.
CD RS CS	51 46 50	O I O	Carrier detection output (LOW active) Request to send input (LOW active) Clear to send output (LOW active)
ST1	48	I	External transmission timing clock input
ADCK SC ADOE	58 59 60	O O O	Clock output for A/D conversion A/D start conversion A/D output enable (High active)
CTCK	40	I	Frequency detect counter input Connect to the binary digitizing circuit output.
INT	41	O	Interrupt request output (See parallel mode timing chart.)
ABTI1 ABTI2 ABTI3 ATI1 CTEST TEST	110 3 16 140 38 93	I I I I I I	Clamp to VDD. " GND. " GND. " GND. " GND. " VDD.

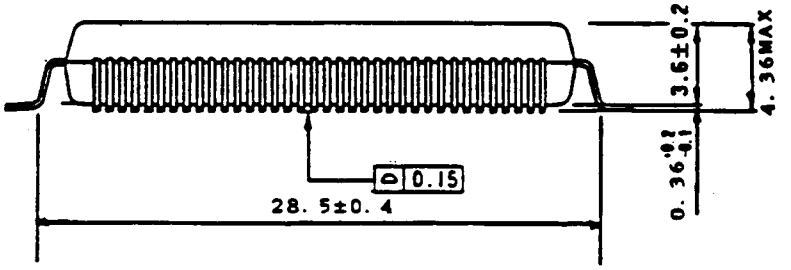
PIN NAME	PIN No.	I/O	FUNCTION
ATO1 ATO2 ATO3 BTO1 BP0 BP1	141 22 23 113 112 111	O O O O O O	Test output terminals (Not in use).
VDD	8 18 31 54 56 65 78 90 101 115 118 126 135 138		+5V Power supply terminal.
GND	9 19 24 32 55 57 66 79 84 91 102 116 127 139		Ground terminal (0V)

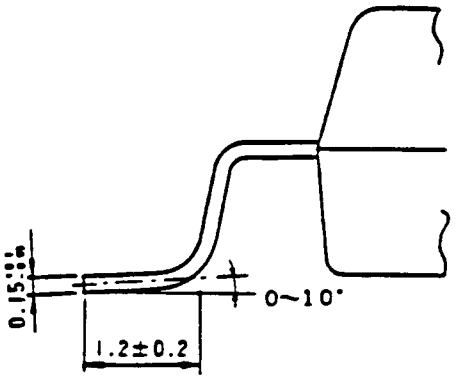
2. 2 PIN ASSIGNMENT

TOP VIEW









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3 REGISTERS

3. 1 STUFF OF REGISTERS

The TC35107F provides three 8bit registers for the operation control, two parallel data registers for transferring transmission/reception data stream, and two 8bit registers for internal status monitor. These registers are addressed by A0 and A1 into microprocessor memory or I/O space and read or written through the 8bit bus (DB0 - DB7).

The TC35107F supports serial interface compatible with CCITT V.24 (RS-232-C) and microprocessor bus interface for parallel data transfer.

The AGC gain to the programmable amplifier and frequency detect counter are readable via microprocessor bus.

3. 2 REGISTER ASSIGNMENT

A1	A0	WR/RD	REGISTER
0	0	WR	Configuration register
0	1	WR	Additional control register 1
1	0	WR	Transmission data input register
1	1	WR	Additional control register 2
0	0	RD	Modem status register
0	1	RD	INVALIED
1	0	RD	Reception data output register
1	1	RD	AGC gain output register (HALC=H) OR Frequency detect counter output register (HALC=L) Refer to the Additional control register 2.

3. 3 CONFIGURATION REGISTER (A1,A0)=(0,0) Write only (Default:11000000B)

V.27ter

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	0	0	0	FB	$\overline{L}$/S	EP

FB (Fall Back) 0: 4800bps 1: 2400bps
$\overline{L}$/S(Long/Short training) 0: Long 1: Short
EP (Echo Protection)*1 TX 0: Non echo protection
1: Echo protection
RX 0: Training enable
1: Training disable

V.29

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	0	0	1	SDS		EP

EP (Same as above)
SDS (Select Data Speed) 00: 9600bps
01: 7200bps
10: 4800bps

GROUP II

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	0	1	0	0	0	PHS

PHS (PHaSe control) 0: Off 1: On
Case of "1", POL bit of additional control register 1 is available.

GROUP I

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	1	0	0	MSEL		0

MSEL (Mode SELect) 00: AM (NTT VF)
10: FSK transmission (USA spec.)
11: FSK transmission (CCITT spec.)
- NOP in reception

V.21

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	1	0	1	0	0	0

TONE GENERATION *2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	1	1	1	FREQ			

FREQ (FREQuency)

0000:	462 Hz	1000:	1700 Hz
0001:	540	1001:	1800
0010:	1080	1010:	1850
0011:	1100	1011:	1900
0100:	1250	1100:	2100
0101:	1300	1101:	2400
0110:	1500	1110:	3240
0111:	1650	1111:	1600

*1 The EP bit means echo protection mode in transmission, and detection/non-detection of the training in reception. Occasionally, in the application of the facsimile, the similer signal to the training (alternative pattern) is included in picture signal. Therefore, preventing erroneous training, set EP to "1" except regular training. In this case, the training signal shall be ignored.

*2 If the code of tone generation is set to configuration register, modem processor begins the generation regardless of the RS (Request to Send).

3. 4 ADDITIONAL CONTROL REGISTER 1

(A1,A0)=(0,1) Write only
(Default:0*000000B) * = never change

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POL	CB	EQH	1	AGCS		FCDS	

CB (Control Bit)

OPERATION
0: DTMF generation, TONE detection
1: MODEM basic operation

FCDS (FCD level Selection)

FCD	ON	OFF
00:	-43	-48 dBm
01:	-26	-31
10:	-16	-21

AGCS (AGC type Selection)

TYPE OF AGC
00: Average type AGC
01: Peak type AGC
10: AGC hold
11: AGC hold

EQH (EQualizer Hold)

STATE
0: EQL active
1: EQL hold

POL (POLarity for G II fax)

POLARITY
0: 0^{0} phase
1: 180^{0} phase

(Note)
1. In any case, set bit 4 to one.
2. The coefficients of the automatic adaptive equalizer in G III reception is not influenced by the RST input.
3. CB (control Bit) for mode switching is not influenced by the RST input.

3. 5 ADDITIONAL CONTROL REGISTER 2 (A1,A0)=(1,1) Write only
(Default : 0000 0000B)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
			HALC	HILT	HPLS	DEL	

(1) DEL (BIT1,BIT0)
The parallel mode data clock is selected by these two bits.

BIT1	BIT0	SUITABLE CONFIGURATION	PARALLEL MODE DATA CLOCK FREQUENCY
0	0	NTT MF, GIII	DTCK x 1
0	1	GI	DTCK x 1/3 (5.184 kHz)
1	0	GII	DTCK x 2/3 (10.368 kHz)
1	1	NTT MF, GIII	DTCK x 1

(2) HPSL (BIT2)
This bit defines the transmission/reception data transfer mode between the host (DTE) and TC35107F via the microprocessor bus or serial interface. In the parallel mode, according to the diagram (shown below), the reception data output and transmission data input are performed through the microprocessor bus DB0 to DB7.
In the reception, regardless of the HPLS bit, data appears to the parallel interface and serial interface.

BIT2	MODE	A1	A0	WR/RD	OPERATION
0	Serial			--	Use TXD,RXD,DTCK (standard V.24)
1	Parallel	1	0	WR	Transmission data writing via the bus.
				RD	Reception data reading via the bus.

(3) HILT (BIT3)
This bit determines the Most Significant Bit of the modem status register.

BIT3	Definition of the Status register bit 7
0	TX (Trasmission/Reception status)
1	Interrupt request to the host processor

(4) HALC (BIT4)
This bit assigns AGC gain register or Frequency detect counter to address 3 (A1,A0)=(1,1). These are read only registers.

BIT4	Address 3 (A1,A0)=(1,1)
0	Frequency detect counter
1	AGC gain register

3. 6 MODEM STATUS REGISTER (A1,A0)=(0,0) Read only.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TX / INT	CS	SQD	G2 POL	CD	PN	P2	FCD

FCD (Fast Carrier Detect) *Invalid if AGC is held.
0: Off 1: Energy detected
P2 (Alternate pattern detect)
0: Non detect 1: Alternate pattern detected
PN (Equalizer training status)
0: Non training 1: Training in progress
CD (data Carrier Detect) *High active
0: RxD invalid 1: RxD valid
G2POL (G2 POLarity) *Valid only in G II.
0: 0° phase. 1: 180° phase
SQD (Signal Quality Detect) *Valid only in G III.
0: Good-quality 1: Poor-quality
CS (Clear to Send)
0: Non ready 1: Ready for transmission
TX (Transmission status) *In the case of HILT=0.
0: Reception 1: Transmission
INT (INTerrupt request) *in the case of HILT=1.
0: Non request 1: Interrupt request

3. 7 AGC GAIN REGISTER/FREQUENCY DETECT COUNTER (A1,A0)=(1,1) Read only

This register is provided for output AGC gain data or Frequency detect counter. The HALC bit of the Additional control register 2 chooses a register should be assigned.

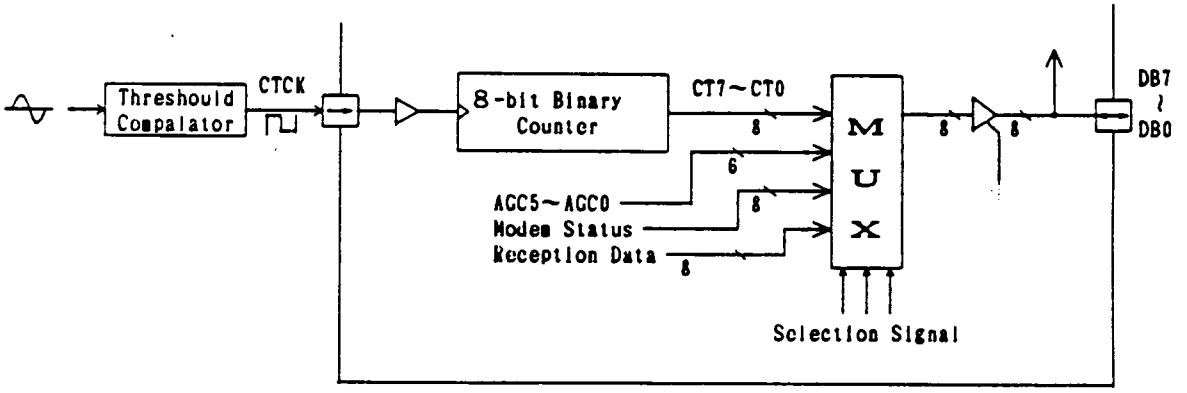
(1) AGC GAIN REGISTER (HALC=1)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0

This data corresponds to the data that appears to the AGC control output terminals (BQ1 to BQ6). When AGC5 to AGC0 are set to "1" (3F Hex-decimal), it indicates the maximum gain. The other hand, they are set to all "0" (00 Hex-decimal), it indicates the minimum gain.

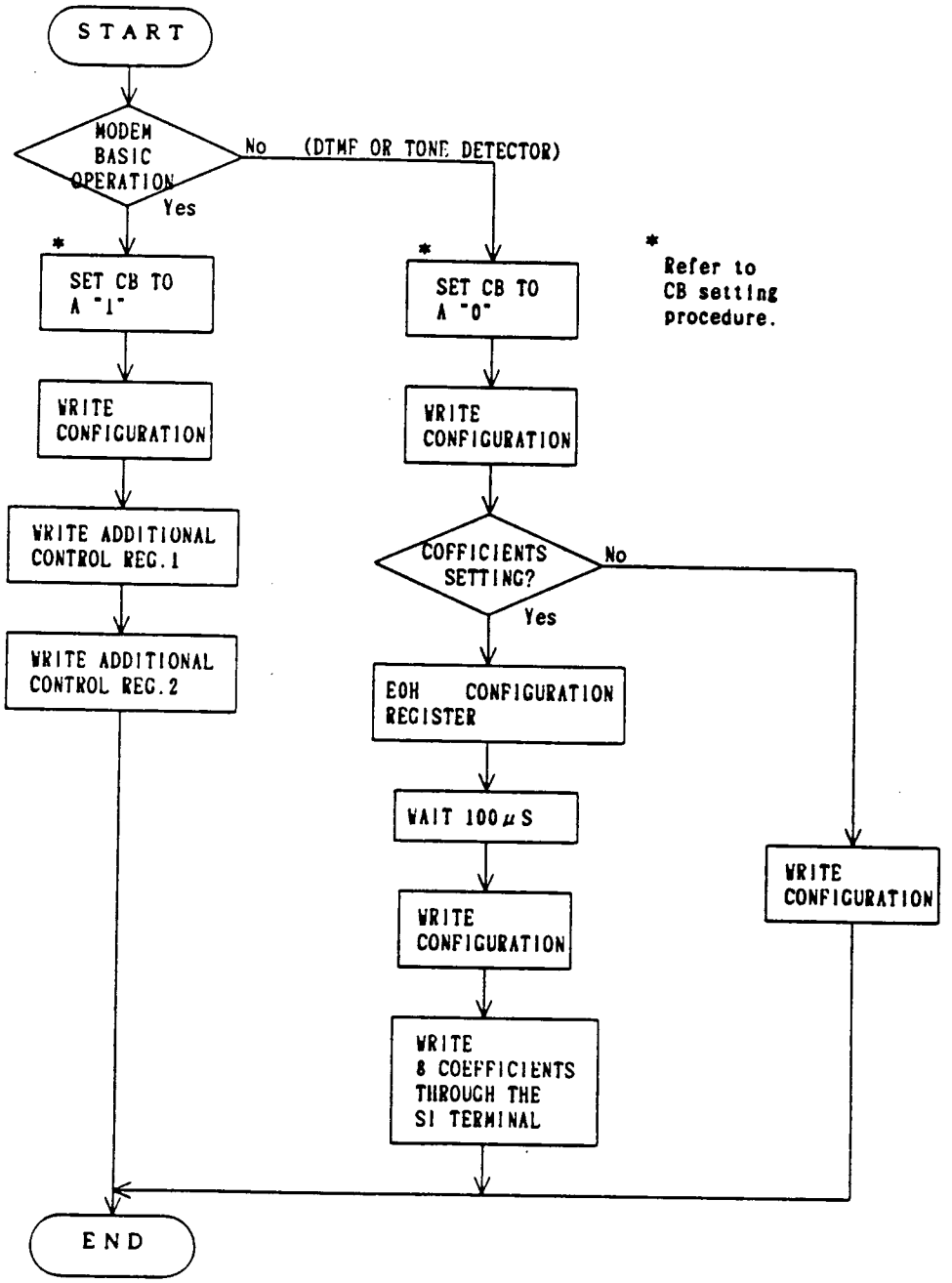
(2) FREQUENCY DETECT COUNTER (HALC=0)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

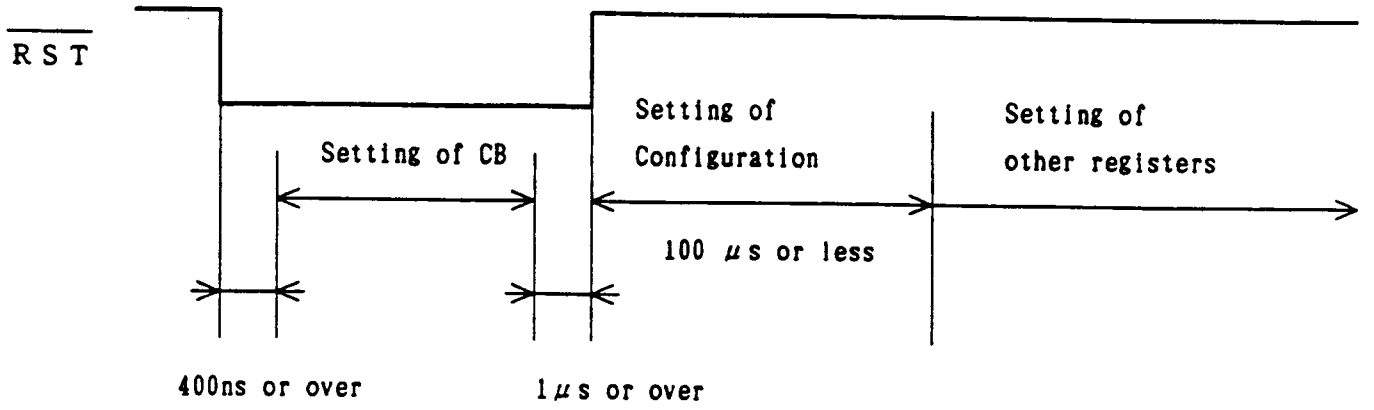


4 OPERATION

4. 1 CONFIGURATION SETTING FLOW



4. 2 SET UP TIMING



Note:

(1) At the power-on-reset, Since CB will never be initialized (never be reset), set or reset during the term of the $\overline{RST}$ low.

(2) Be sure to change the Configuration register after resetting.

(3) For changing the additional control registers 1 and 2,resetting is not required. However, in this case, never change the setting of the CB.

(4) At $\overline{RST}$=L, the Configuration register becomes C0h, the additional control register 1 becomes 00H or 40H (because the CB is not influenced by the RST input) and the additional control register 2 becomes 00H.

5 PARALLEL MODE

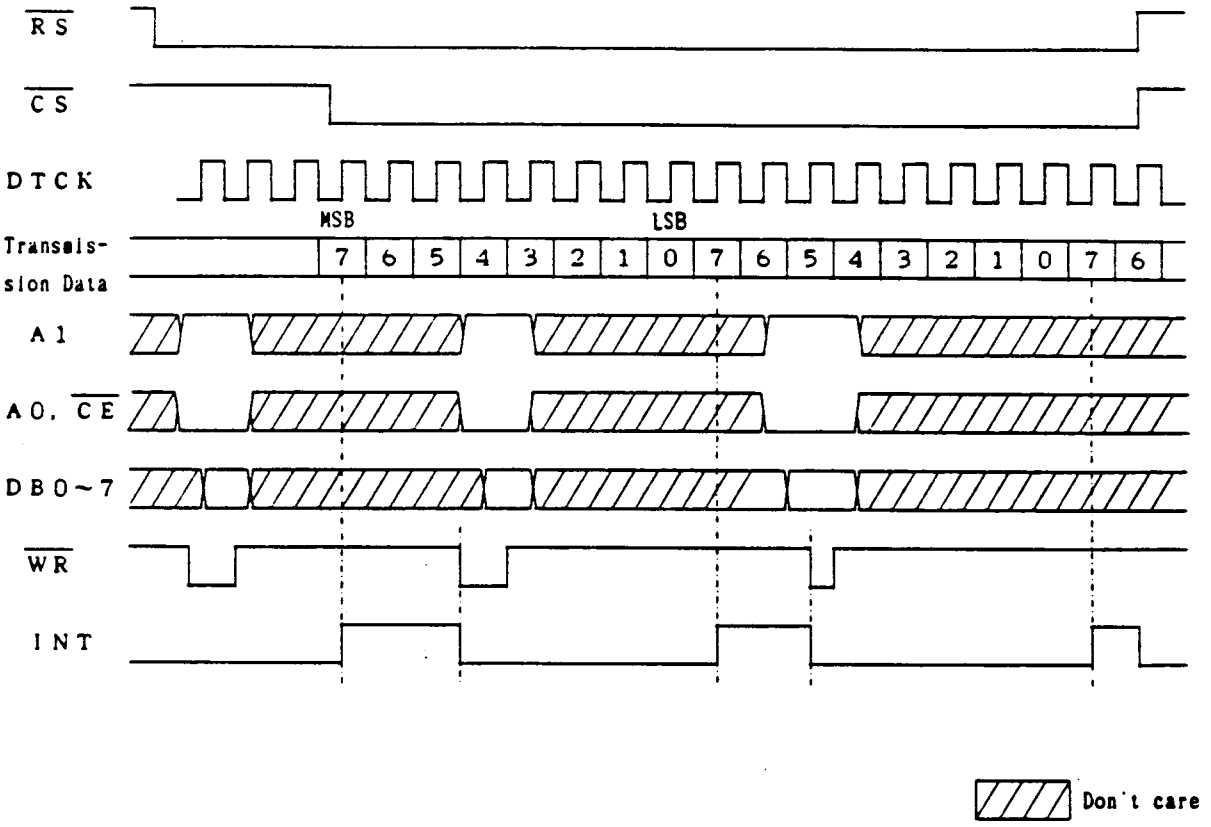
5. 1 USAGE OF THE PARALLEL MODE

The modem processor changes its data transfer mode according to the HPLS bit of the additional control register 2. In the parallel data transfer mode, reception data appears to the RxD terminal (serial interface) and reception data register (readable through the microprocessor bus) regardless of the HPLS. Interrupt request signal 'INT' for the hand-shake between host (DTE) and TC35107F is generated in the parallel data transfer mode. 'INT' signal is also output to the bit-7 of the modem status register (if HILT bit is set to 1) and goes logical one if the interrupt factor has occured. The interrupt factor means 1 byte data is received (or transmitted) and the modem generates read (or write) request to the host processor. Then host must access immediately to the data register by the interrupt or polling routine. Once the data register is accessed, 'INT' becomes zero again.

Parallel mode uses 'INT' terminal in both reception and transmission as represented above. So that if the operation has changed reception to transmission, there may be interrupt factor that generated in last reception. It is needed to clear such illegal interrupt factor. In the case of changing from transmission to reception, illegal interrupt factor disappears automatically.

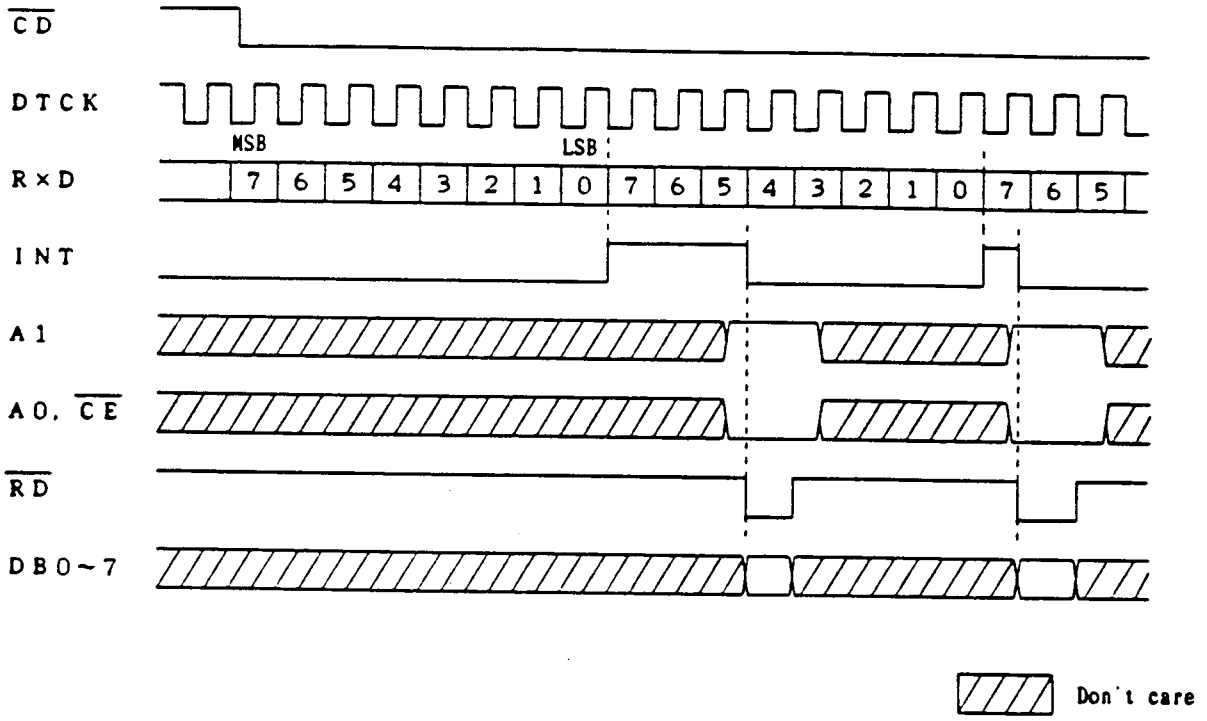
For more details, refer to the timing chart drawn later.

5. 2 PARALLEL MODE TRANSMISSION TIMING



Note:
Write first transmission data before $\overline{CS}$ becomes Low.

5. 3 PARALLEL MODE RECEPTION TIMING



Note:
During a reception term, received data will be provided from serial interface and reception data register (A1,A0)=(1,0).

6 CONTROL SIGNAL SEQUENCE

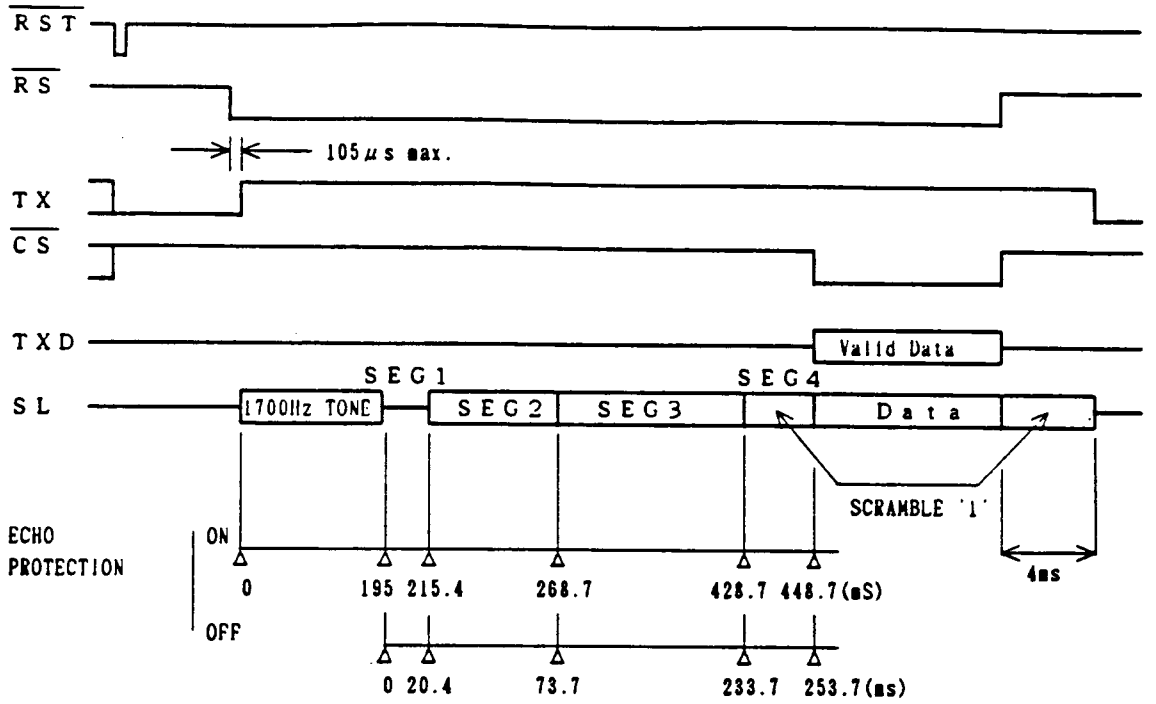
This modem processor is capable of 300 to 9600bps data transfering suitable for Group III facsimile. Then, turn-on/turn-off sequence and response time of Clear-to-Send may be changed according to its configuration.

In Group II reception mode, modem requires switching of AGC type in order to trace received line signal.

For the reference of understandings of these circumstances, this section describes the control signal sequence.

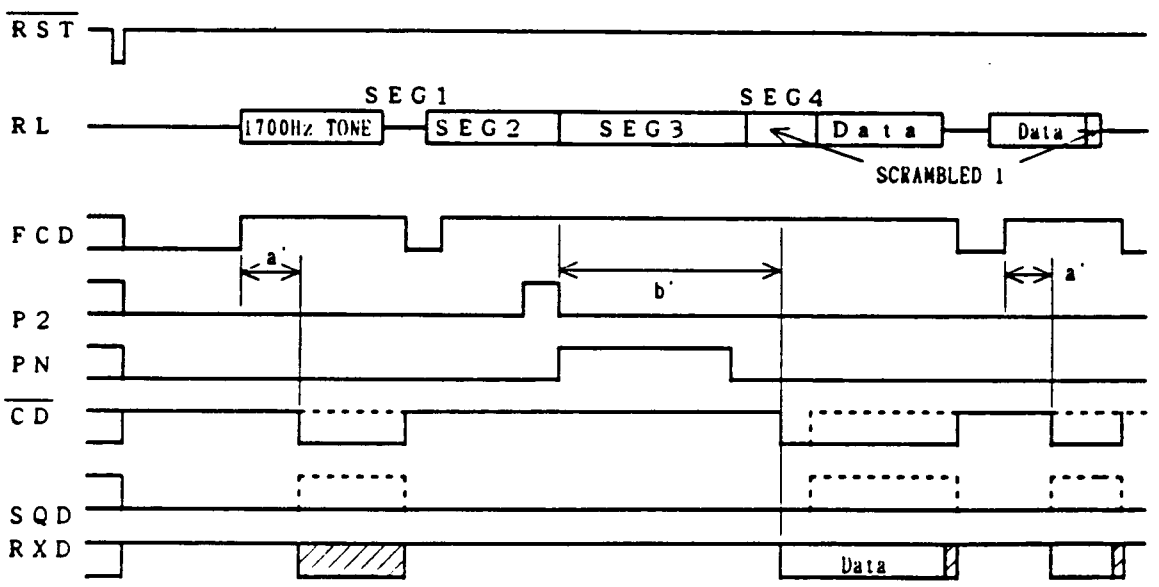
6. 1 V.29 SEQUENCE

(A) TRANSMISSION



Note:
Response time of $\overline{RS}$ to $\overline{CS}$ is different from CCITT V.29 specification.

(B) RECEPTION

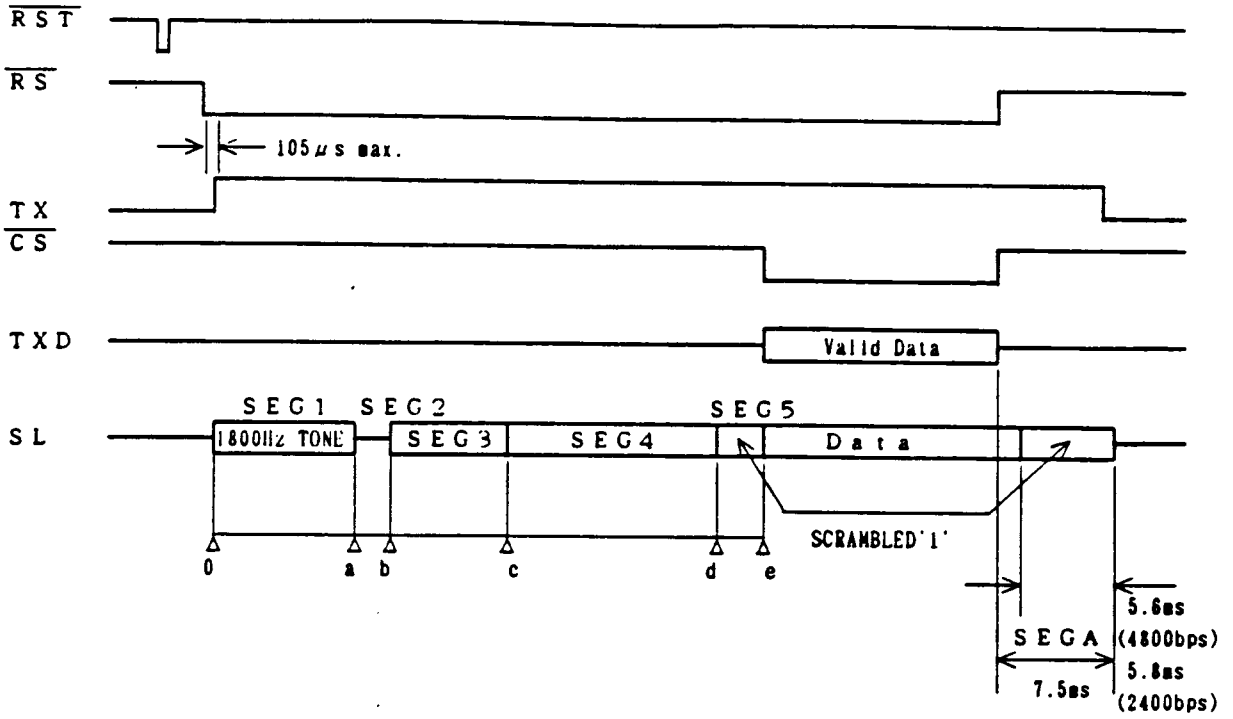


(Broken-line portion show failure of reception.)

a' =47.5ms
b' =170ms

6. 2 V.27ter SEQUENCE

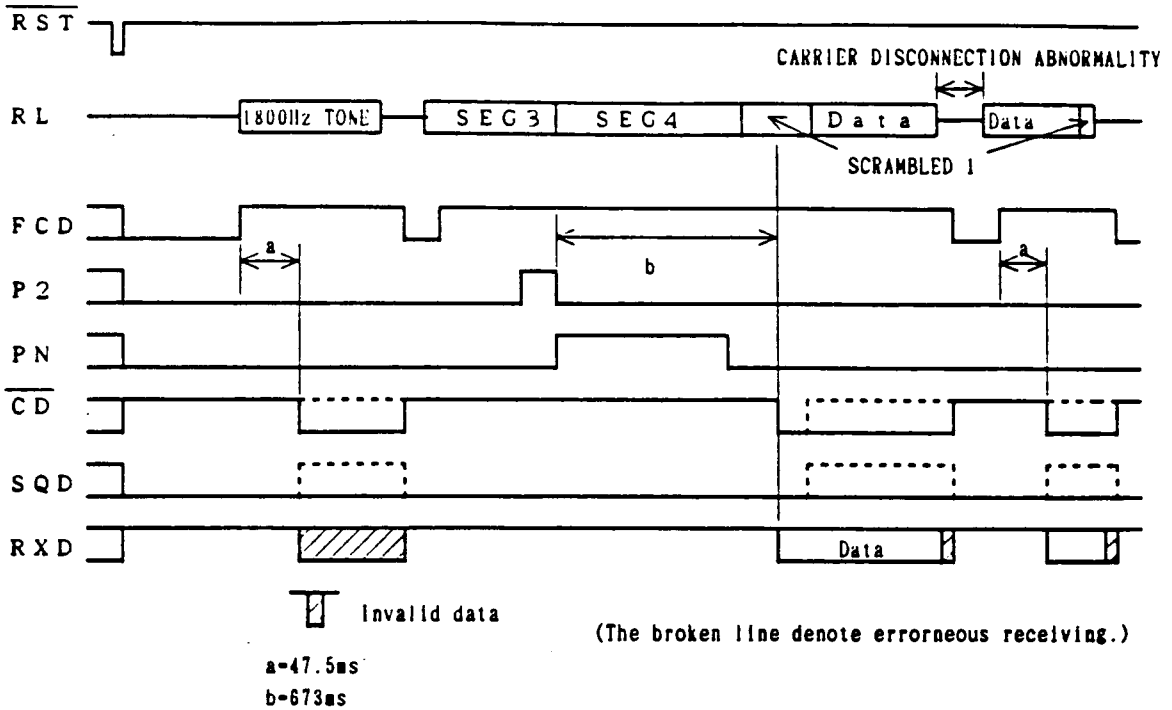
(A) TRANSMISSION



			a	b	c	d	e
Echo Protection ON	Long	4800bps	195.0	215.4	246.7	917.9	922.9
		2400bps	195.0	215.4	257.1	1152.1	1158.7
	Short	4800bps	195.0	215.4	224.2	260.4	265.4
		2400bps	195.0	215.4	227.1	275.4	282.1
Echo Protection OFF	Long	4800bps	0	0	31.3	702.5	707.5
		2400bps	0	0	41.7	936.7	943.3
	Short	4800bps	0	0	8.8	45.0	50.0
		2400bps	0	0	11.7	60.0	66.7

(ms)

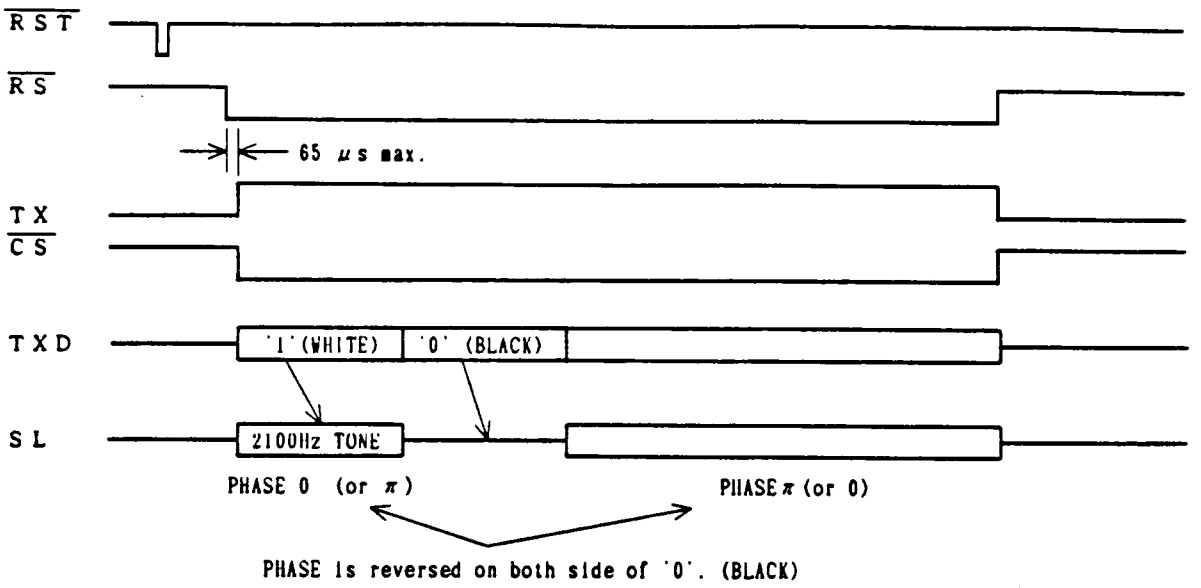
(B) RECEPTION



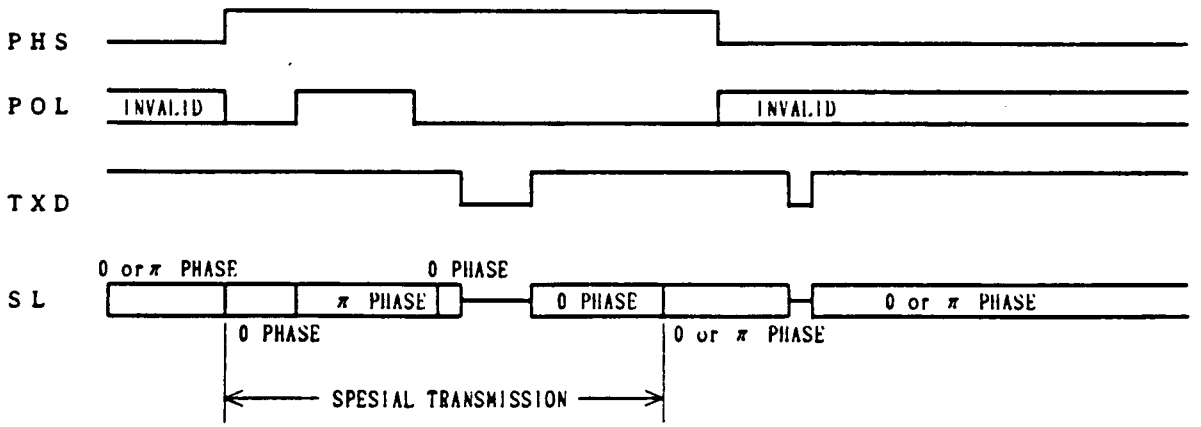
Note:
This is the case of V.27ter long training. The TC35107F can receive V.27ter with short training. Since the training detection is impossible in this mode, the training will be ignored and internal software timer in the modem processor makes $\overline{CD}$ active 47.5ms after the rising edge of FCD. As a result, initialize of the automatic adaptive equalizer coefficients can not be performed in short training. At least, long training for initializing coefficients is required in the first connection of the line. If the coefficients were already set, correct reception data will appear even if V.27ter with short training.

6. 3 Group II SEQUENCE

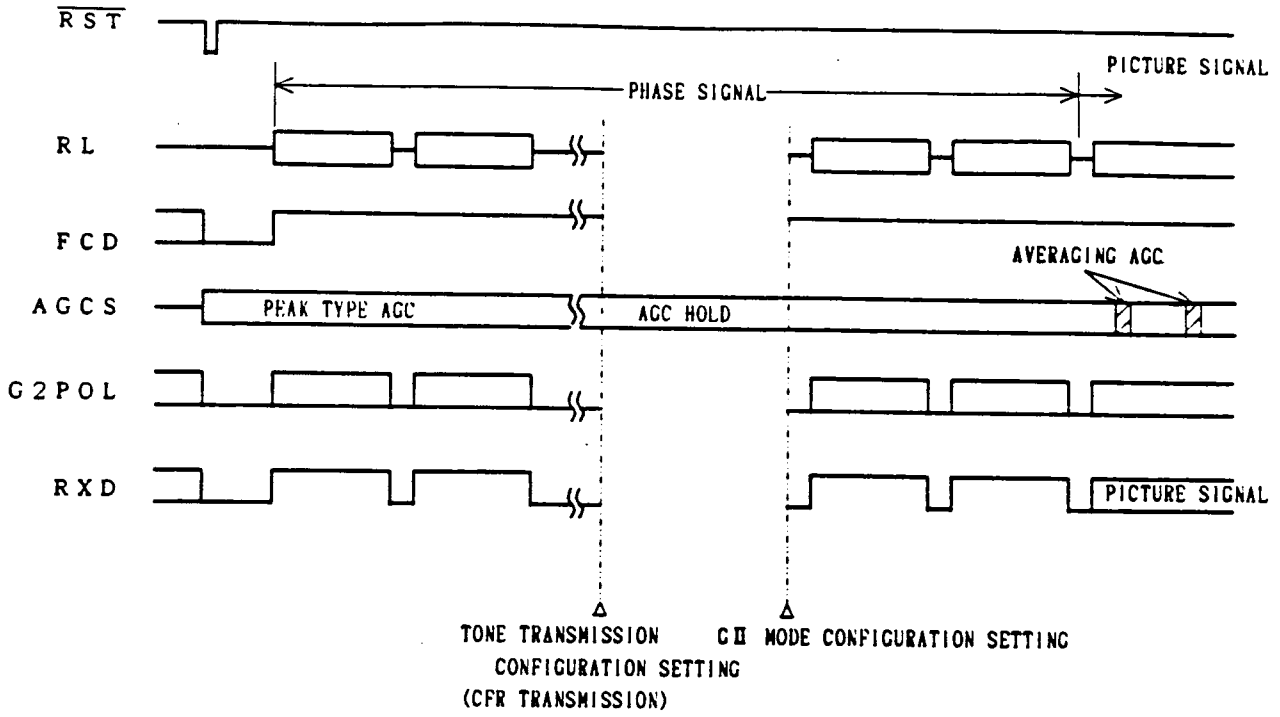
(A) NORMAL TRANSMISSION



(B) SPECIAL TRANSMISSION (PHS = H. See additional control register1.)



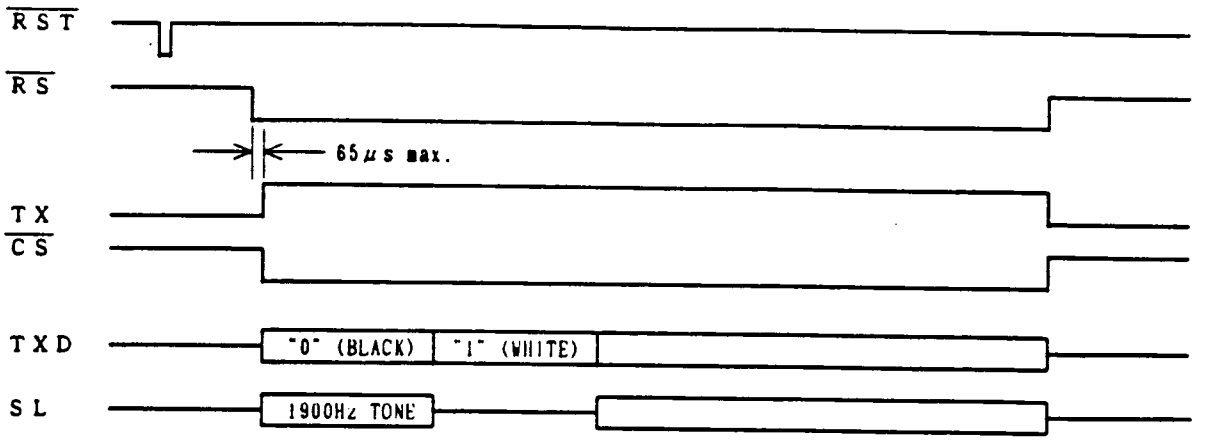
(C) RECEPTION



Note:
(1) This is an instance of AGC type switching.
(2) When changing the operation mode for CFR transmission (See CCITT T.30 facsimile procedure) and reentering into this mode, do not hardware reset. Or synchronization of software PLL circuit will not be maintained.
(3) If the judgement of NTT VF/MF mode is required, set VF mode first and watch the stream of reception data.

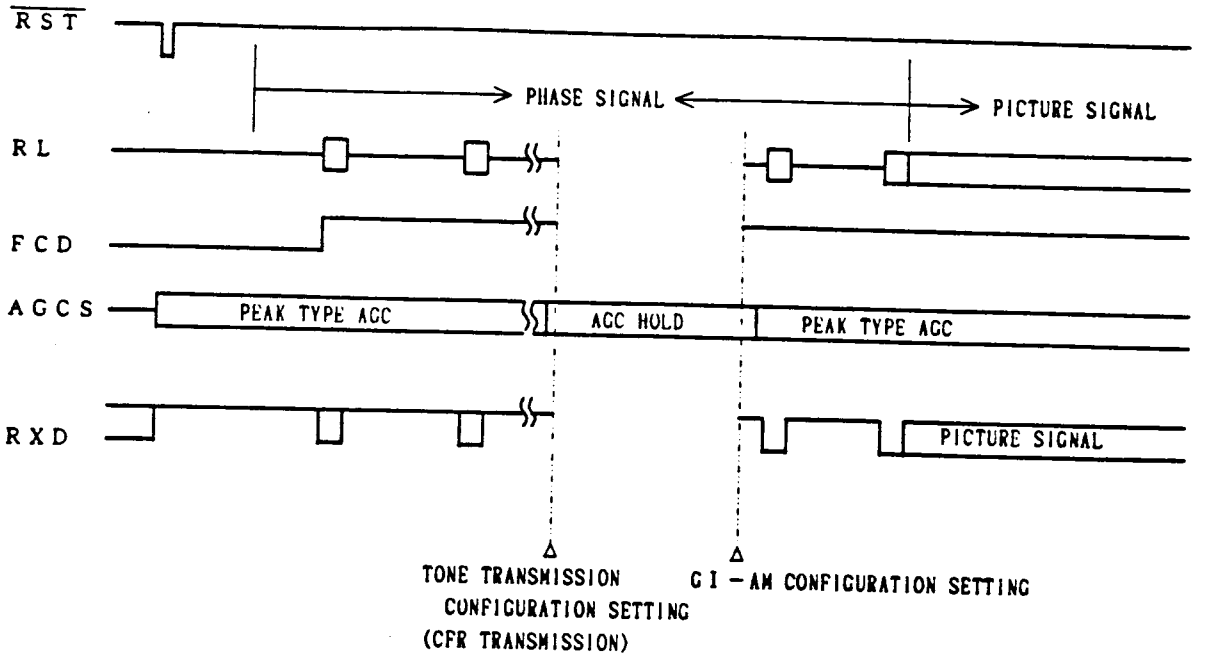
6. 4 Group I -AM (NTT VF) SEQUENCE

(A) TRANSMISSION



* TXD sampling frequency is 15.552KHz.

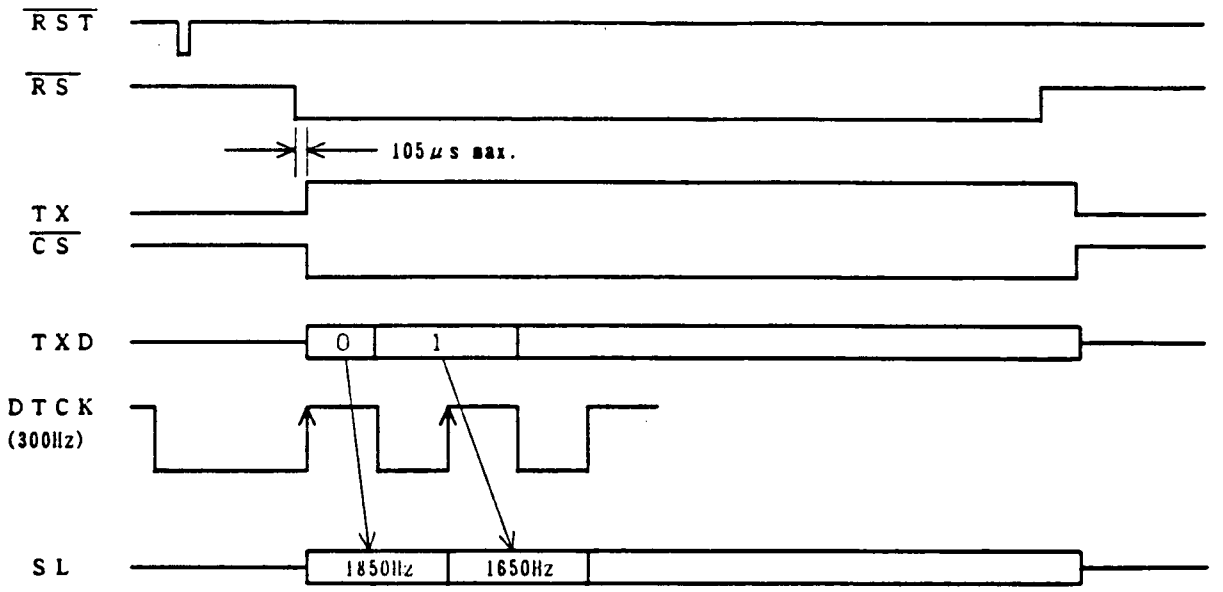
(B) RECEPTION



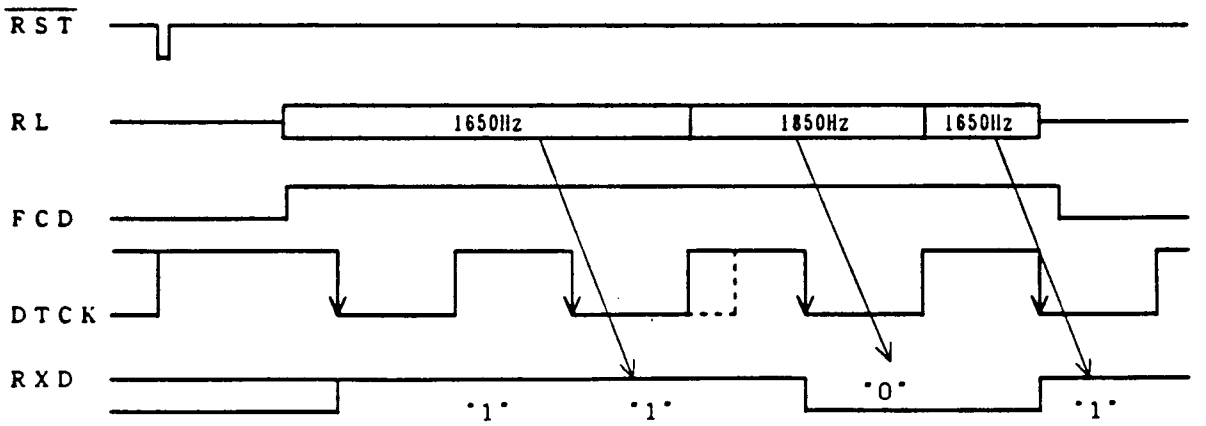
Note:
(1) This is an instance of AGC type switching.
(2) When changing the operation mode for CFR transmission and reentering into G I mode, do not hardware reset. Or the gain of AGC will not be kept.

6. 5 V.21

(A) TRANSMISSION



(B) RECEIVING



Note:

The modem generates DTCK (DaTa ClocK) by deviding master clock. This master clock runs freely regardless of received data stream but, internal hardware circuits connected to devider clears its count at the changes of the data. Therefore, DTCK automatically synchronize to data stream.

7 OTHER FUNCTIONS

The TC35107F assumes DTMF generator or programmable tone detector accomplished by the software signal processing. Set CB (Control Bit. Refer to ADDITIONAL DATA REGISTER 1.) to zero to invoke these functions.

7. 1 DTMF GENERATOR

This LSI is capable of generating Dual Tone Multi Frequency signal for dialing or applications. Just writing configuration code to the register, generating starts immediately no matter what RS is inactive.

Configuration code

7	6	5	4	3	2	1	0
TL	TH	1	1	HGS		LGS	

TL (Low group tone level)
1:Low group fixed level 0:Low group inhibit

TH (High group tone level)
1:High group fixed level 0:High group inhibit

HGS (High Group frequency Selection)
00:1209Hz 01:1336
10:1477 11:1633

LGS (Low Group frequency Selection)
00: 697Hz 01: 770
10: 852 11: 941

Note:
At TL=TH=0, signal level is defined by the coefficients which is set in the coefficients setting mode (described later).

7. 2 TONE DETECTION

This is a single tone detect function accomplished by software signal processing and output result to FCD bit of modem status register. FCD=1 indicates detection of the energy at selected frequency. This LSI provides coefficients for specified frequency detection. Coefficients are selected by configuration code.
Furthermore, coefficients writing mode allows rewriting these coefficients. Then, user defined coefficients are available.

Configuration code

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DL	1	0	0	FREQ			

DL (Detection Level)
0: approx. -43 dBm 1: approx. -52 dBm

FREQ (FREQuency)

0001: 462 Hz	0100: 1650 Hz
0010: 1100 Hz	0101: 1850 Hz
0011: 1300 Hz	0110: 2100 Hz
1000: 400 Hz	0111: User defined frequency

Note:
User defined frequency (FREQ = 0111) is determined by the coefficients set to modem processor. Coefficients calculation method is described later.

7. 3 COEFFICIENTS WRITING

This is the mode for using more flexibly the tone detect function and DTMF generator. The required coefficients are written into the LSI through the SI (serial input) terminal.

1st:
When E0h is written into the mode register after resetting, the LSI begins to wait the serial input from SI terminal. Once LSI begins to wait, regardress of the configuration, modem does not change the mode until 8 coefficients are written through the SI terminal.

2nd:
For ensuring the operation, wait for about 100us until the LSI turns into the waiting state for input.

3rd:
Write tone detection code or DTMF generation code to the mode register.

4th:
Make $\overline{\text{SIEN}}$ enable and input serial data to the SI terminal with synchronous clock to the SICK terminal. The coefficients should be 2's complement form. Be sure to write 8-word of coefficients. The coefficients are transferred by MSB first.

Then:
After the writing of coefficients, LSI begins tone detection or DTMF generation immediately.

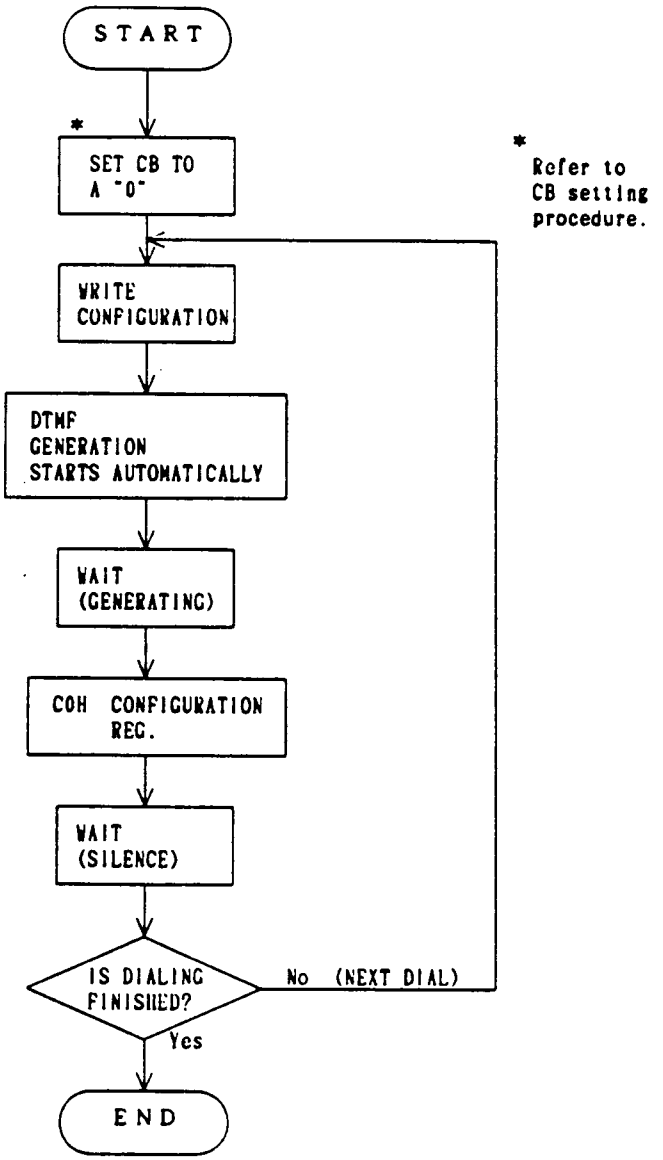
7. 4 FUNCTION HALT

Write C0h to the configuration register and make RS inactive, then the LSI halts its function. That is, the LSI halts DTMF generation or tone detection. (FCD flag does not change.) This configuration avails only the case of CB = 0.

8 APPLICATION SOFTWARE

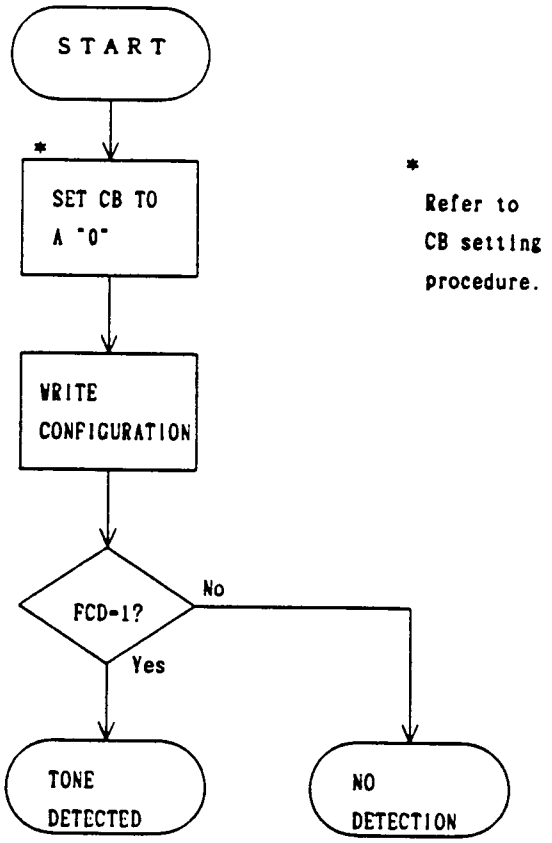
8. 1 DIALING FLOW CHART

FIXED LEVEL DTMF GENERATION



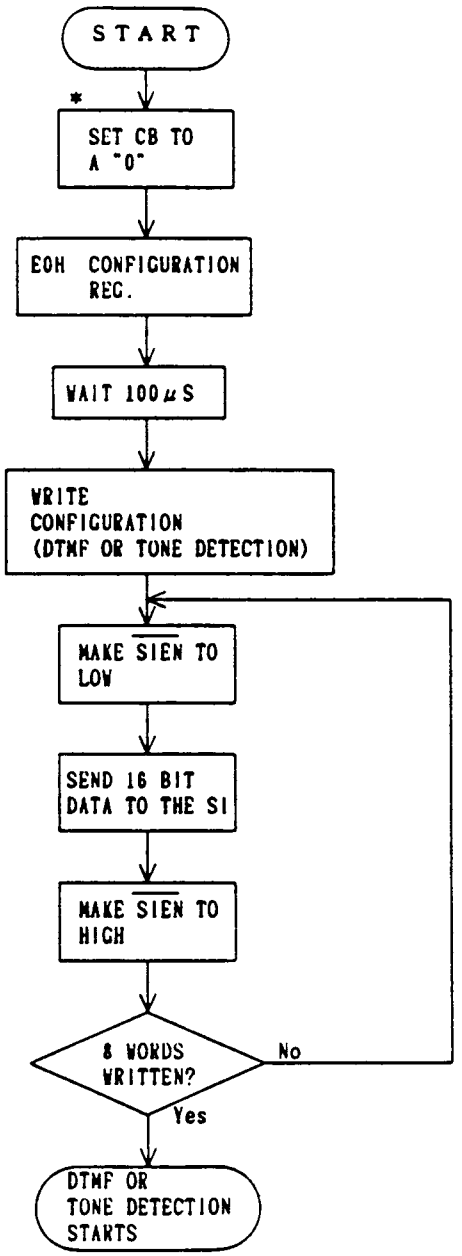
8. 2 TONE DETECTION FLOW CHART

SPECIFIED TONE DETECTION



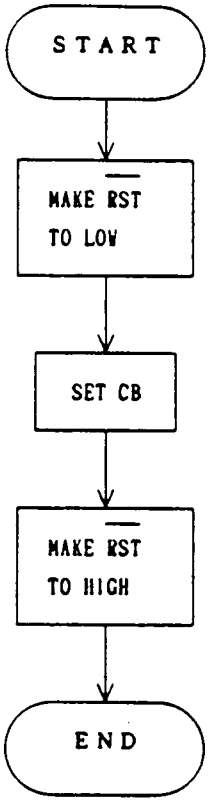
Note:
Keep RS inactive while the detection. FCD bit indicates detection result.

8. 3 COEFFICIENTS WRITING FLOW CHART



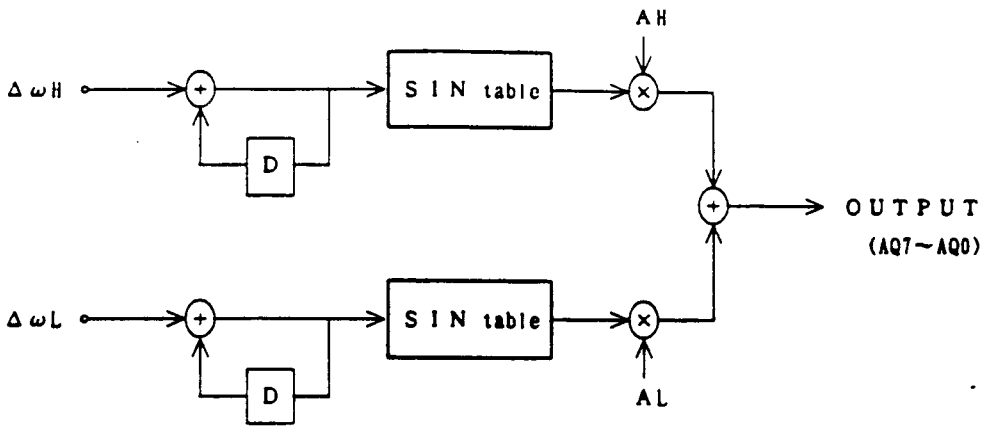
* Refer to CB setting procedure.

CB (Control Bit) SETTING PROCEDURE



9 SIGNAL PROCESSING

9. 1 DTMF SIGNAL FLOW



At coefficients setting mode, write the coefficients in order of AH to AL and write 0000h six times as dummy. At this time, set AH+AL 7FFFh (≈ 1.0).

At fixed transfer level, AH=1223h (0.1416931) and AL=0E68h (0.1125488).

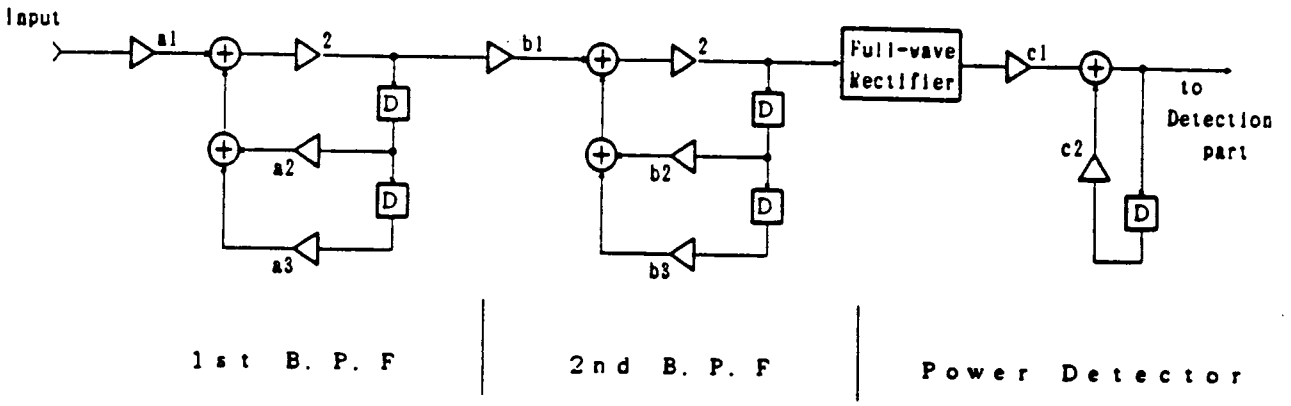
At this time, the digital data which are output to the transmission signal outputs AQ7 to AQ0 become 60h (min.) to A0h (max.) at peak to peak.

The level difference between the low group and the high group is 2 dB.

DTMF GENERATOR FREQUENCY DEVIATION (Deviation of system clock is not included.)

Frequency of Low or High Group(Hz)		ERROR (Hz)	DEVIATION(%)
STANDARD VALUE	ACTUAL VALUE		
697	696.96	-0.04	-0.0057
770	769.82	-0.18	-0.0234
852	851.92	-0.08	-0.0094
941	940.91	-0.09	-0.0096
1209	1208.83	-0.17	-0.0141
1336	1335.79	-0.21	-0.0157
1477	1476.98	-0.02	-0.0014
1633	1632.89	-0.11	-0.0067

9. 2 TONE DETECTOR SIGNAL FLOW



Write the eight coefficients in the order of a1, a2, a3, b1, b2, b3, c1, and c2.

9. 3 COMPUTATION OF TONE DETECTOR COEFFICIENTS

The tone detector consists of two second-order filters in cascade, a power detector and a comparator as shown in the signal flow on the previous page.

The first and second filter have transfer functions Ha(z) and Hb(z). The power detector has a transfer function Hc(z). Each function is shown below.

$(z=e^{-jwt})$

$$Ha(Z) = \frac{2a_1 Z^2}{Z^2 - 2a_2 Z - 2a_3} \qquad (1)$$

$$Hb(Z) = \frac{2b_1 Z^2}{Z^2 - 2b_2 Z - 2b_3} \qquad (2)$$

$$Hc(Z) = \frac{c_1 Z}{Z - c_2} \qquad (3)$$

STEP 1:

Transfer function (1) has a conjugate pair of poles P1 and P2.

$$p1 = a_2 + j\sqrt{a_2^2 + 2a_3}$$
$$p2 = a_2 - j\sqrt{a_2^2 + 2a_3} \qquad (4)$$

These poles lie on the circle of radius R on the Z-plane.

$$\cos^{-1}\frac{a_1}{R} = \theta = 360^\circ \times \frac{f0}{fs} \qquad (5)$$

fs: sampling frequency
fo: center frequency of filter

from equation (4), R is represented by:

$$R = \sqrt{a_2^2 + (-a_2^2 - 2a_3)} \qquad (6)$$

Solving for a2 and a3:

$$a_2 = R \cdot COS\left(360° \times \frac{f0}{fs}\right) \quad (7)$$

$$a_3 = -\frac{R^2}{2} \quad (8)$$

In these equations, only Ha(z) is considered. The tone detector consists of two similar Band Pass Filters in cascade. The center frequency of each BPF should be shifted above and below to the desired center frequency. Therefore, a response with the desired band width is achieved.

Considering band width B:

$$fa = 0.72 \times \frac{B}{2}$$

$$fa' = 0.99\, fa$$

fo-f'a and fo+fa individually become the center frequency.
Then the filter coefficients are given by:

$$a_1 = b_1 = \begin{cases} \dfrac{(104/319)\, f0 - 78.62}{32767} & 500 \le f0 \le 1100\,Hz \\ \dfrac{(44/275)\, f0 + 104}{32767} & 1100 \le f0 \le 1650\,Hz \\ \dfrac{(4/45)\, f0 + 221}{32767} & 1650 \le f0 \le 3000\,Hz \end{cases}$$

$$a_2 = R \cdot COS\left[360° \times (f0 - fa')/fs\right]$$

$$b_2 = R \cdot COS\left[360° \times (f0 + fa)/fs\right]$$

$$a_2 = b_2 = -\frac{R^2}{2}$$

The poles must lie inside of the unit circle on the Z-plane because of stability of the filter. When R≥1, stability can not be expected. In this application, R=0.994030884 is recommended.

STEP2:

Next, decide the coefficients C1 and C2 of the power detector. When the detection delay time is τ, C1 and C2 are represented as:

$$c_1 = \frac{1}{1+9600\tau} \qquad c_2 = \frac{1}{1+\frac{1}{9600\tau}}$$

10 ELECTRICAL CHARACTERISTICS

10. 1 MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.5 - 7.0	V
Input Voltage	VIN	-0.5 - 7.0	V
Output Voltage	VOUT	-0.5 - 7.0	V
Input Current	IIN	+20	mA
Output Current	IOUT	+20	mA
Power Dissipation	Pd	1.3	W
Storage Temperature	Tstg	-55 - 150	℃
Soldering Temperature (10 sec)	Tsol	260	℃

RECOMMENDED OPERATIONAL CONDITION

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD			4.75	5.0	5.25	V
Input Voltage	VIN			0		VDD	V
System Clock Frequency Deflection	f	VDD=5.0V+5% fCLK=6.2208MHz (TYP)	at GI and GII	-5		5	ppm
			other than the above	-100		100	ppm
Operating Temperature	Topr			0		70	℃

10. 2 DC CHARACTERISTICS (VDD=4.75 - 5.24V, Ta= 0 - 70℃)

CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Consumption Current	IDD	VDD	VDD=5.25V CLK=6.3MHz			120	mA
Terminal group 1 High Level Input Voltage	VIH(1)	DB0 - DB7 A1, A0, $\overline{CE}$ $\overline{WR}$, $\overline{RD}$, $\overline{RS}$, TXD, ST1		2.4			V
Terminal group 1 Low Level Input Voltage	VIL(1)					0.8	V
Terminal group 2 High Level Input Voltage	VIH(2)	All the input terminals except mentioned above terminals.		0.7 VDD			V
Terminal group 2 Low Level Input Voltage	VIL(2)					0.3 VDD	V VDD
Low Level Input Current (1)	IIL(1)	CD0 - CD7	VIN=GND	-750*	-500*	-365*	uA
High Level Input Current (1)	IIH(1)		VIN=VDD			10	uA
Low Level Input Current (2)	IIL(2)	DB0 - DB7	VIN-GND	-250*	-165*	-120*	uA
High Level Input Current (2)	IIH(2)		VIN-VDD			10	uA
Low Level Input Current (3)	IIL(3)	All the input terminal other than the above	VIN=GND	-1.0			uA
High Level Input Current (3)	IIH(3)		VIN=VDD			1.0	uA
Low Level Output Current (1)	IOL(1)	DB0 - DB7 DTCK, RXD $\overline{CD}$, $\overline{CS}$	VOL=0.4V	3.2			mA
High Level Output Current (1)	IOH(1)		VOH=2.4V			-3.0	mA
Low Level Output Current (2)	IOL(2)	All the input terminals except mentioned above terminals and BSORQ	VOL=0.4V	2.0			mA
High Level Output Current (2)	IOH(2)		VOH=2.4V			-100	mA
Low Level Output Current (3)	IOL(3)	$\overline{BSORQ}$	VOL=0.4V	2.0			mA
High Level Output Voltage	VOH	All the input except $\overline{BSORQ}$	IOH=-10uA	4.5			V
High Level Output Off-leak Current	IDH	$\overline{BSORQ}$, BSO	VDH=VDD			10	uA
Low Level Output Off-leak Current	IDL		VDL=GND	-10			uA

10. 3 AC CHARACTERISTICS (VDD=4.75 - 5.25V, Ta= 0 - 70 ℃)

DATA BUS WRITE TIMING

CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Data Bus Write Pulse Width	TWW (2)	$\overline{WR}$	Cin=10pF	120*			nS
Data Write Register Selection Input Set-up Time	Tset (5)	A0,A1	Cin=10pF	50*			nS
Data Write Register Selection Input Hold Time	Thold (5)	A0,A1	Cin=10pF	30*			nS
Data Bus Data Set-up Time	Tset (2)	DB0 - DB7	Cin=10pF	60			nS
Data Bus Data Hold Time	Thold (2)	DB0 - DB7	Cin=10pF	35*			nS

* : Temporary

DATA BUS READ TIMING

CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Data Bus Read Pulse Width	TWR (2)	$\overline{RD}$	Cin=10pF	200*			nS
Data Read Register Selection Input Set-up Time	Tset (6)	A0,A1	Cin=10pF	50*			nS
Data Read Register Selection Input Hold Time	Thold (6)	A0,A1	Cin=10pF	30*			nS
Data Bus Output Enable Time	Tpzh (2) Tpzl (2)	DB0 - DB7	CL=100pF RL=1.5 k Ohm			150	nS
Data Bus Output Disable Time	Tphz (2) Tplz (2)	DB0 - DB7	CL=100pF RL=1.5 k Ohm			150*	nS

* : Temporary

OPERATION TIMING

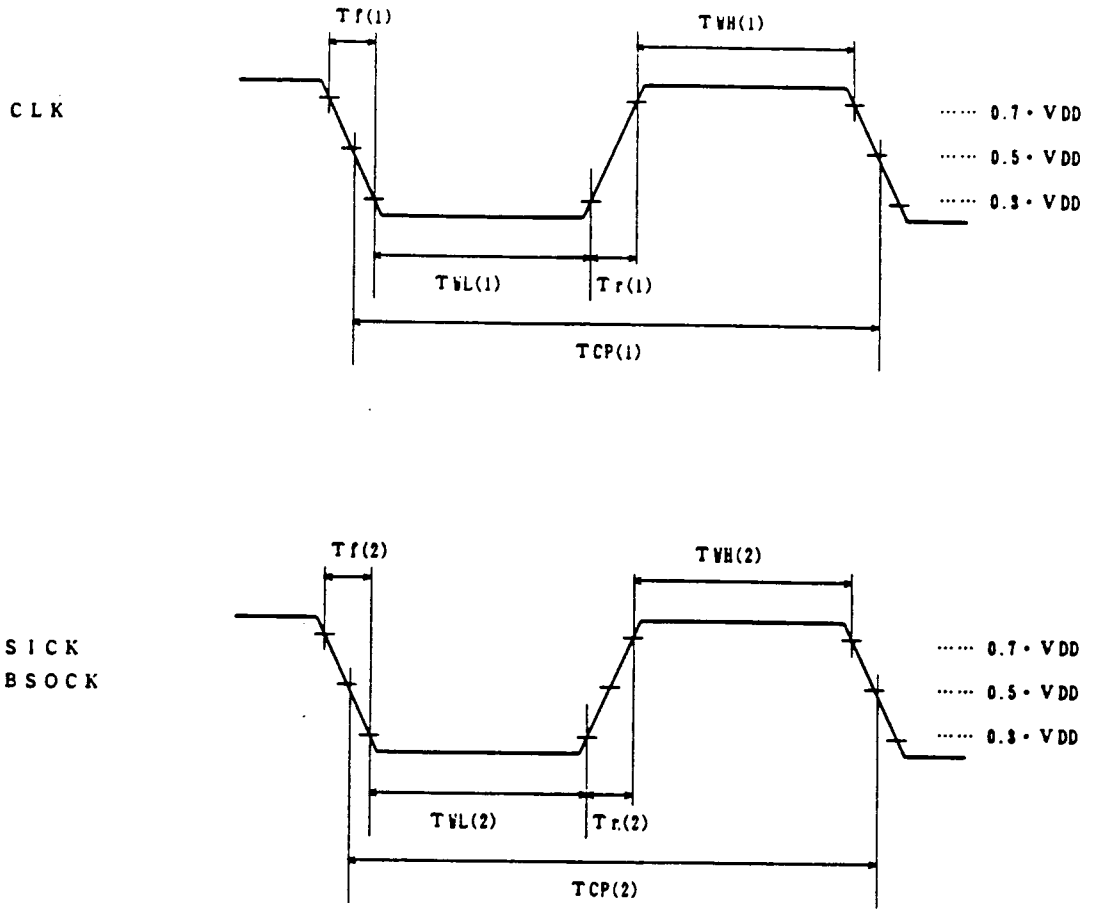
CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock synchronization (1)	TCP (1)	CLK	Cin= 10 pF	160			nS
Clock Synchronization (2)	TCP (2)	SICK,SOCK	Cin= 10 pF	1040			nS
System Clock Width	TWH (1) TWL (1)	CLK	Cin= 10 pF	60			nS
Serial Data Synchronous Clock Width	TWH (2) TWL (2)	SICK,SOCK	Cin= 10 pF	500			nS
System Clock Rise Time	Tr (1)	CLK	Cin= 10 pF			15	nS
System Clock Fall Time	Tf (1)	CLK	Cin= 10 pF			10	nS
Serial Data Synchronous clock Rise Time	Tr (2)	SICK,SOCK	Cin= 10 pF			20	nS
Serial Data synchronous clock Fall Time	Tf (2)	SICK,SOCK	Cin= 10 pF			20	nS
System Reset Pulse Width	TWRST	RST,CRST	Cin= 10 pF	450			nS

SERIAL DATA INPUT TIMING

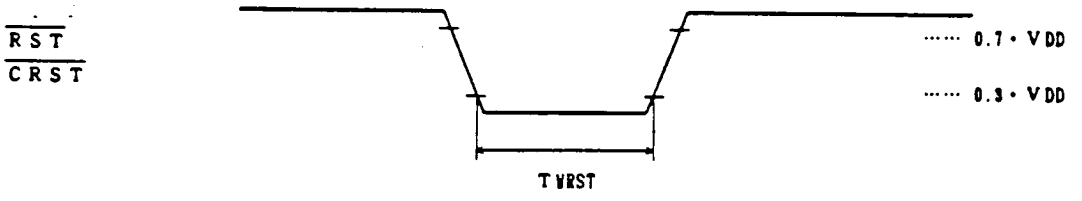
CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Serial Data Input Data Set-up Time	Tset(7)	SI	Cin=10pF	30			nS
Serial Data Input Data Hold Time	Thold(7)	SI	Cin=10pF	200			nS
Data Input Disable Data Set-up Time	Tset (8)	$\overline{SIEN}$	Cin=10pF	20			nS
Data Input Disable Data Hold Time	Thold(8)	$\overline{SIEN}$	Cin=10pF	30			nS

SERIAL DATA OUTPUT TIMING

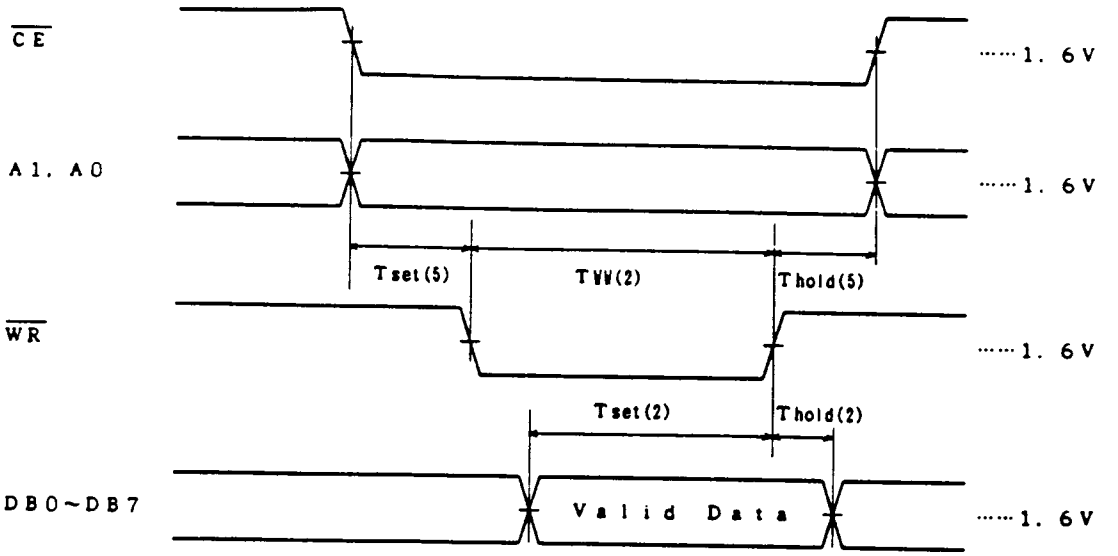
CHARACTERISTIC	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
Serial Data Output Enable Time	Tpzh(3) Tpzl(3)	BSO	CL=100pF RL=1.5k Ohm			170	nS
Serial Data Output Delay Time	Tphl(1) Tplh(1)	BSO	CL=30pF			170	nS
Serial Data Output Disable Time	Tphz(3) Tplz(3)	BSO	CL-100pF RL=1.5k Ohm			500	nS
Serial Data Request Output Enable Time	Tpzl (4)	$\overline{BSORQ}$	CL=30pF RL=1.5k Ohm			170	nS
Serial Data Request Output Disable Time	Tplz (4)	$\overline{BSORQ}$	CL=30pF RL=1.5k Ohm			170	nS



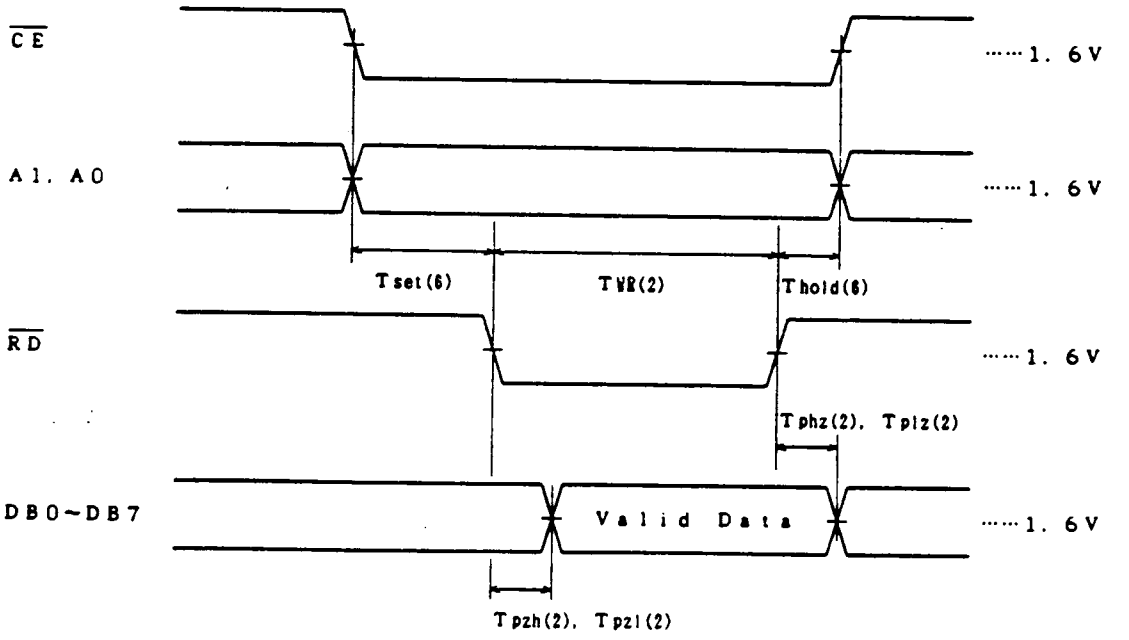
Input Clock Wave Form



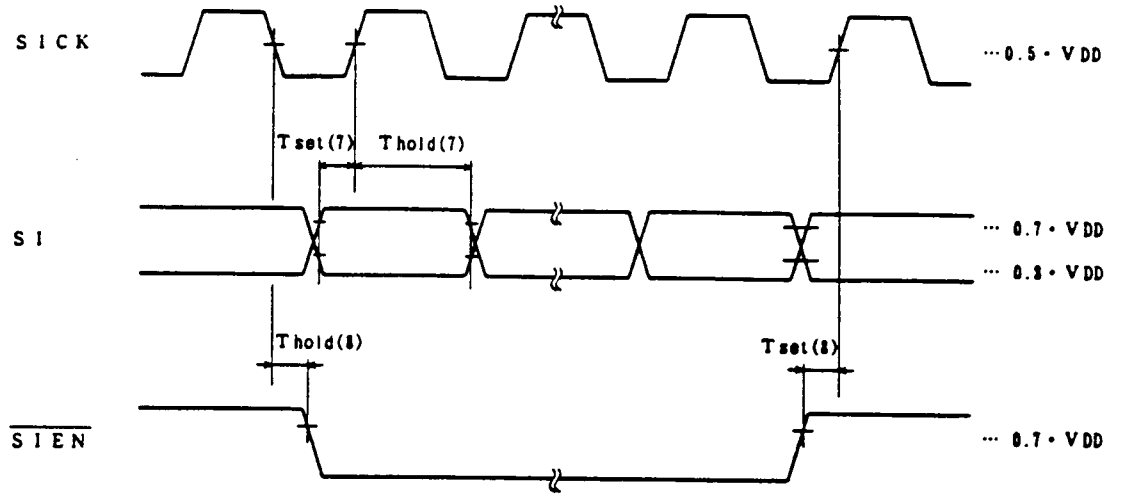
System Reset Pulse Wave Form



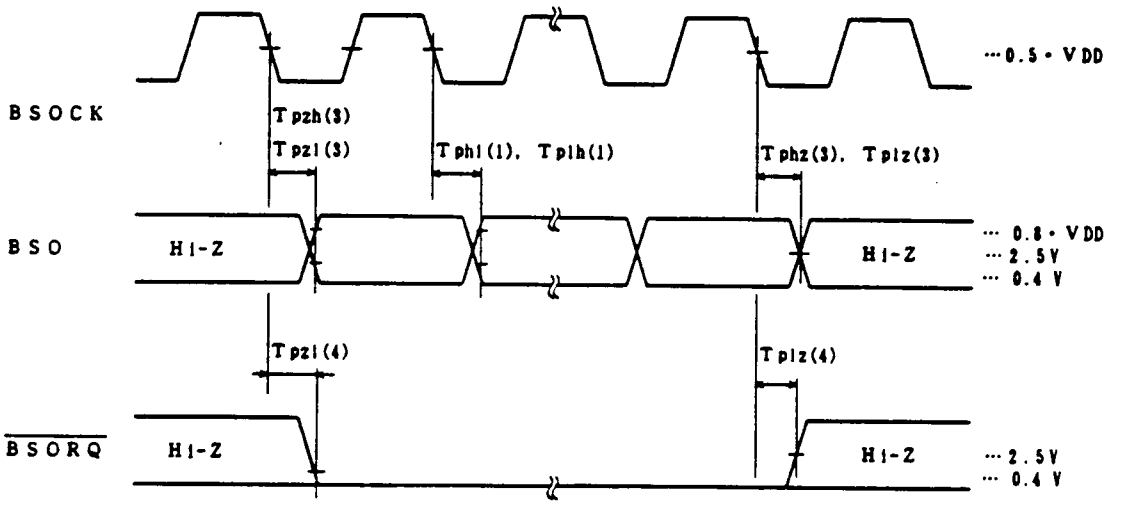
8bit Data Bus Write Timing



8bit Data Bus Read Timing



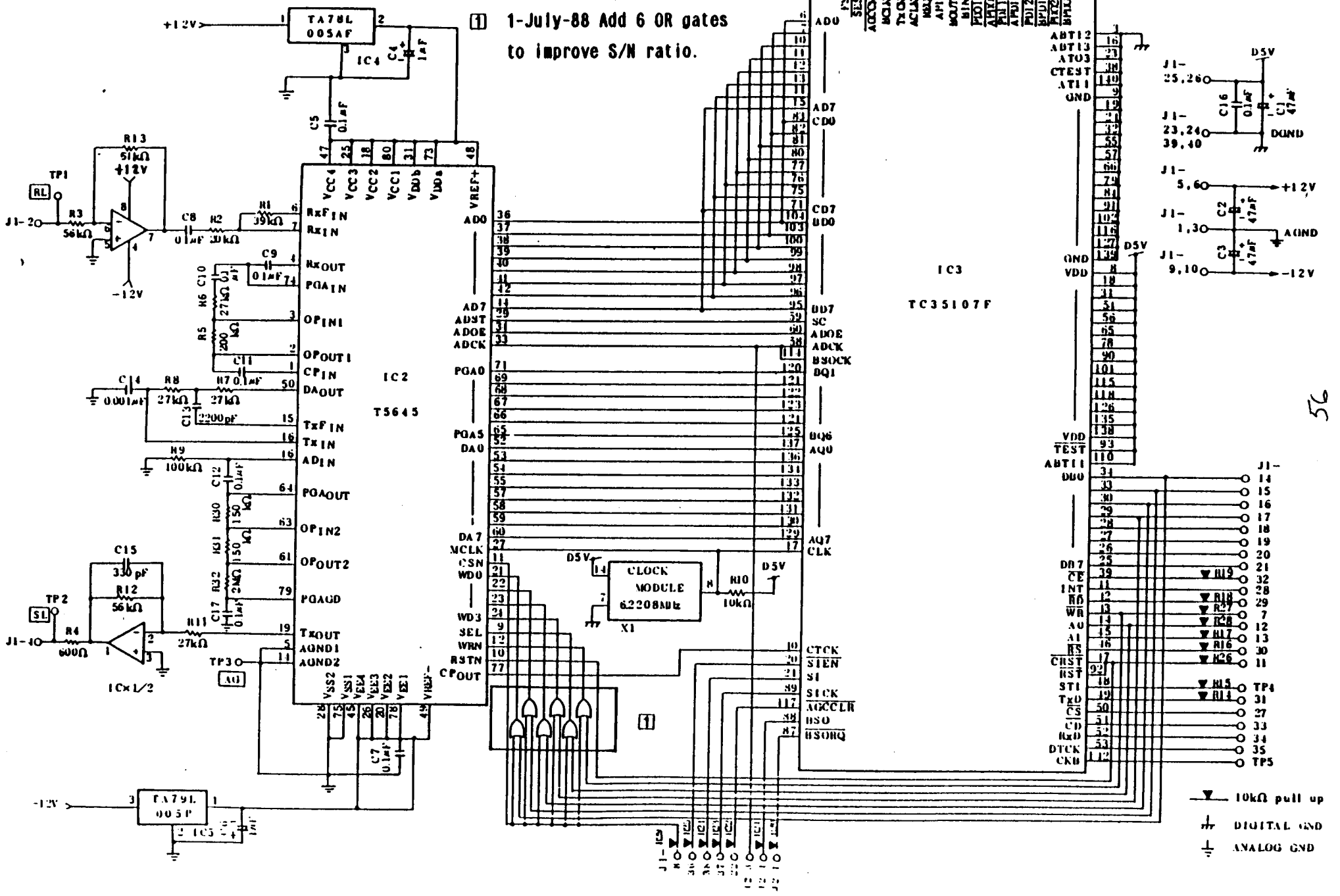
Serial Data Input Timing



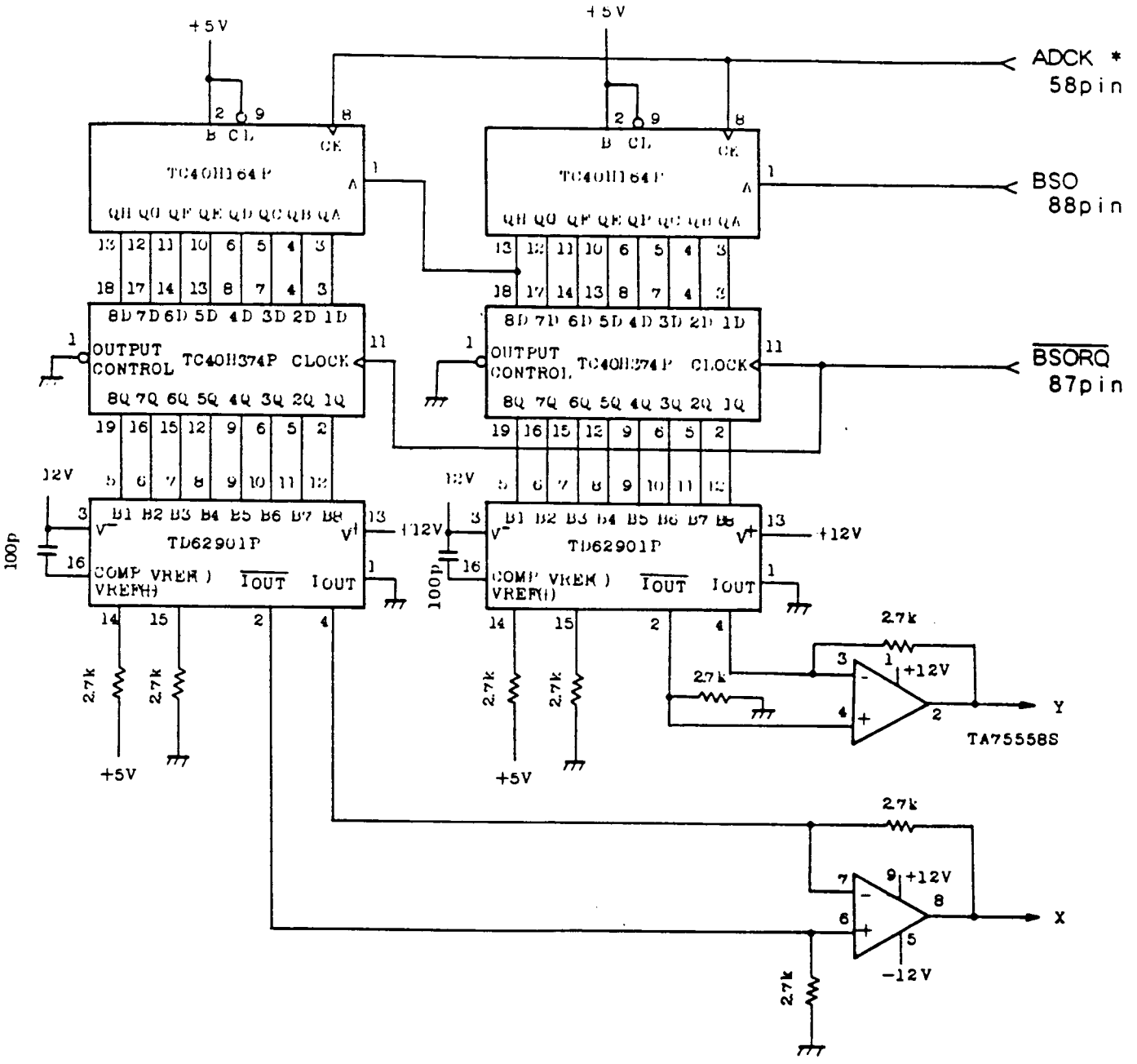
Serial Data Output Timing

11 INSTANCES OF THE CIRCUITS

11. 1 9600BPS FACSIMILE MODEM (1)



11. 3 EYE-PATTERN MONITOR

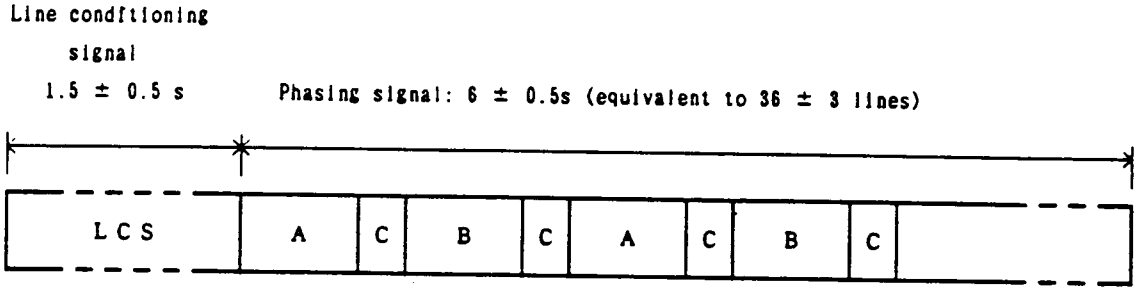


* ADCK(58pin) should be connected to BSOCK(114pin)

APPENDIX 1

TRANSMISSION OF GROUP II FACSIMILE PHASING SIGNAL

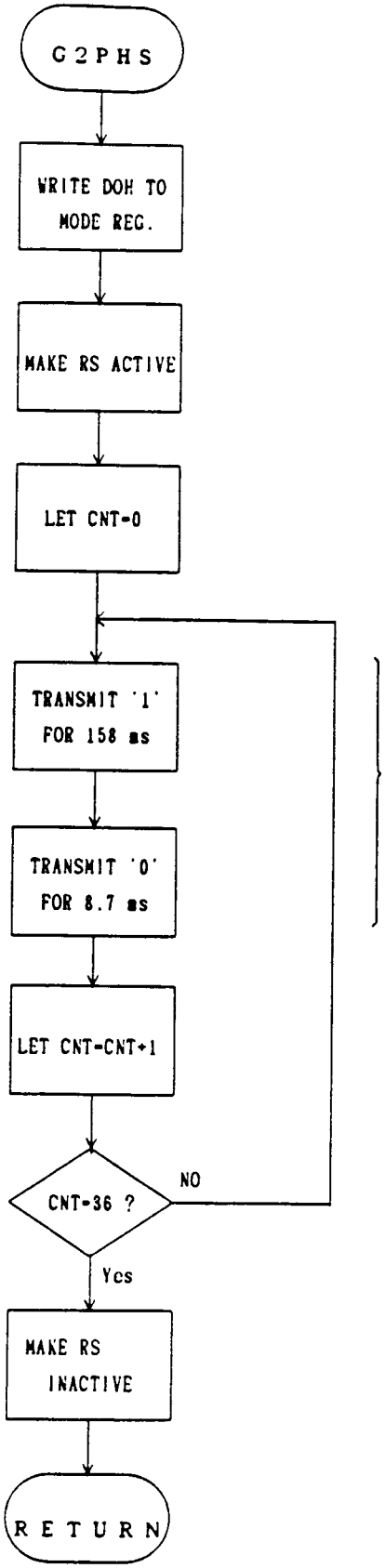
Group II facsimile phasing procedure is standardized in CCITT Recommendation T.3. The signaling scheme is shown below. An example of transmission control flow chart of this signal is described in next page.
For more details, refer to T.3.



L C S Line conditioning signal:1100 ± 50Hz. Transmission of this signal is optional
A Carrier in 0° phase for 94-96% of total scanning line length
B As A but may be in 180° phase
C No signal (at least 26 dB below the carrier) for the remaining 6-4% of TLL

Structure of line conditioning and phasing signal

G II PHASING SUBROUTINE (LCS is omitted)



SET G II MODE
REFER TO SETTING
PROCEDURE OF
OPERATION MODE

READY FOR TRANSMISSION

COUNTER CLEAR

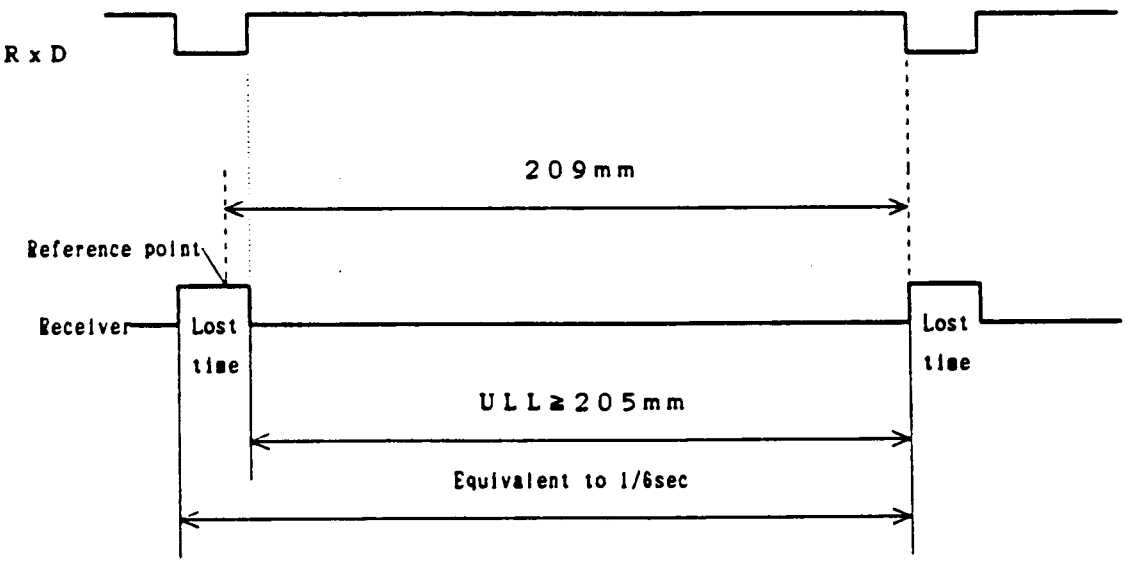
1/6 sec
EQUIVALENT TO
TOTAL SCANNING
LINE PERIOD

Note:
Carrier phase at '1' follows '0' is switched in 0° phase and 180° phase automatically.

APPENDIX 2

GROUP II FACSIMILE LINE SYNCHRONIZATION

Group II facsimile line synchronization can be performed in the reception term of phasing signal.
The start of the carrier indicates the end of the lost time. The receiver should adjust the reference point with an accuracy of 1% of TLL (Total scanning Line Length) to this start of the carrier that is, the rising edge of the RxD.
The reference point should be 209mm before the end of ULL (Usable scanning Line Length). For more details, refer to T.3 Recommendation.



APPENDIX 3

TIMING CHART OF THE STATUS BITS IN THE CASE OF NOISE-ON-TRAINING

At the reception mode of V.29 or V.27ter, the status bit of the modem status register indicates the conditions as follows.

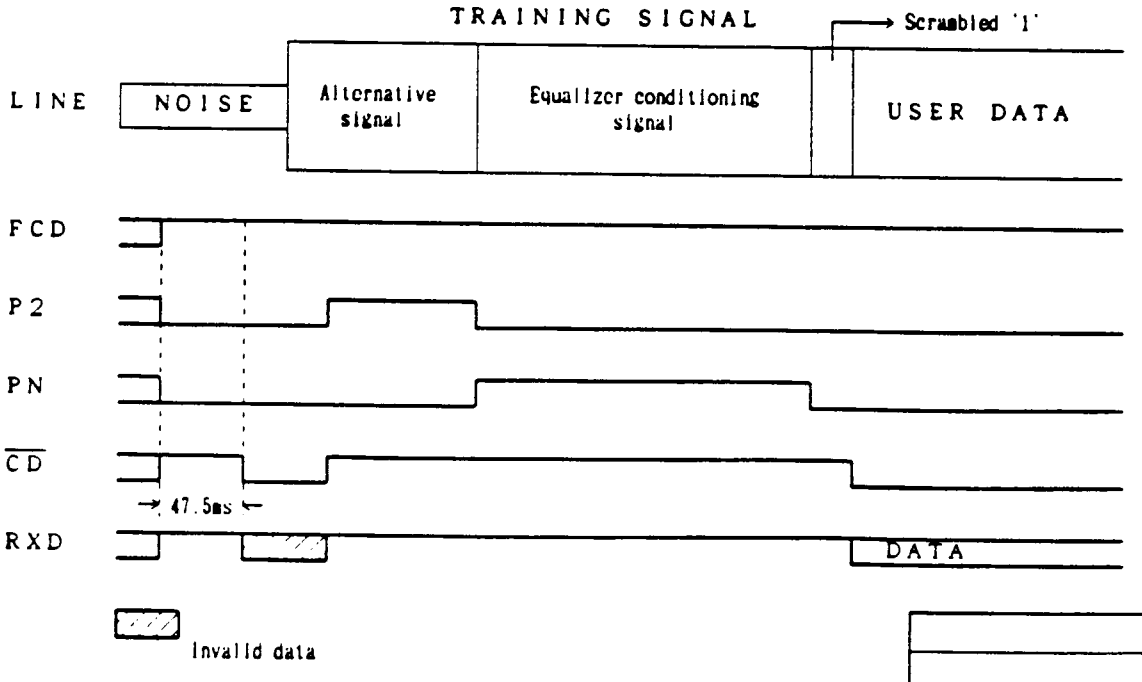
FCD (Fast Carrier Detect)
Signal processor TC35107F generates this signal using power detector. Therefore FCD goes active against any kind of the energy appears to the line.

$\overline{CD}$ (Carrier Detect)
It becomes active at the end of the training sequence of V.27 ter and V.29. The another case of $\overline{CD}$ becomes active is caused by the internal timer. In the case of non-detection of the training, internal timer makes $\overline{CD}$ active approximately 50 ms after rising of the FCD.

P2 (Alternative pattern detection)
This signal indicates the result of the alternative signal detection. The training sequence starts following such alternative signal.

PN (Pseudo random pattern)
This signal indicates the end of P2 sequence and equalizer conditioning period. P2 and PN present accurate response in the training sequence.

The training of the modem with noise beyond the FCD on threshold level is called Noise-on-Trainig. Therefore, the FCD becomes active even if the Rx line does not have signals.
Considering the circumstance mentioned above, timing chart of the status bit at Noise-on-Training is plotted as below.



APPENDIX 4

AGC Gain Data Register

The AGC gain data corresponds to the inverse proportion to the signal level at the line. Therefore, the data is effective of carrier detection the case of high level noise above -43dBm.
AGC gain step is equivalent to 0.75dB, 6bits of '0' means minimum gain and all '1' of 6bits means maximum gain to the amplifier. When the gain register indicates 00(hex-decimal), energy of 0dBm is appearing to the Rx terminal. The other case, at the maximum gain (3F hex-decimal) points out energy of -47.5dBm.

Example:

MSB	LSB	Signal level (ideal)
1 1 1 1 1	1	less than -47.5dBm
1 1 1 1 1	0	-46.75dBm
1 1 1 1 0	1	-46.0 dBm
1 1 1 1 0	0	-45.25dBm
0 0 0 0 1	1	-2.5 dBm
0 0 0 0 1	0	-1.75dBm
0 0 0 0 0	1	-1.0 dBm
0 0 0 0 0	0	greater than -0.25dBm

APPENDIX 5

IMPLEMENTATION OF T.30

The standardized facsimile procedure CCITT Recommendation T.30 says the negotiation method using V.21 (300bps FSK). After the negotiation, facsimile sends the information of the picture. Therefore, the trouble in the negotiation using V.21 may make impossible to receive the picture.

The case of the multi-page transmission, the negotiation will also be needed between pages. (Refer to the case A and case B represented latter.)

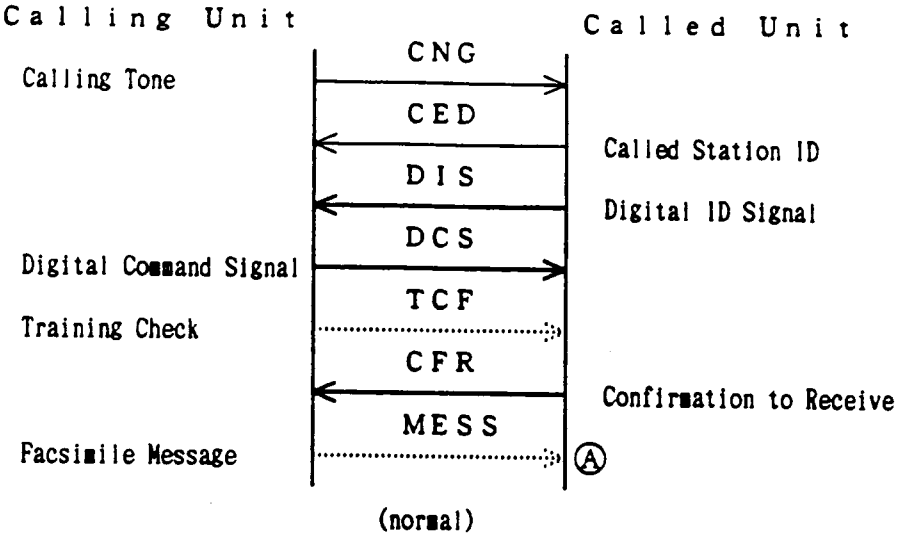
We propose the usage for solving these problems.

The binary data of V.21 based on HDLC format have flag sequence for 1sec prior to the information flame. Then, at first, the controller of the facsimile will observe High speed signals (V.27ter or V.29) for certain period. If the status bit of the P2 which indicates the training detection did not becomes high, change the operation mode to V.21 immediately. HDLC flag sequence has adequate time for changing the operation mode by microprocessor.

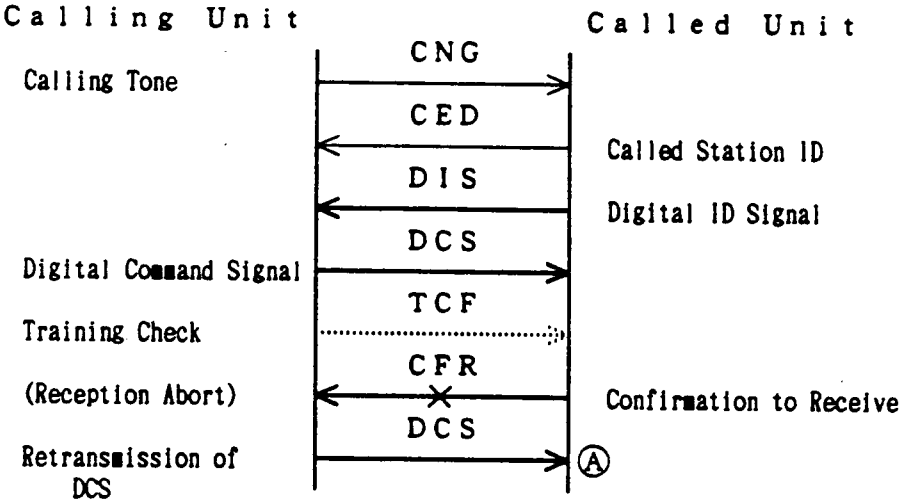
For more details, refer to CCITT Recommendations.

Group III Facsimile Procedure

Case A:



(normal)

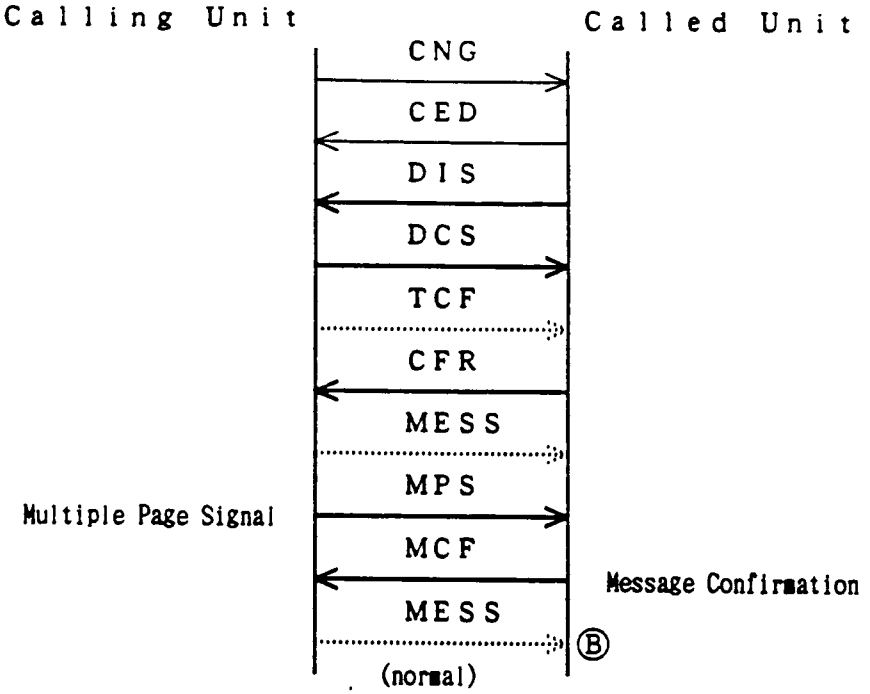


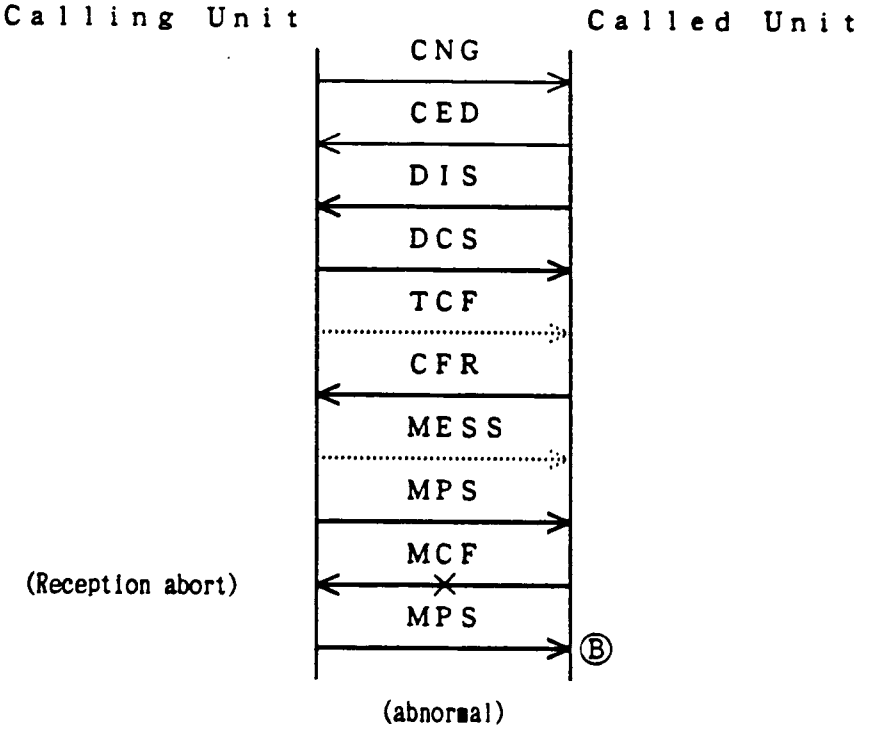
(abnormal)

At Ⓐ Called Unit has to observe the High speed and Low speed (V.21) messages at the same time because of the case described above.

(arrows)
→ TONE
⟶ 300bps FSK (V.21)
⇢ HIGH SPEED DATA (V.27 ter. V.29)

Case B:



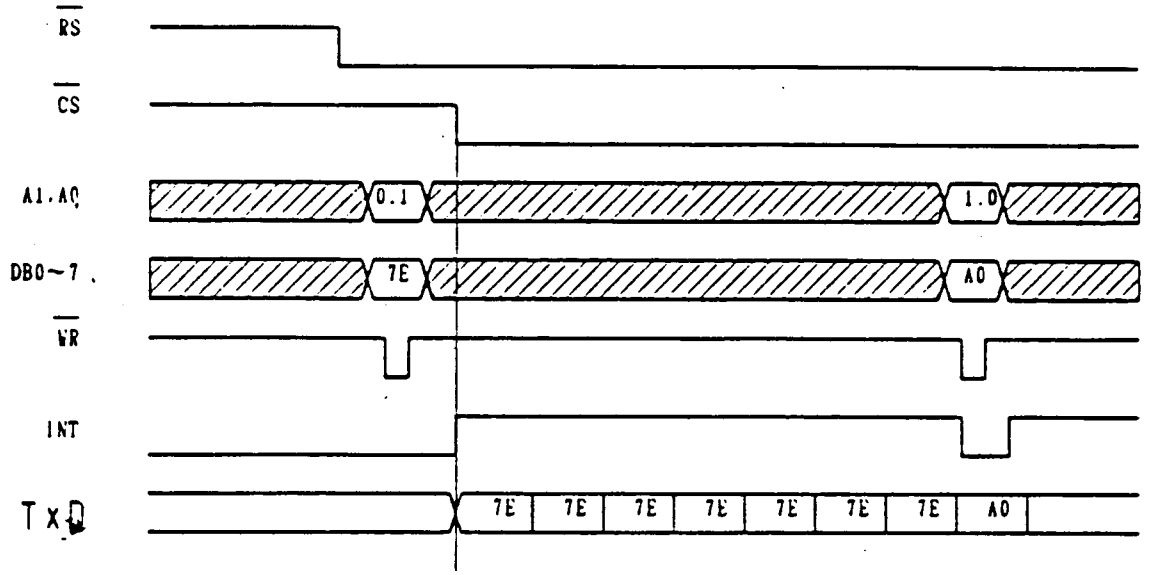


At Ⓑ similer problem as case A is concerned.

APPENDIX 6

FLAG TRANSMISSION

Transmitting at parallel mode, Interrupt request appears in every 8bit data transfer. In transmission, for example 00H data, the flag of HDLC 7EH data at this parallel mode, it makes microcomputer process easier. See consecutive frag as follows :



After setting the transmission data(A0=1,A0=0), if the INT which appears every 8bit data transfer is ignored and host processor writes no consecutive transmission data, the modem continuously transmit previous setting data. (By setting it again, the other data will be transmtted.)
Set the first transmission data before CS becomes a "0".

9600bps MODEM BOARD MANUAL

(T96FX-A1 ··· TC35107F & T5645)

TOSHIBA CORPORATION

INTRODUCTION

The T96FX-XX is a 9600bps modem card designed for facsimile equipment.

This modem card satisfies CCITT Recommendations V. 29, V. 27ter, V21 (ch2), T. 30, T. 4 and T. 3.

By small size and low power consumption, the T96FX-XX effectively realizes Modem part required in GIII Facsimile machines.

FEATURES

- GIII CCITT V. 29, V. 27ter
- GII CCITT NTT (JAPAN) mini-fax mode
- GI CCITT NTT (JAPAN) VF mode
  FSK mode (only transmission)
- T. 30 V. 21 (ch2)
  Tone Generation Tonal Procedure
- DTMF Generation and Detection for various tones (Programmable)
- Changeable Detect level (3 ways)
- DTE Interface Parallel/Serial
  CCITT V. 24 (RS-232-C)
- Attuator for transmission (0~-15dB)
- Cable Equalizer for transmission and reception (0, 4, 8, 12dB)
- Power supply +5V, ±12V
- Low Power Consumption (1 watt typical)

Communication method

- V.29 (QAM) — 9600bps, 7200bps, 4800bps (2400baud) Echo protect
- V.27ter (PSK) — 4800bps (1600baud), 2400bps (1200baud) Echo protect, Short/Long Trainning
- V21 ch2 (FSK) — 300bps for Binary Procedure
- GII — AM·PM·VSB
- GI — FM
- Half-Duplex (2-WIRE)

Transmit Level

- +5 ~ -10 dBm ±1dBm

Receive Level (3 ways)

- 0~-43 dBm (off level : -48dBm)
- 0~-26 dBm (off level : -31dBm)
- 0~-16 dBm (off level : -21dBm)

Operating Current

- 5V : typ 65mA
- 12V : typ 25mA
- -12V : typ-25mA

GENERAL SPECIFICATION

POWER

	Min	typ	Max	unit	Current(Ta=25 ℃)
+5V	4.75		5.25	V	typ 65mA
+12V	11.75		12.25	V	typ 25mA
-12V	-12.25		-11.75	V	typ-25mA

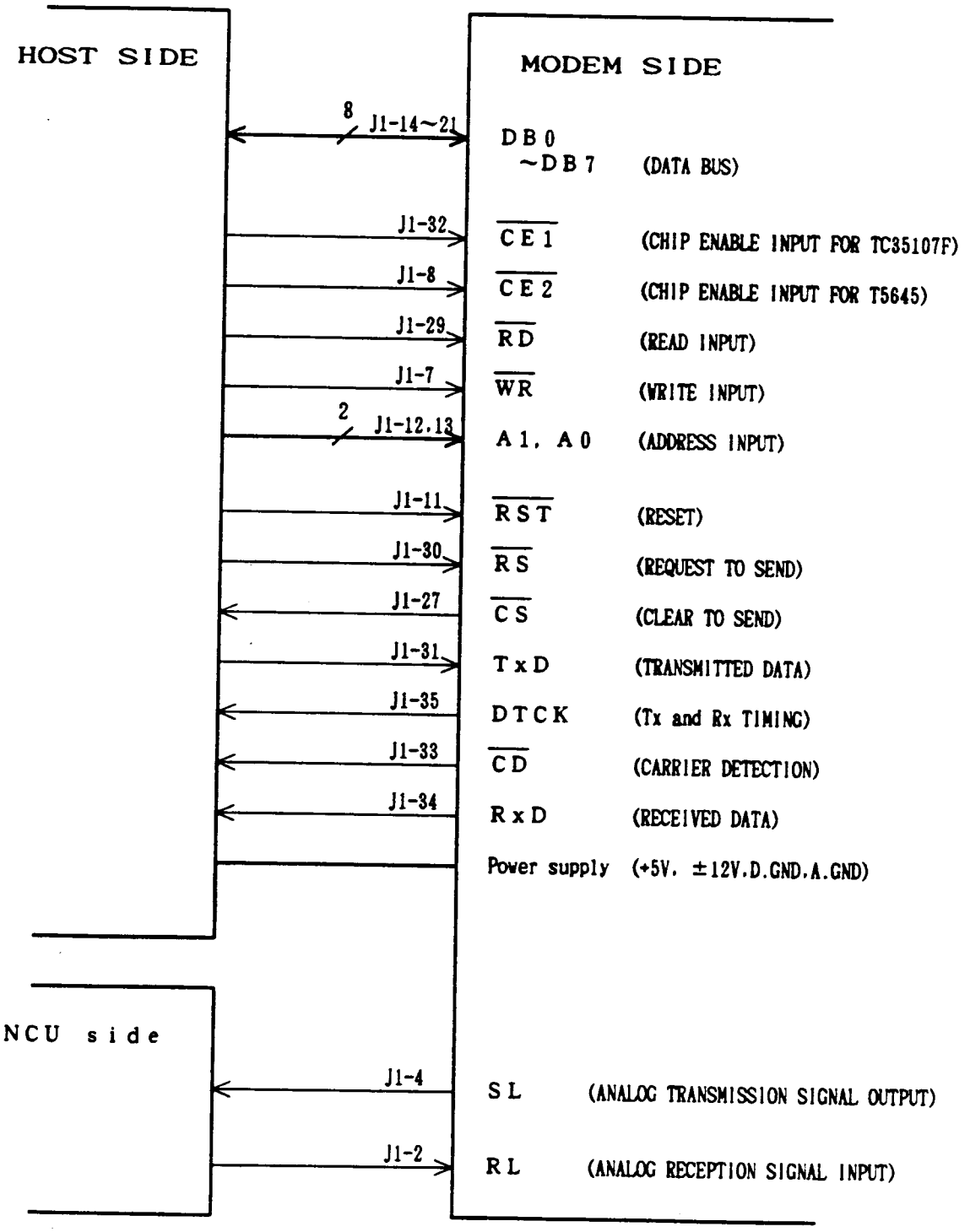
ENVIRONMENTAL

Operation Temperature	0 ~ 60 ℃
Storage Temperature	-20 ~ 80 ℃
Relative Humidity	up to 90% (noncondensing)

MECHANICAL

Length	60 mm
Width	85 mm
Heith	10 mm
Weight	100 g

9600bps CARD MODEM INTERFACE (T96FX-A1)



9600bps MODEM BOARD INTERFACE (T96FX-A1)

PIN NO.	I/O	NAME	PIN NO.	I/O	NAME
J1-1	-	A. GND	J1-21	I/O	DB7 (TC35107F 25pin)
2	I	RL	22	I	AGCCLR (TC35107F 117pin)
3	-	A. GND	23	-	D. GND
4	O	SL	24	-	D. GND
5	-	+12V	25	-	+5V
6	-	+12V	26	-	+5V
7	I	$\overline{WR}$ (TC35107F 43pin)	27	O	$\overline{CS}$ (TC35107F 50pin)
8	I	$\overline{CE2}$ (T5645 11pin)	28	O	INT (TC35107F 41pin)
9	-	-12V	29	I	$\overline{RD}$ (TC35107F 42pin)
10	-	-12V	30	I	$\overline{RS}$ (TC35107F 46pin)
11	I	$\overline{RST}$ (TC35107F 92pin)	31	I	TxD (TC35107F 49pin)
12	I	A0 (SEL) (TC35107F 44pin)	32	I	$\overline{CE1}$ (TC35107F 39pin)
13	I	A1 (TC35107F 45pin)	33	O	$\overline{CD}$ (TC35107F 51pin)
14	I/O	DB0 (TC35107F 34pin)	34	O	RxD (TC35107F 52pin)
15	I/O	DB1 (TC35107F 33pin)	35	O	DTCK (TC35107F 53pin)
16	I/O	DB2 (TC35107F 30pin)	36	I	$\overline{SIEN}$ (TC35107F 20pin)
17	I/O	DB3 (TC35107F 29pin)	37	I	SICK (TC35107F 89pin)
18	I/O	DB4 (TC35107F 28pin)	38	I	SI (TC35107F 21pin)
19	I/O	DB5 (TC35107F 27pin)	39	-	D. GND
20	I/O	DB6 (TC35107F 26pin)	40	-	D. GND

CONNECTOR PIN NAME	INPUT/ OUTPUT	PIN No.	Description
DB0 (LSB) DB1 DB2 DB3 DB4 DB5 DB6 DB7 (MSB)	I/O	14 15 16 17 18 19 20 21	Data Bus (8bits) Only DB0 TO DB3 are available for analog front-end LSI TC35102F.
$\overline{CE2}$	I	8	Chip enable for analog front-end LSI T5645 (active low)
$\overline{CE1}$	I	32	Chip enable for modem signal processor TC35107F (active low)
$\overline{WR}$ *	I	7	Write Enable (active low)
$\overline{RD}$ *	I	29	Read Enable (active low)
A0 * A1 *	I	12 13	Address lines for register selection Only A0 is available for TC35102F For more details, refer to Technical Data
$\overline{RS}$ *	I	30	Request to Send (active low)
$\overline{CS}$	O	27	Clear to Send (active low)
$\overline{CD}$	O	33	Carrier Detect (active low) This signal indicates the valid data ready. As usual, it goes active at the end of GIII training.
TXD *	I	31	Transmission data input
RXD	O	34	Reception data output (MARK is high)
DTCK	O	35	Transmission/Reception synchronous clock Data should be input/output at the rising/falling edge

CONNECTOR PIN NAME	INPUT/ output	PIN No.	Description
$\overline{RST}$ *	I	11	Modem hardware reset
INT	O	28	Interrupt request signal (active high) This signal avails at the parallel data handling mode. TC35107F generates interrupt request at when data to be transmitted is required and when received data is ready in internal buffer. This terminal goes to high level when the interrupt factor has occured. INT may be used as hand shake signal between the host-processor and the modem.
$\overline{AGCCLR}$ *	I	22	AGC clear input When this terminal is set to low. AGC gain is fixed at the minimum value.
SI $\overline{SIEN}$ SICK	I I I	38 36 37	Serial data input and control terminals These are available at the coefficients writing into TC35107F.
RL	I	2	Reception analog line terminal
SL	O	4	Transmission analog line terminal
+12V	I	5 6	+12 volt power supply
-12V	I	9 10	-12 volt power supply
+5V	I	25,26	+5 volt power supply
A. GND	I	1 3	Analog Ground
D. GND	I	23,24 39,40	Digital Ground

NOTE:

The terminals marked (*) are connected to +5 volt supply through 10K ohm resistors.
Data Bus (DB0 to DB7) is also connected to +5 volt supply through 30K ohm resistor.

EYE-PATTERN INTERFACE (T96FX-A1) (OPTION)

PIN NO.	NAME	DESCRIPTION
J2-1	T S*	EYE-PATTERN DATA WORD SYNCHRONOUS CLOCK OUTPUT
2	A. GND	ANALOG GND
3	EYECK*	EYE-PATTERN DATA BIT SYNCHRONOUS CLOCK
4	E Y E*	SERIAL DATA OUTPUT FOR MONITORING EYE-PATTERN
5	D. GND	DIGITAL GND
6	+ 5 V	+5V POWER SUPPLY
7	+12V	+12V POWER SUPPIY
8	-12V	-12V POWER SUPPLY

*. USING THESE SIGNALS,MONITORING EYE-PATTERN(OPTION) IS PERFORMED . REFER TO THE APPLICATION CIRCUIT.

T96FX-A1 BOARD TEST PIN

PIN NO.	NAME	DESCRIPTION
TP 1	R L	RECEPTION ANALOG LINE TERMINAL
TP 2	S L	TRANSMISSION ANALOG LINE TERMINAL
TP 3	A. GND	ANALOG GND
TP 4	ST 1	EXTERNAL TRANSMISSION TIMING INPUT
TP 5	CKB	BAUD RATE SYNCHRONOUS CLOCK OUTOUT

PARTS LIST (T96FX-A1)

I C	
IC1	TA75558F
IC2	T5645
IC3	TC35107F
IC4	TA78L005AF
IC5	TA79L005P

CAPACITOR	
C 1	**47μF
C 2	**47μF
C 3	**47μF
C 4	*1μF
C 5	0.1μF
C 6	*1μF
C 7	0.1μF
≀	≀
C12	0.1μF
C13	0.0022μF
C14	0.001μF
C15	330PF
C16	0.1μF
C17	0.1μF

*: TANTALUM

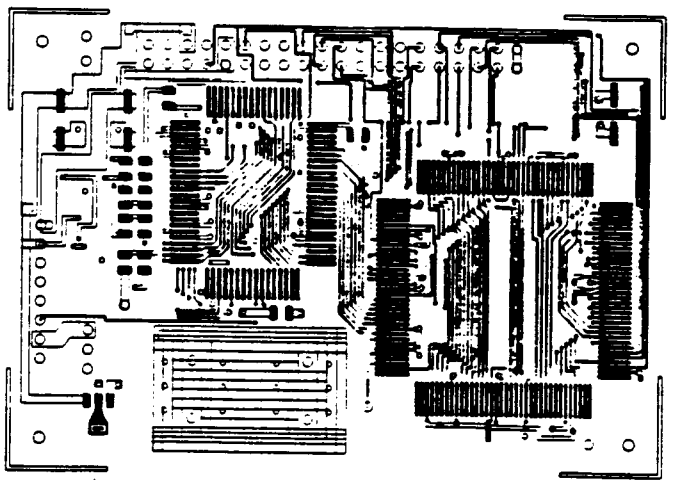
**: CHEMICAL

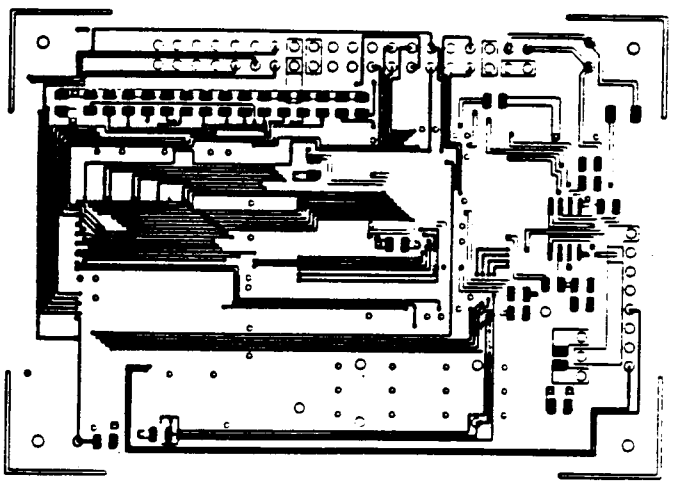
RESISTOR	
R 1	39KΩ
R 2	20KΩ
R 3	56KΩ
R 4	600Ω
R 5	200KΩ
R 6	27KΩ
R 7	27KΩ
R 8	27KΩ
R 9	100KΩ
R10	10KΩ
R11	27KΩ
R12	56KΩ
R13	51KΩ
R14	10KΩ
≀	≀ (For Pull up)
R29	10KΩ
R30	150KΩ
R31	150KΩ
R32	2MΩ

CLOCK MODULE	
X 1	6.2208MHZ

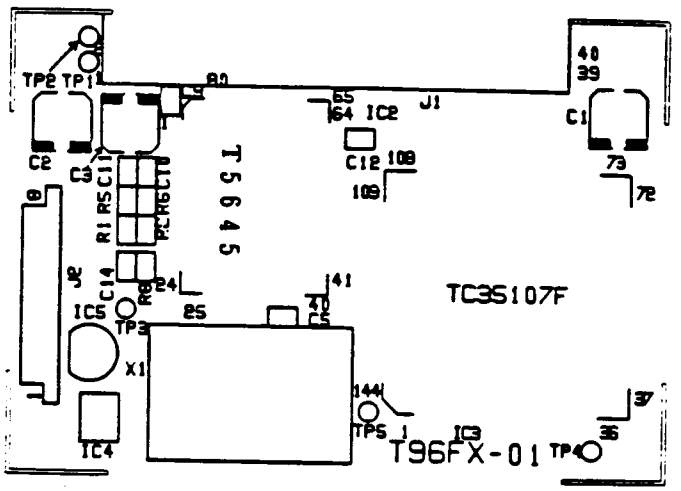
9600bps MODEM BOARD (T96FX-A1)

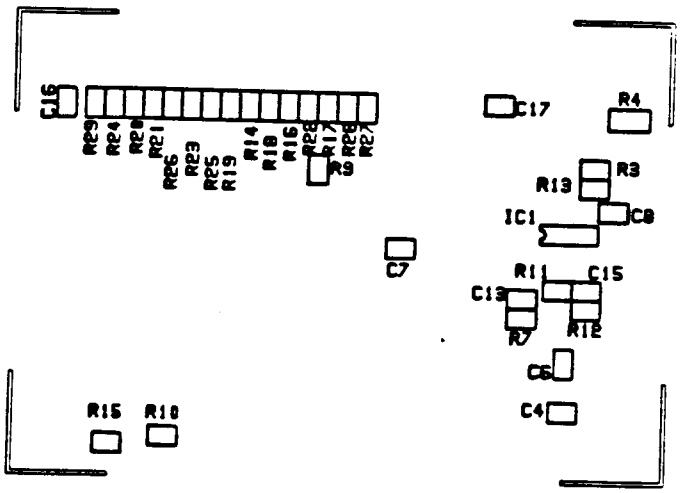
(SIZE 85 ×60 mm)



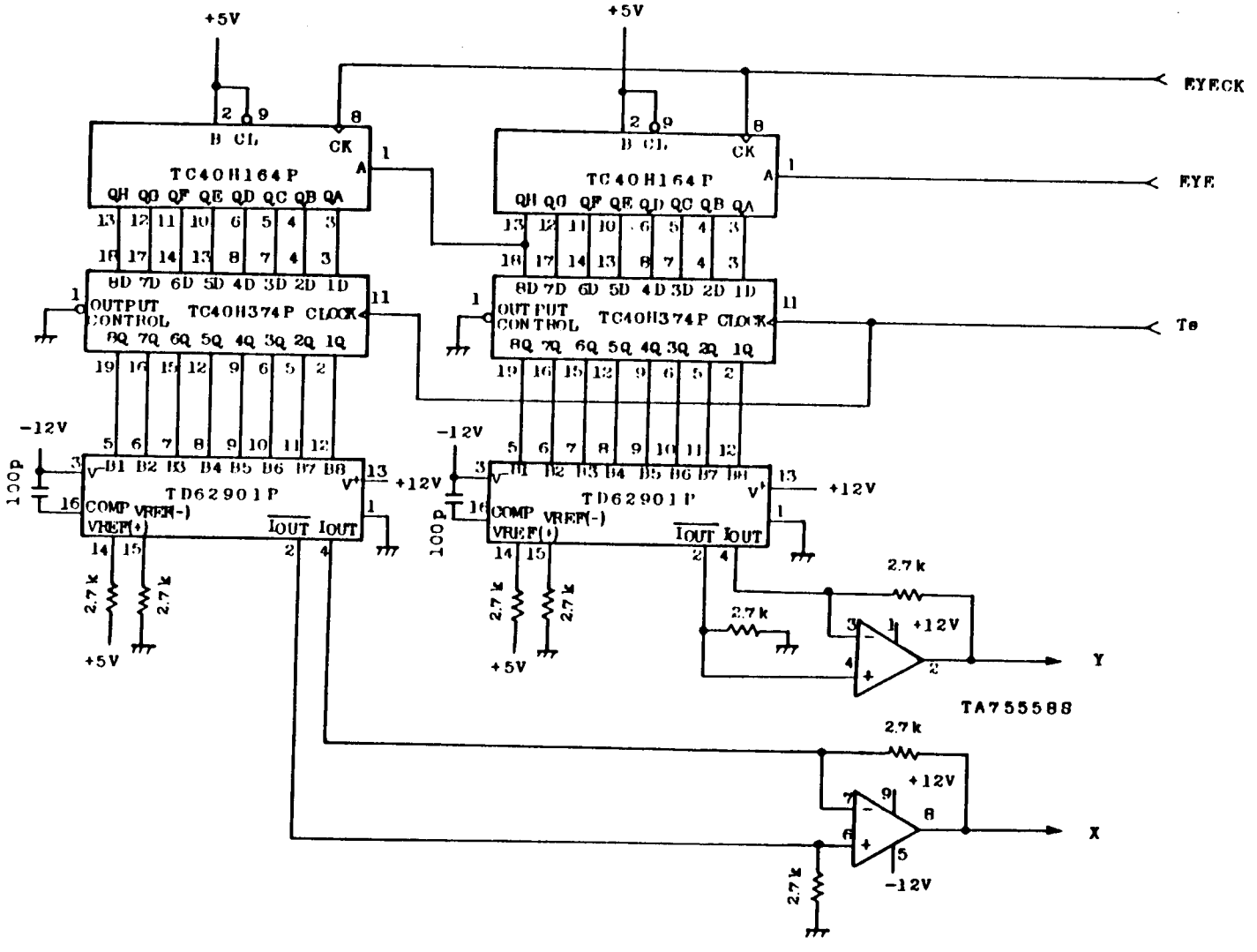


(T96FX-A1)

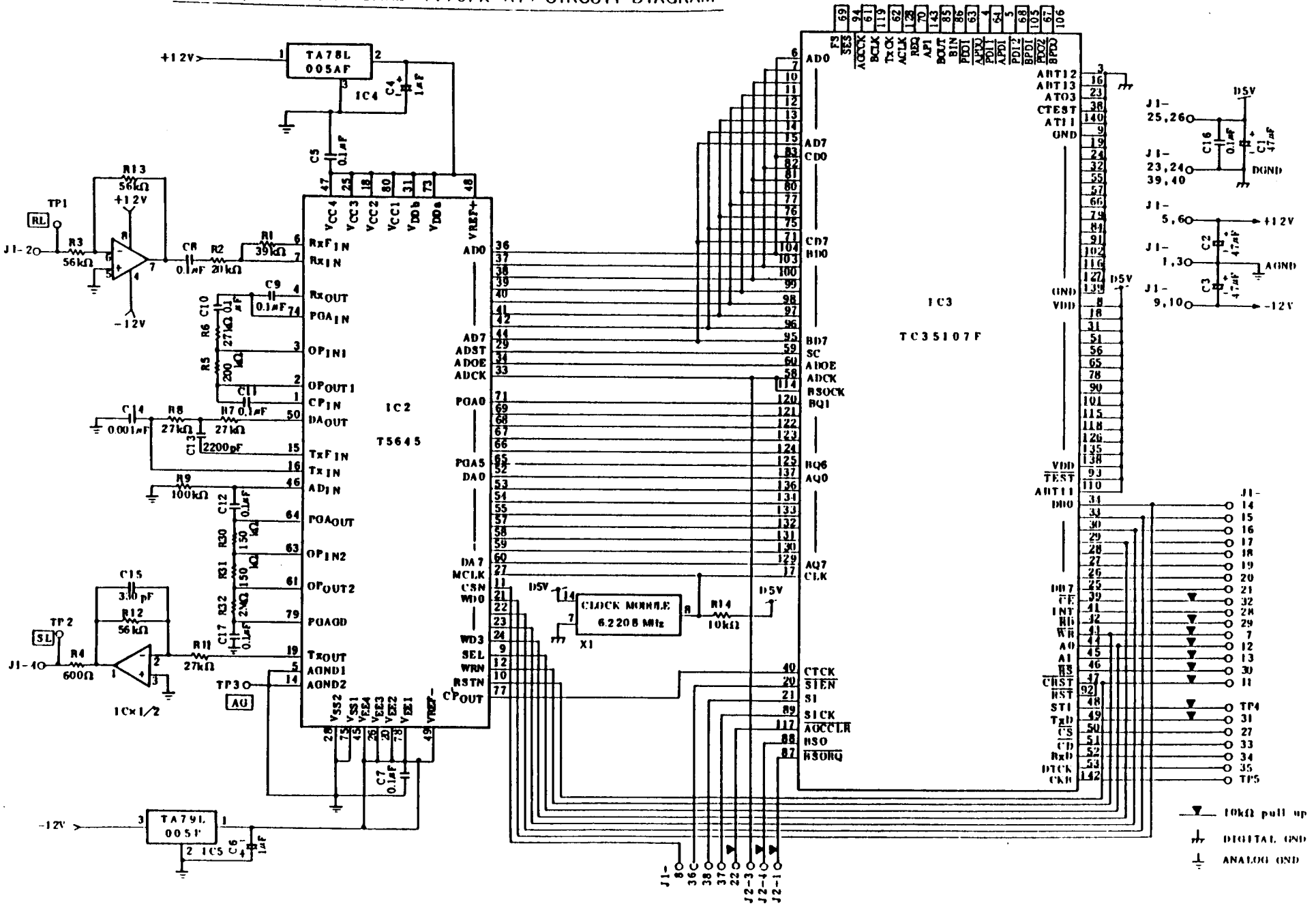

TP2
TP1
C2
C3
C11
R1
R5
C14
R8
R24
IC5
TP3
X1
IC4
T5645
J2
J1
IC2
C12
C1
40
39
73
72
109
64
65
41
42
25
144
TP5
1
IC3
37
36
TP4
TC35107F
T96FX-01


C16
R29
R24
R28
R21
R26
R23
R25
R19
R14
R18
R16
R22
R17
R9
R20
R27
C17
R4
R13
R3
IC1
C8
C7
R1
C15
C13
R7
R12
C6
C4
R15
R10

EYE PATTERN MONITOR CIRCUIT (T96FX-A1)



9600 bps MODEM BOARD (T96FX-A1) CIRCUIT DIAGRAM



9600 bps MODEM BOARD (T96FX-A2) CIRCUIT DIAGRAM