TC35661SBG-009 Bluetooth® HCI IC Rev 1.01

Contents

1. General Description

1.1. Product Concept

TC35661SBG-009 is a 1-chip CMOS IC for Bluetooth® communication, which includes an RF analog part and a Baseband digital part. TC35661 provides Bluetooth® HCI (Host Control Interface) function specified in Bluetooth® Core Specifications, EDR function, and LE (Low Energy) function. Bluetooth® application is easily realized when TC35661 is connected to an external host processor and Bluetooth® profile/stack and signal procedure are executed.

1.2. Features

- Compliant with Bluetooth® Ver4.2
  - Built-in Bluetooth® baseband digital core
  - Built-in Bluetooth® RF analog core
  - Built-in PLL for multi-clock input
  - Built-in ARM7TDMI-S™ core
  - On-chip Program Mask-ROM for Bluetooth® communication
  - On-chip Work memory (RAM) for Bluetooth® Baseband procedure
  - Supports patch program loader function
- Supports a CODEC for audio communication
  - CVSD (Continuous Variable Slope Delta Modulation) CODEC
  - PCM (Pulse Code Modulation) CODEC
  - mSBC for WBS (Wide Band Speech)
- Connectable Serial Flash ROM/ EEPROM at external serial memory interface
  - Serial Flash ROM interface (SPI)
  - EEPROM interface (I^2C/SPI)
- Host Interface (set for the product test.)
  - UART interface: Baud rate from 2400 bps to 4.33 Mbps
- Voice/Audio CODEC Digital Interface (1-ch)
  - Supports I^2S (The Inter-IC Sound Bus) interface
  - Left-justified interface
  - Supports PCM (Pulse Code Modulation) digital interface
- General Purpose I/O (GPIO) with pull-up and pull-down resistors (MAX: 19 ports)
- Wake-up Interface
  - Wake-up input function and remote wake-up output function
- Wi-Fi co-existence interface (2-wire, 3-wire and 4-wire)
- Test Interface
  - JTAG Interface (ICE Interface)
- Supports OSC (Crystal oscillator: 26 MHz)
  - Supports an external clock input
  - Built-in oscillation circuit for an external crystal oscillator
- Supports a sleep clock
  - Built-in divider for the reference operation clock
  - Supports an external clock input
- Built-in sleep function
- Power Supply: Single 1.8 or 3.3 V
- Package
  - P-TFBGA64-0505-0.50 [64 balls, 5x5 mm, 0.5 mm pitch, and 1.2 mm height]

2. Pin Function

2.1. Pin Assignment

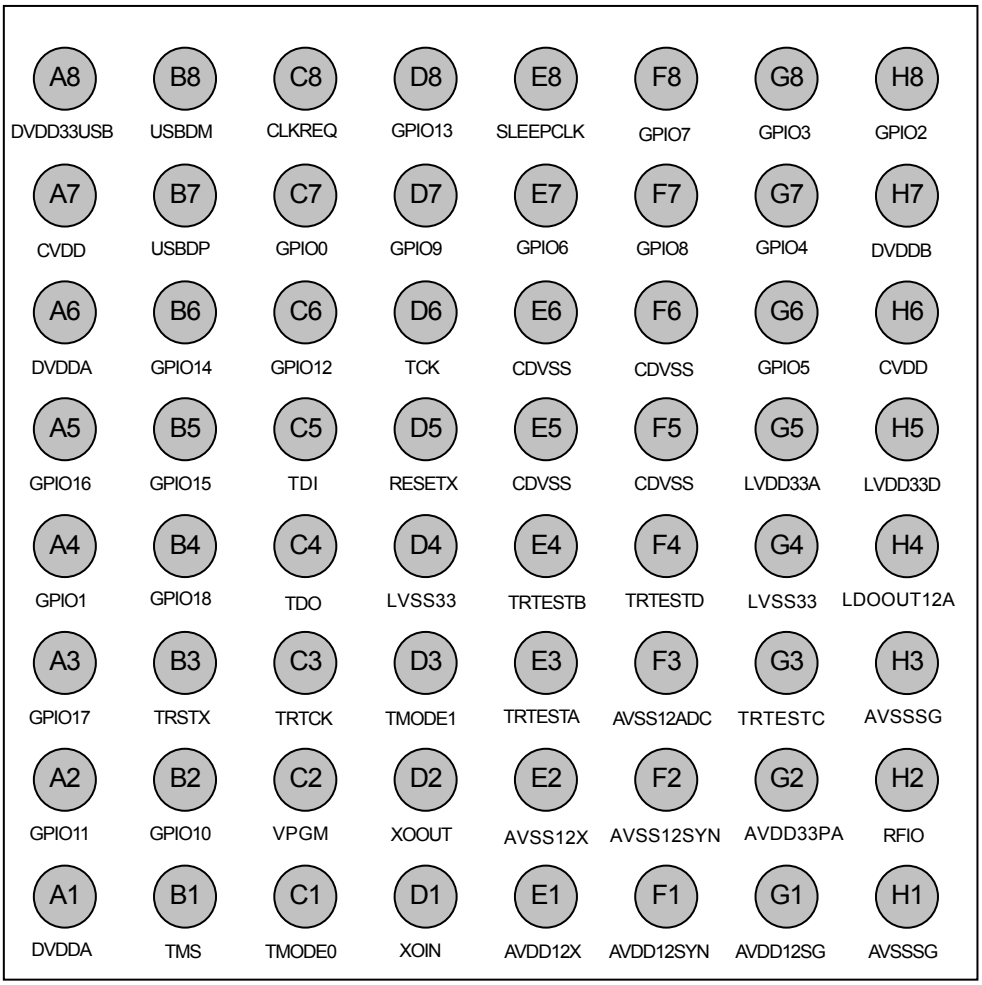

Figure 2-1 Pin Assignment (Top view)

2.2. Pin Functions

Table 2-1 shows an attribute of each pin, input or output state at operation, and function of each pin.

The power supply pins are shown in Table 2-2.

Table 2-1 Pin Functions

Pin name	Pin No.	Attribute VDD category Direction Type	Condition During BT communication During a reset After a reset release	Functional description
Reset interface				
RESETX	D5	DVDDA IN Schmitt trigger	IN IN IN	Hardware reset input pin Low level indicates the reset.
Clock interface				
XOIN	D1	AVDD12X IN OSC	IN IN IN	Reference clock input pin Crystal oscillator or TCXO input pin. The clock frequency is 26 MHz. The clock frequency uncertainty should be +/- 20 ppm or less. A feedback resistor is built in between XOIN pin and XOOUT pin. A resistor and a capacitor suitable for the used crystal oscillator should be externally connected. The clock is used as the internal reference clock.
XOOUT	D2	AVDD12X OUT OSC	OUT OUT OUT	Reference clock feedback output pin Crystal oscillator output pin. A feedback resistor is built in between XOIN pin and XOOUT pin. A resistor and a capacitor suitable for the used crystal oscillator should be externally connected. The clock is used as the internal reference clock. If using TCXO for a reference clock, this pin needs to be kept open.
CLKREQ	C8	DVDDA OUT 2 mA	OUT OUT OUT	Reference clock (26 MHz) request pin Reference clock request signal. By using this signal to control ON/OFF of an external clock, lower power consumption of the hardware system is achieved. A high level indicates a request for the clock supply. If SLEEPCLK is not used and only X'tal is used, or during a reset, this pin always outputs High. When the clock supply is not necessary, this pin outputs Low. When not using this pin, this pin needs to be kept open.
SLEEPCLK	E8	DVDDA IN Schmitt trigger	IN IN IN	Sleep clock input pin This pin is a clock input for low power consumption operation. The clock frequency should be 32.768 kHz. Frequency uncertainty of the sleep clock should be less than or equal to +/-250 ppm. When not using this pin, this pin needs to be pulled down by 100 kΩ.

Pin name	Pin No.	Attribute VDD category Direction Type	Condition During BT communication During a reset After a reset release	Functional description
RF interface				
RFIO	H2	AVDD12SG IN/OUT Analog	IN/OUT GND GND	RF I/O pin Chapter 6 shows the external connection example of the circuit which matches this pin to 50 Ω. Refer to the connection example, confirm operations in customer's environment, and adjust the components constant. The pattern before and behind the matching circuit should wire with the 50 Ω transmission line as much as possible, and should not interfere with the power supply line. Don't connect DC voltage directly to this pin.
General purpose I/O port				
GPIO0	C7	DVDDA IN/OUT Pull-up/ Pull-down Schmitt trigger 1, 2, and 4 mA	IN/OUT No-pull-up No-pull-up	General purpose I/O pin 0 During a reset GPIO0 is set as an input whose built-in pull-up resistor is disabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. When not using this pin, this pin needs to be pulled down by 100 kΩ.
GPIO1	A4	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 1 During a reset GPIO1 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. When not using this pin, this pin needs to be kept open.
GPIO2	H8	DVDDB IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 2 During a reset GPIO2 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to PCMOUT pin of PCM codec interface. When not using this pin, this pin needs to be kept open.
GPIO3	G8	DVDDB IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 3 During a reset GPIO3 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to PCMIN pin of PCM codec interface. When not using this pin, this pin needs to be kept open.

Pin name	Pin No.	Attribute	Condition	Functional description
		VDD category Direction Type	During BT communication During a reset After a reset release	
GPIO4	G7	DVDDB IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 4 During a reset GPIO4 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to PCMCLK pin of PCM codec interface. When not using this pin, this pin needs to be kept open.
GPIO5	G6	DVDDB IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 5 During a reset GPIO5 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to FSYNC pin of PCM codec interface. When not using this pin, this pin needs to be kept open.
GPIO6	E7	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 6 During a reset GPIO6 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin is switched to UART-TX pin in Host CPU interface. When not using this pin, this pin needs to be kept open.
GPIO7	F8	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 7 During a reset GPIO7 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin is switched to UART-RX pin in Host CPU interface. When not using this pin, this pin needs to be kept open.
GPIO8	F7	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 8 During a reset GPIO8 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin is switched to UART-RTSX (Request to send) pin in Host CPU interface. When not using this pin, this pin needs to be kept open.
GPIO9	D7	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 9 During a reset GPIO9 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin is switched to UART-CTSX (Clear to send) pin in Host CPU interface. When not using this pin, this pin needs to be kept open.

Pin name	Pin No.	Attribute VDD category Direction Type	Condition During BT communication During a reset After a reset release	Functional description
GPIO10	B2	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 10 During a reset GPIO10 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to BtActivity signal pin of Wi-Fi device coexistence interface. When not using this pin, this pin needs to be kept open.
GPIO11	A2	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 11 During a reset GPIO11 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to BtState signal pin of Wi-Fi device coexistence interface. When not using this pin, this pin needs to be kept open.
GPIO12	C6	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 12 During a reset GPIO12 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to WiActivity signal pin of Wi-Fi device coexistence interface. When not using this pin, this pin needs to be kept open.
GPIO13	D8	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 13 During a reset GPIO13 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to BtInband signal pin of Wi-Fi device coexistence interface. When not using this pin, this pin needs to be kept open.

Pin name	Pin No.	Attribute	Condition	Functional description
		VDD category Direction Type	During BT communication During a reset After a reset release	
GPIO14	B6	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 14 During a reset GPIO14 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to SCL signal pin of the serial memory interface. I^2C and SPI are selectable as the serial memory interface. When not using this pin, this pin needs to be kept open.
GPIO15	B5	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 15 During a reset GPIO15 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to SDA/DOUT signal pin of the serial memory interface. I^2C and SPI are selectable as the serial memory interface. When not using this pin, this pin needs to be kept open.
GPIO16	A5	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 16 During a reset GPIO16 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to DIN signal pin of the serial memory interface. I^2C and SPI are selectable as the serial memory interface. When not using this pin, this pin needs to be kept open.
GPIO17	A3	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 17 During a reset GPIO17 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to CS0X signal pin of the serial memory interface. I^2C and SPI are selectable as the serial memory interface. When not using this pin, this pin needs to be kept open.

Pin name	Pin No.	Attribute VDD category Direction Type	Condition During BT communication During a reset After a reset release	Functional description
GPIO18	B4	DVDDA IN/OUT Pull-up/ Pull-down Schmitt 1, 2, and 4 mA	IN/OUT Pull-up Pull-up	General Purpose I/O pin 18 During a reset GPIO18 is set as an input whose built-in pull-up resistor is enabled. After the reset release, the data direction and the built-in pull-up resistor are set by using the internal software. After the pin configuration set by the internal software, this pin can operate as a general-purpose input and output pin. By the configuration after the boot, this pin is switched to CS1X signal pin of the serial memory interface. I^2C and SPI are selectable as the serial memory interface. When not using this pin, this pin needs to be kept open.
IC test interface				
TMODE0 TMODE1	C1 D3	DVDDA IN Schmitt trigger	IN IN IN	Test mode setting pins These pins are used to test a product in Toshiba. TMODE0 and TMODE1 pins need to be connected to GND.
TRTESTA TRTESTB TRTESTC TRTESTD	E3 E4 G3 F4	LVDD33A IN/OUT Analog	IN IN IN	Analog test pins These pins are used for analog inputs or outputs at the test of a product. These pins are used to test a product in Toshiba. TRTESTA, TRTESTB, TRTESTC and TRTESTD pins have to be connected to GND.
USBDP	B7	DVDD33USB IN/OUT Differential	IN/OUT Hi-Z Hi-Z	Test pin This pin has to be connected to GND.
USBDM	B8	DVDD33USB IN/OUT Differential	IN/OUT Hi-Z Hi-Z	Test pin This pin has to be connected to GND.

Pin name	Pin No.	Attribute VDD category Direction Type	Condition During BT communication During a reset After a reset release	Functional description
JTAG interface				
TRSTX	B3	DVDDA IN Schmitt trigger	Pull-down Pull-down Pull-down	JTAG reset input pin This pin is a reset input for test or debugging. During a reset the TRSTX is set as an input whose built-in pull-down resistor is enabled. Low level indicates JTAG reset. High level indicates JTAG operation. This pin needs to be kept open (not connected) or to be pulled down if not used for JTAG.
TCK	D6	DVDDA IN Schmitt trigger	Pull-up Pull-up Pull-up	JTAG clock input pin This pin is a clock input for test or debugging. This pin needs to be kept open (unconnected) or to be pulled up if not used for JTAG.
TMS	B1	DVDDA IN Schmitt trigger	Pull-up Pull-up Pull-up	JTAG mode selection input pin This pin is a serial signal input of the mode selection for test or debugging. This pin needs to be kept open (unconnected) or to be pulled up if not used for JTAG.
TDI	C5	DVDDA IN Schmitt trigger	Pull-up Pull-up Pull-up	JTAG data input pin This pin is a serial data input for test or debugging. This pin is for a chip boundary test and firmware development. This pin needs to be kept open (unconnected) or to be pulled up if not used for JTAG.
TDO	C4	DVDDA TristateOUT 4 mA	Hi-Z Hi-Z Hi-Z	JTAG data output pin This pin is a serial data output for test or debugging. This pin needs to be kept open (unconnected) if not used for JTAG.
TRTCK	C3	DVDDA OUT 4 mA	OUT OUT OUT	ICE return clock output pin Wait control signal to JTAG clock when using ICE. This pin is used for firmware development using ICE. This pin needs to be kept open (unconnected) if not used for JTAG.

2.2.1. Power Supply Pins

Table 2-2 shows an attribute of each pin and the supply voltage for each pin at operation.

Table 2-2 Power supply pins

Pin name	Pin No.	Attribute	Condition	Functional description
		Type VDD/GND	Normal Exceptional	
VDD/ GND				
VPGM	C2	Digital VDD/GND	GND 3.3 V	Test pin for IC manufacturing VPGM shall be connected to GND directly.
DVDDA	A1 A6	Digital VDD	3.3 V —	Power supply pin for GPIOm pins (m = 0, 1, and 6 to 18) 3.3 V needs to be supplied to all DVDDA pins because two DVDDA pins, A1 and A6 are connected internally in the IC.
DVDDB	H7	Digital VDD	3.3 V —	Power supply pin for GPIOn pins (n = 2 to 5) 3.3 V needs to be supplied to DVDDB pin.
DVDD33USB	A8	Digital VDD/GND	GND —	Test pin (for power supply) This pin needs to be connected to GND in normal operation.
CVDD	A7 H6	Digital VDD	1.2 V —	Power supply pin for the IC core LDO output voltage (1.2 V) is supplied to the digital circuit in the IC. A capacitor of at least 0.8 µF or more in the operating temperature range needs to be connected to this pin as the load of LDO. All CVDD pins, A7 and H6 are connected internally in the IC.
CDVSS	E5 E6 F5 F6	Digital GND	GND —	GND pin for the digital core logic and I/O interface All CDVSS pins need to be connected to GND.
AVDD12X	E1	Analog VDD	1.2 V —	Power supply pin for the crystal oscillator interface LDO output voltage (1.2 V) is supplied to the digital circuit in the IC. A capacitor of 0.8 µF or more needs to be connected in the operating temperature range as the load of the LDO.
AVDD12SYN	F1	Analog VDD	1.2 V —	Power supply pin for RFPLL This pin needs to be connected to LDOOUT12A.
AVDD12SG	G1	Analog VDD	1.2 V —	Power supply pin for LNA/ Receiver MIX (RxMIX)/ ADC/ DAC/ Low pass filter (LPF)/ PAcontrol/ BasebandPLL This pin needs to be connected to LDOOUT12A.
AVDD33PA	G2	Analog VDD	3.3 V —	Power supply pin for PA 3.3 V needs to be supplied to AVDD33PA pin.
AVSS12X	E2	Analog GND	GND —	GND pin for the crystal oscillator interface AVSS12X pin needs to be connected to GND.
AVSS12SYN	F2	Analog GND	GND —	GND pin for RFPLL AVSS12SYN pin needs to be connected to GND.
AVSS12ADC	F3	Analog GND	GND —	GND pin for ADC/ DAC/ LPF/ BasebandPLL AVSS12ADC pin needs to be connected to GND.
AVSSSG	H1 H3	Analog GND	GND —	GND pin for LNA/ RxMIX/ PAcontrol/ PA All AVSSSG pins need to be connected to GND.
LVDD33D	H5	LDO IN VDD	3.3 V —	Power supply pin for LDO-type regulator for the digital core 3.3 V needs to be supplied to LVDD33D pin.
LVDD33A	G5	LDO IN VDD	3.3 V —	Power supply pin for LDO-type regulator for the analog core 3.3 V needs to be supplied to LVDD33A pin.
LVSS33	D4 G4	LDO GND GND	GND —	GND pin for LDO-type regulators for the analog core and the digital core All LVSS33 pins need to be connected to GND.

Pin name	Pin No.	Attribute	Condition	Functional description
		Type VDD/GND	Normal Exceptional	
LDOOUT12A	H4	LDO OUT OUT	OUT —	Voltage output pin of LDO-type regulator for the analog core LDOOUT12A pin needs to be connected to both AVDD12SYN pin and AVDD12SG pin. A capacitor of 0.8 μF or more needs to be connected in the operating temperature range as the load of the LDO.

3. System Configuration

3.1. Block Diagram

Figure 3-1 shows a block diagram of TC35661 and a connection example to peripheral devices.

TC35661 should have a single power supply of 3.3 V or 1.8 V, and the IC has LDO regulators that have to have external capacitors.

The reference operation clock of 26 MHz should be input.

TC35661 supports the sleep clock function for low power operation. External clock input and the divided clock of the internal system clock are selectable. 32.768-kHz external clock should be used to save more power.

To connect a serial memory, use SPI or I^2C interface.

Host CPU interface can be UART one.

Some of the functional blocks, circuits, and constants in the block diagram may be omitted or simplified for explanatory purpose.

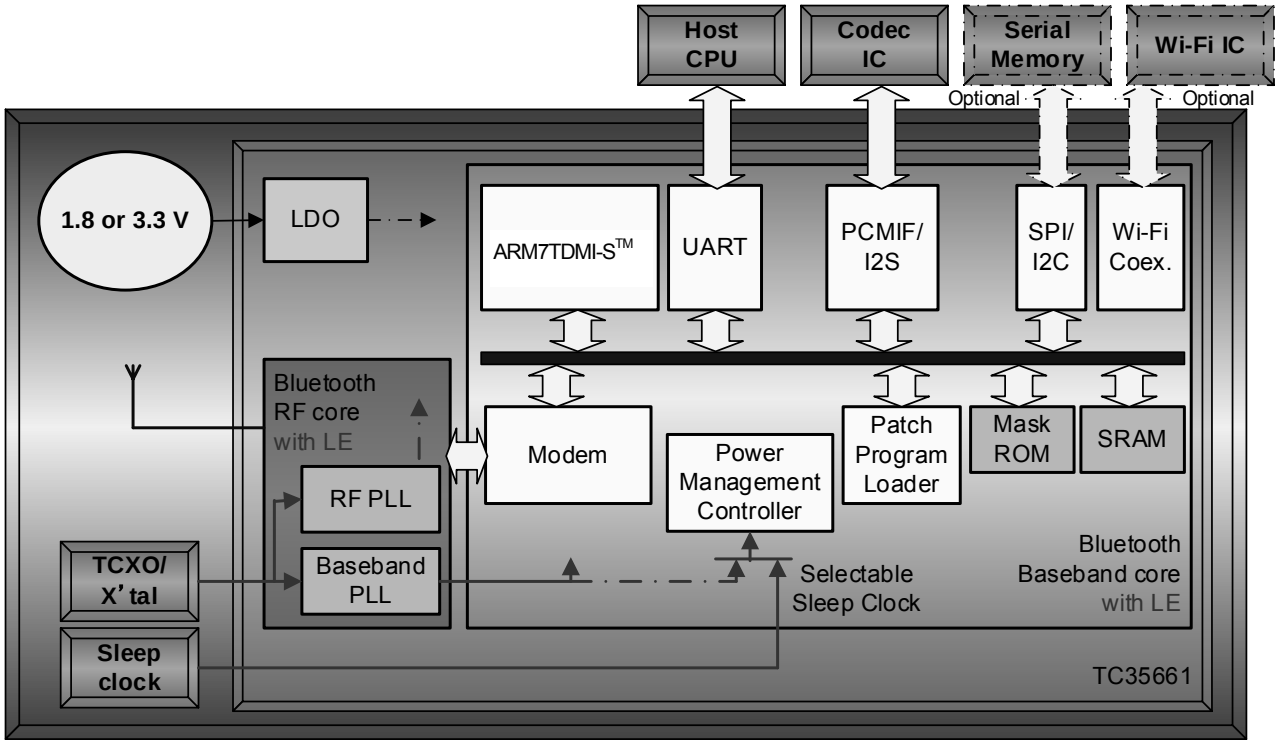

Figure 3-1 TC35661 block diagram and a connection example to peripheral devices

4. Hardware Interface

4.1. Reset Interface (Power Supply Sequence)

4.1.1. Features

Reset interface has the following features.

- 3.3 V or 1.8 V operation
- Level sensitive asynchronous reset (Low level: reset)

When the power is turned on, set the reset signal in the reset state (RESETX = Low). After the power supply and the clock are stable, release the reset.
Crystal oscillator stable time is about 2 ms, so set the reset release time after enough evaluation.
When the power is turned off, set the reset signal in the reset state (RESETX = Low). If the power is turned off while the reset signal is High, this IC may be destroyed due of overcurrent flow to VDD pins.

4.1.2. Connection Example

The reset interface can be connected to Reset IC or the device which has the level sensitive asynchronous reset function.
Figure 4-1 shows a Reset IC connection example. Figure 4-2 and Figure 4-3 show the reset sequences of Power-on and Power-off, respectively.

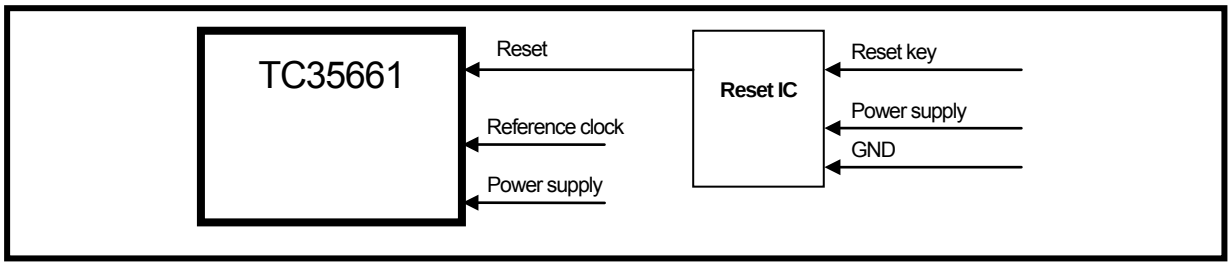

Figure 4-1 Rest IC connection example

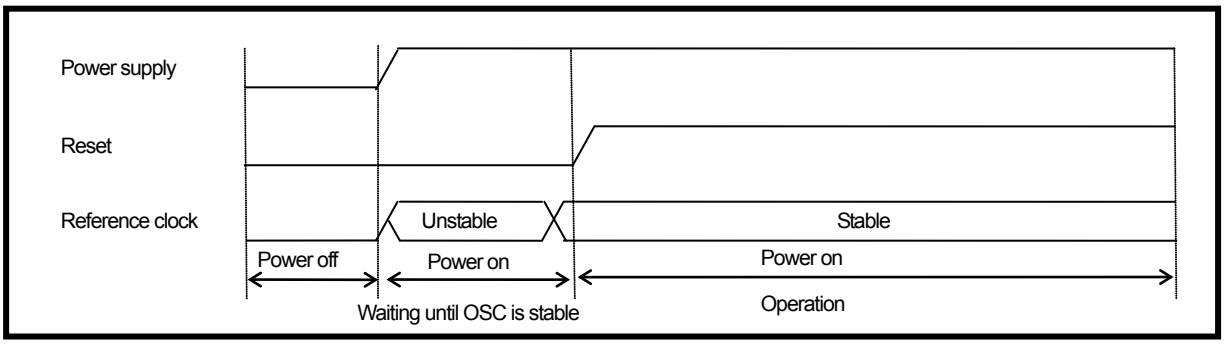

Figure 4-2 Power-on reset sequence

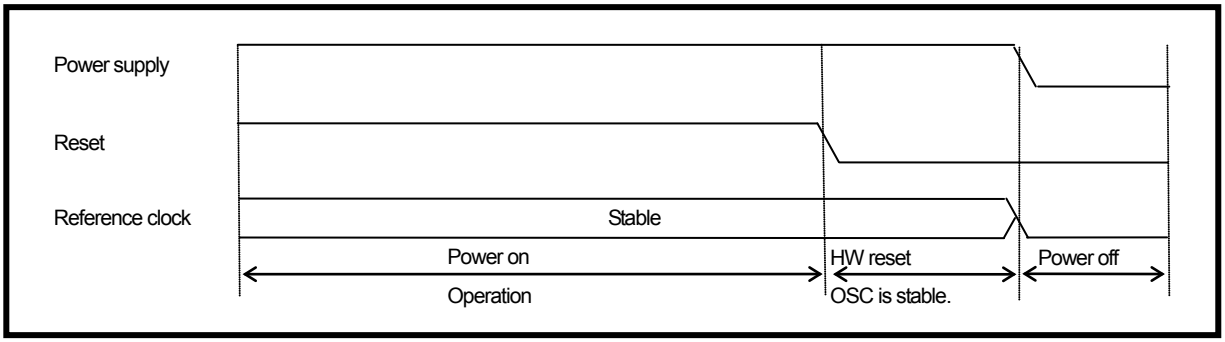

Figure 4-3 Power-off reset sequence

4.2. UART Interface

4.2.1. Features

TC35661 UART interface has the following features.

- Operation voltage: 3.3 V or 1.8 V
- Full-duplex 4-wire start/stop synchronization data transfer: RX, TX, RTSX, and CTSX
- Data format (No parity bits): LSB first
  - Start bit (1-bit)
  - Data bit (8-bit)
  - Stop bit (1-bit)
- Programmable baud rate: 2400 bps to 4.33 Mbps (Default 115200 bps)
- Error detection: Inter-character timeout, Overrun error, and Framing error

TC35661 UART interface is used to transfer commands, status, and data with the Host CPU, and the pin is multiplexed with GPIO pin. After release of the reset, TC35661 firmware sets UART interface function to the related GPIO pins in Boot procedure. Operation voltage is 3.3 V. The power voltage cannot be selected only for the UART interface because the power supply is shared by other hardware interfaces.

4.2.2. Connection Example

The UART interface can connect with the Host CPU which has UART function.
Figure 4-4 shows UART connection example with an external Host CPU.
Figure 4-5 shows a sequence diagram from reset state to setting of UART pins.

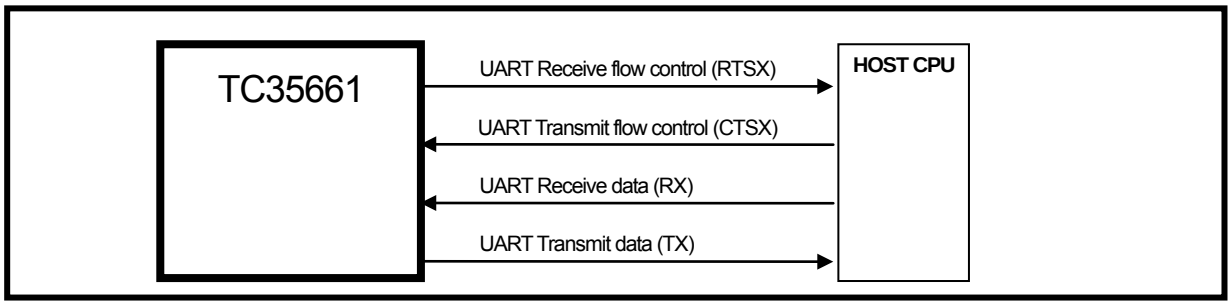

Figure 4-4 UART connection example

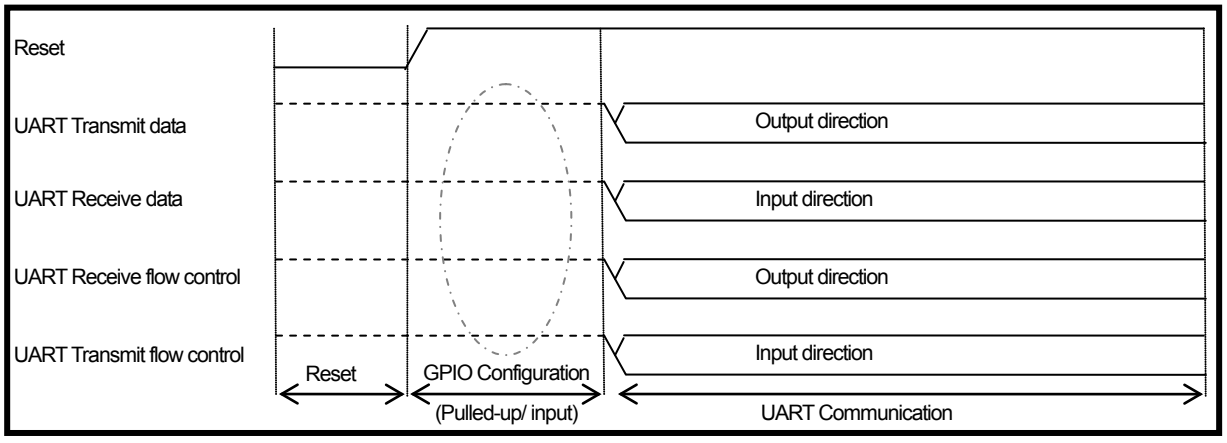

Figure 4-5 Assignment of UART function

4.2.3. Frame Format

TC35661 supporting format is as follows.

- Number of data bits: 8 bits
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX

Figure 4-6 shows UART data frame.

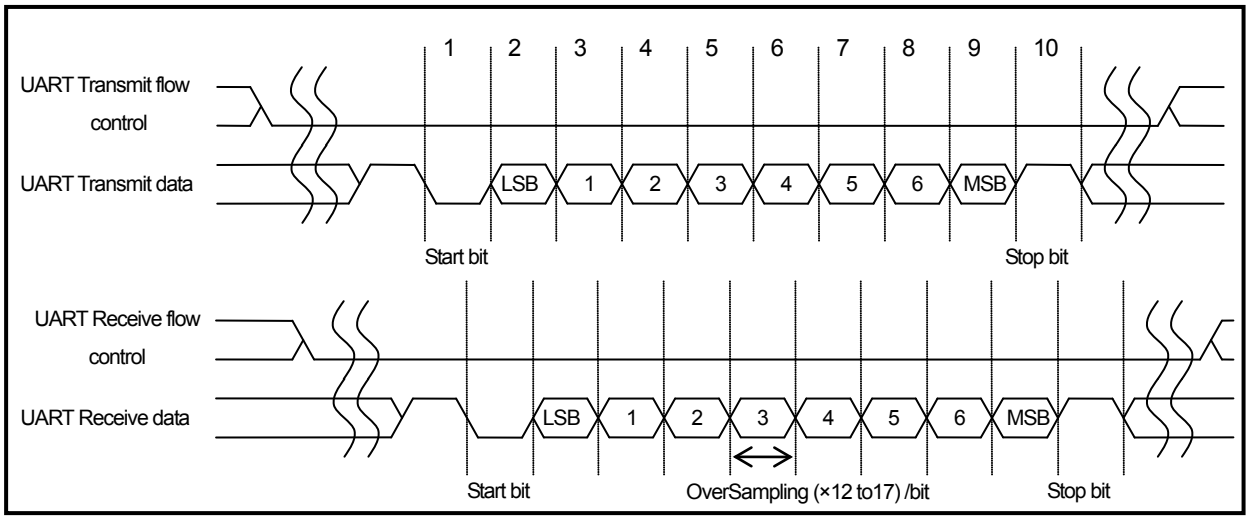

Figure 4-6 UART data frame

4.2.4. Flow Control Function

TC35661 UART interface uses flow control function by hardware signals, Transmit flow control (CTSX) and Receive flow control (RTSX). Figure 4-4 shows the signal input and output directions. Figure 4-6 shows the signal polarities.

CTSX input signal is used for UART transmitting. Low input indicates the completion of the preparation for the other party to receive data and TC35661 does UART transmitting if there is data for transmission. In case of High level input, TC35661 stops transmitting in the units of the UART frame.

RTSX output signal is used for UART receiving. Low output indicates data transmission request to UART transmission side device of the other party. TC35661 outputs Low level from RTSX when it can receive data, and it prepares to receive data. When it becomes Busy where data reception is disabled, it outputs High level and stops UART transmitting in the units of the UART frame.

Response time of UART transmitting and receiving for the flow control signal depends on the baud rate and the frame internal process status. It is from 1 frame to 4 frames.

4.2.5. UART Baud Rate Setting

TC35661 UART interface has a programmable baud rate setting function. The UART baud rate can be set using the over-sampling number and the dividing ratio according to the following equation. The baud rate generating clock frequency is set to either 39 MHz or 52 MHz. The over-sampling number is set to an integer that ranges from 12 to 17. The dividing ratio is set to an integer that ranges from 1 to 65,535.

$$UART\,BaudRate = \frac{Baud\,Rate\,Generating\,Clock\,Frequency}{Over-Sampling\,Number \times Dividing\,Ratio}$$

Table 4-1 shows examples of the target baud rates supported by TC35661. If the other target baud rate is necessary, please contact our representative.

Table 4-1 UART Baud rate setting

Target baud rate [bps]	Actual baud rate [bps]	Baud rate generating clock frequency [MHz]	Over-sampling number	Dividing ratio	Deviation [%]
115,200	116,071	52	14	32	+0.7564
921,600	928,571	52	14	4	+0.7564
1,843,200	1,857,143	52	14	2	+0.7564
4,329,600	4,333,333	52	12	1	+0.0862

4.2.6. Error Detection Function

TC35661 UART interface has 3 kinds of error detection functions.

- Receiver timeout error
- Receiver overrun error
- Receiver frame error

Receiver timeout error judges as an error if the interval between reception frames counted by TC35661 internal timer is equal to or greater than a predetermined time

Receiver overrun error judges as an error if UART reception frame buffer in TC35661 overflows. When data transfer is done according to the flow control in Section 4.2.4, the overflow does not occur.

Receiver frame error judges as an error if a frame unit is not recognized. If “0” is detected as Stop bit field after Start bit detection, it is considered that the frame organization fails.

4.3. Audio CODEC Digital Interface

4.3.1. Features

TC35661 has the following main features for an audio CODEC digital interface.

- Operation voltage: 3.3 V or 1.8 V
- Data format: A-law, μ-law, and Linear PCM
- Frame format: MSB left-justified, I^2S, and PCM digital
- Frame frequency: 8 kHz and 16 kHz
- Data length: 8-bit and 16-bit
- Bit clock function: Master and Slave
- Data sampling edge: Rise and fall edges
- Frame synchronization signal polarity: High-active and Low-active
- Built-in CODEC:
  - CVSD (Continuous variable slope delta modulation)
  - PCM (Pulse code modulation)

TC35661 transmits and receives audio data through the audio CODEC digital interface.
The pins in the audio CODEC digital interface are multiplexed with GPIO pins. After release of the reset, TC35661 firmware sets the interface function to the related GPIO pins in Boot procedure.
This interface does not share a power supply pin with the other hardware interface so it is able to use its own voltage.

4.3.2. Connection Examples

This CODEC digital interface can be connected to a CODEC IC and a DSP (Digital signal processor) using the same digital interface. Figure 4-7 through Figure 4-9 show connection examples for each operation mode. The selection of Master mode or Slave mode is done at the configuration setting. When this IC operates in Slave mode, the master is the device which has the bit clock and control function of the frame synchronization signal.
Figure 4-10 shows a sequence of the assignment of the CODEC function to the related GPIO pins.

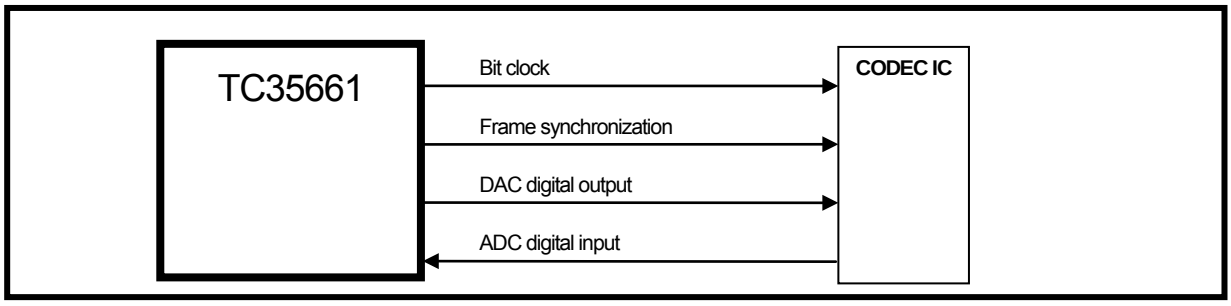

Figure 4-7 CODEC connection example (TC35661 is Master.)

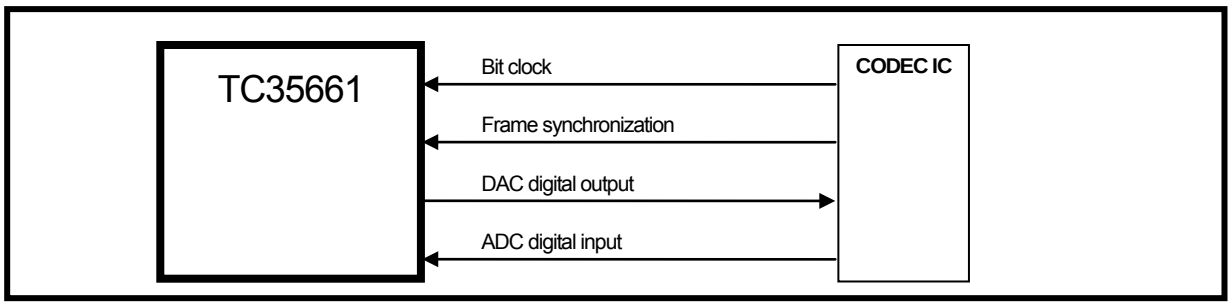

Figure 4-8 CODEC connection example (TC35661 is Slave.)

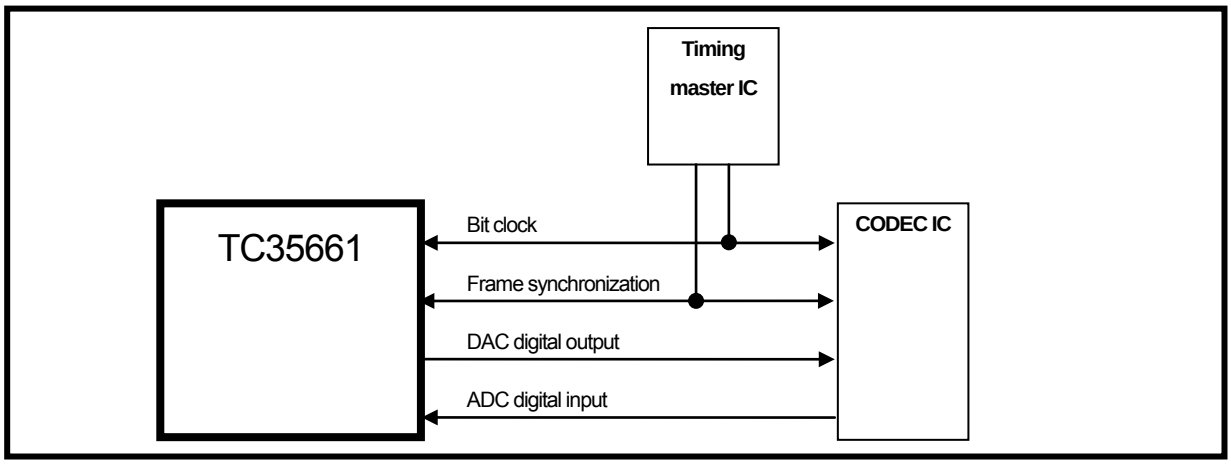

Figure 4-9 CODEC connection example (TC35661 and CODEC are Slaves.)

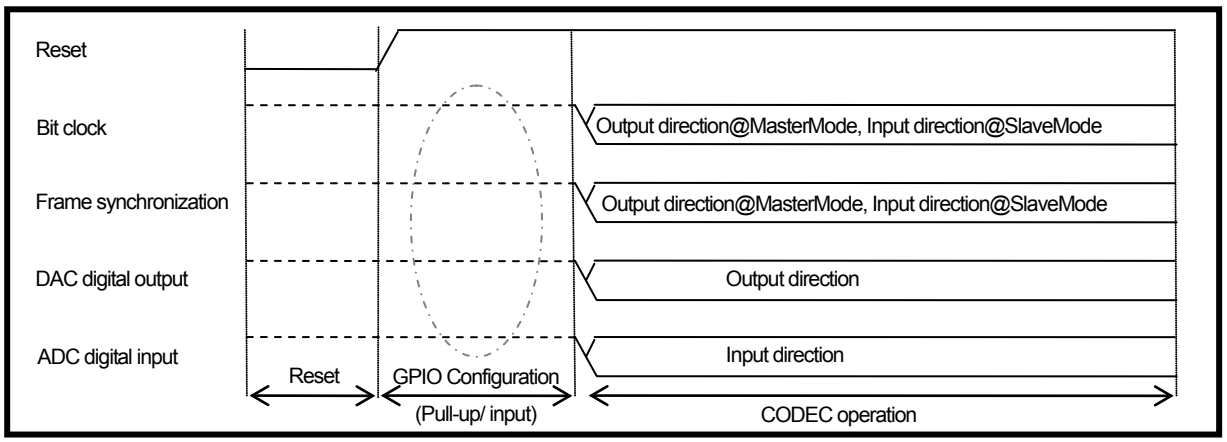

Figure 4-10 Assignment of CODEC interface function

4.3.3. Frame Format

There are several frame formats for a CODEC digital interface. TC35661 supports one of the most popular frame formats.

- MSB left-justified
- MSB right-justified
- I^2S
- PCM digital short frame
- PCM digital long frame

The following data lengths are supported.

- 8 bits
- 16 bits

Figure 4-11 through Figure 4-15 show the frame formats of the audio CODEC digital interface.
Note that if monaural data are handled using MSB left-justified format and I^2S format, either left channel or right channel always has the dummy data that can be all-0 data, all-1 data or previously transferred data.

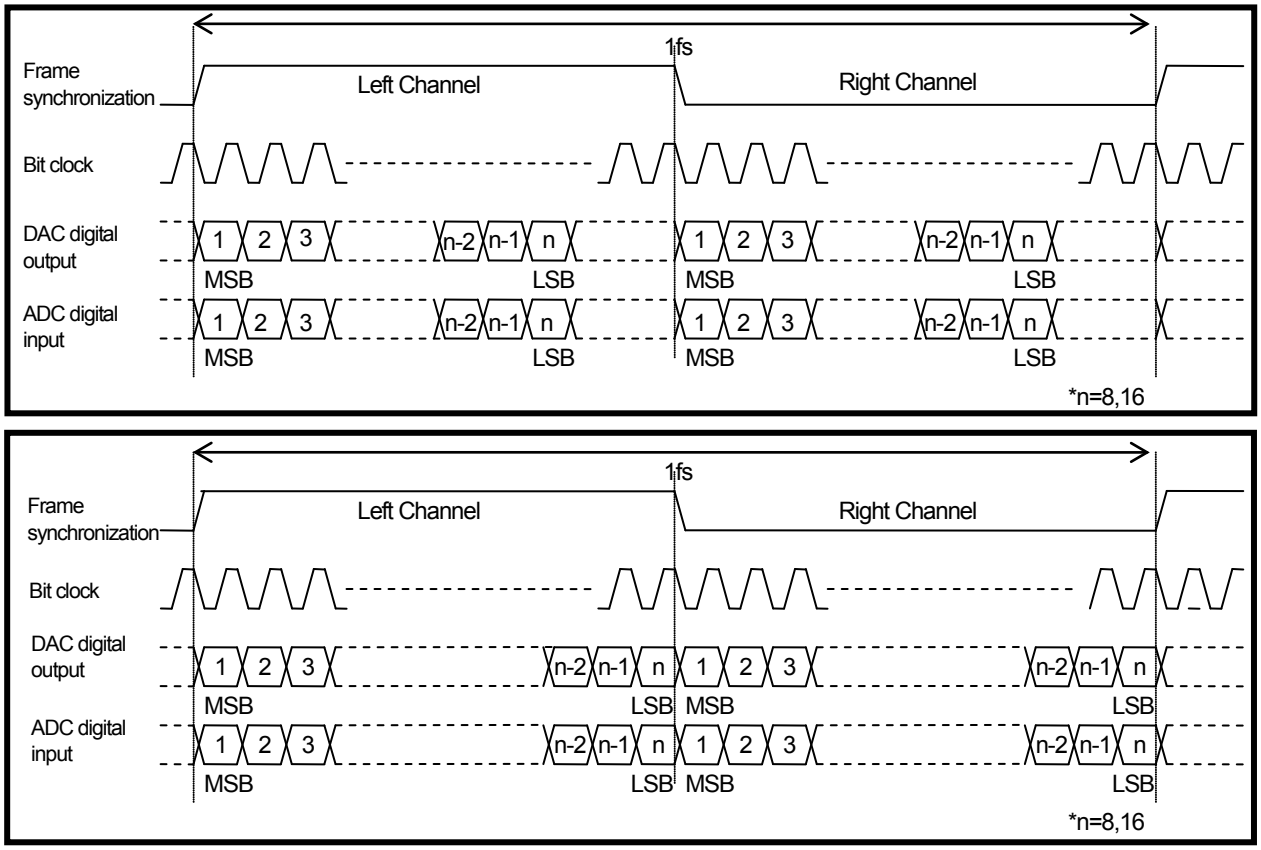

Figure 4-11 MSB left-justified format

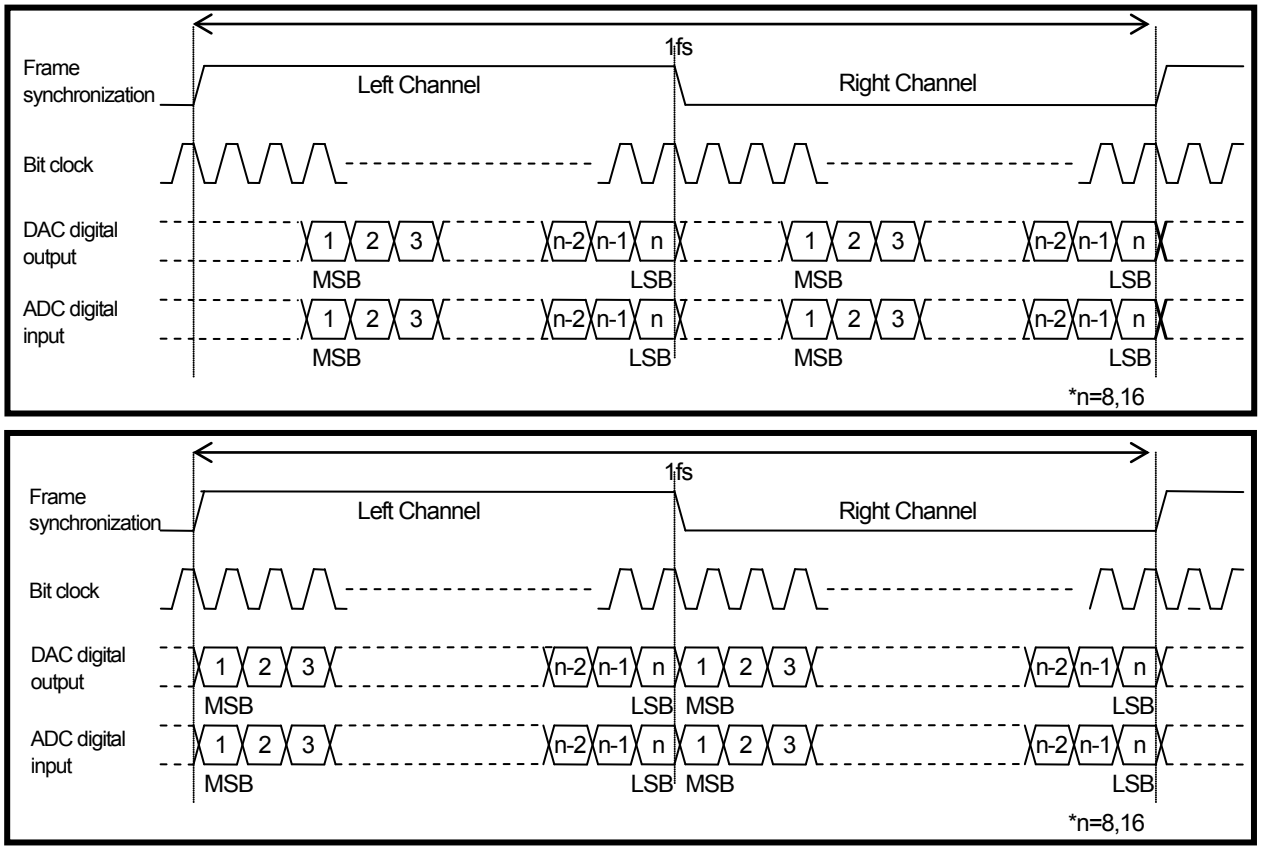

Figure 4-12 MSB right-justified format

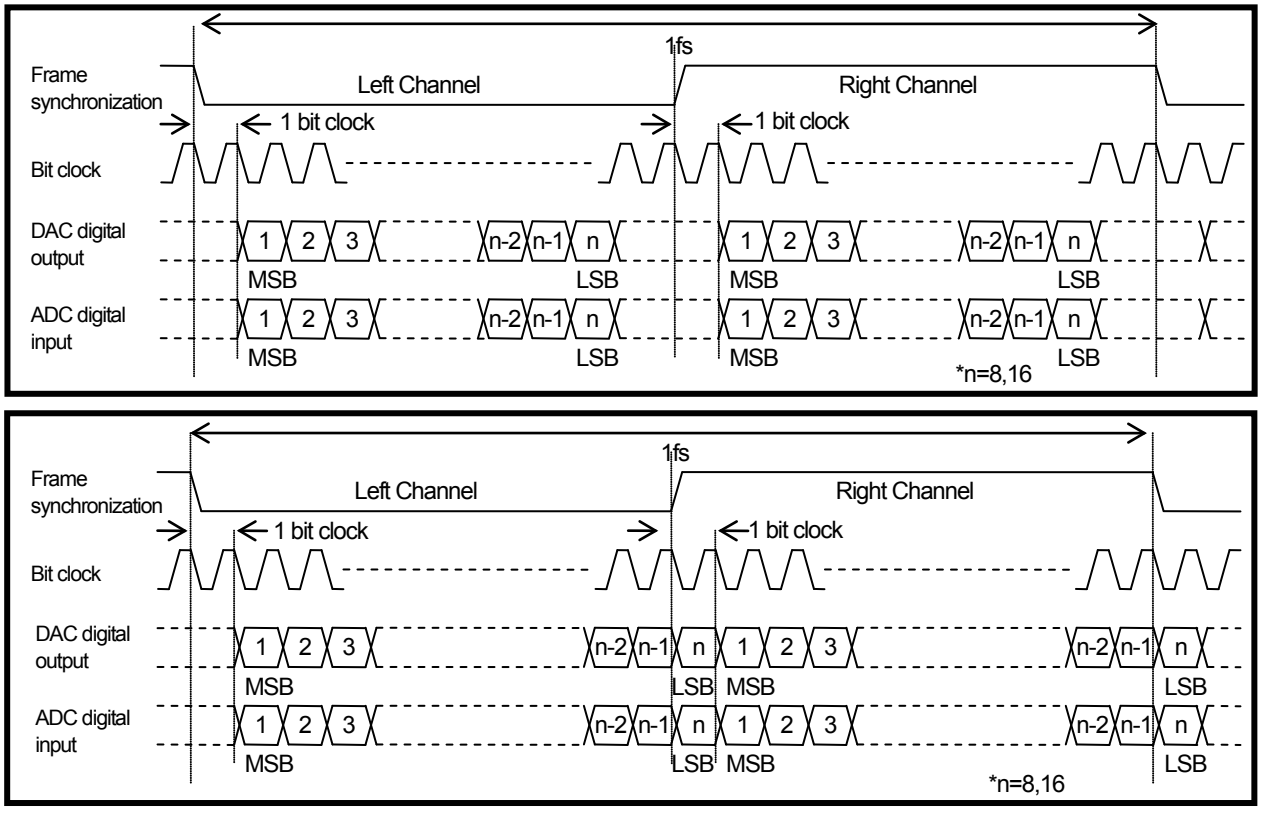

Figure 4-13 I^2S format

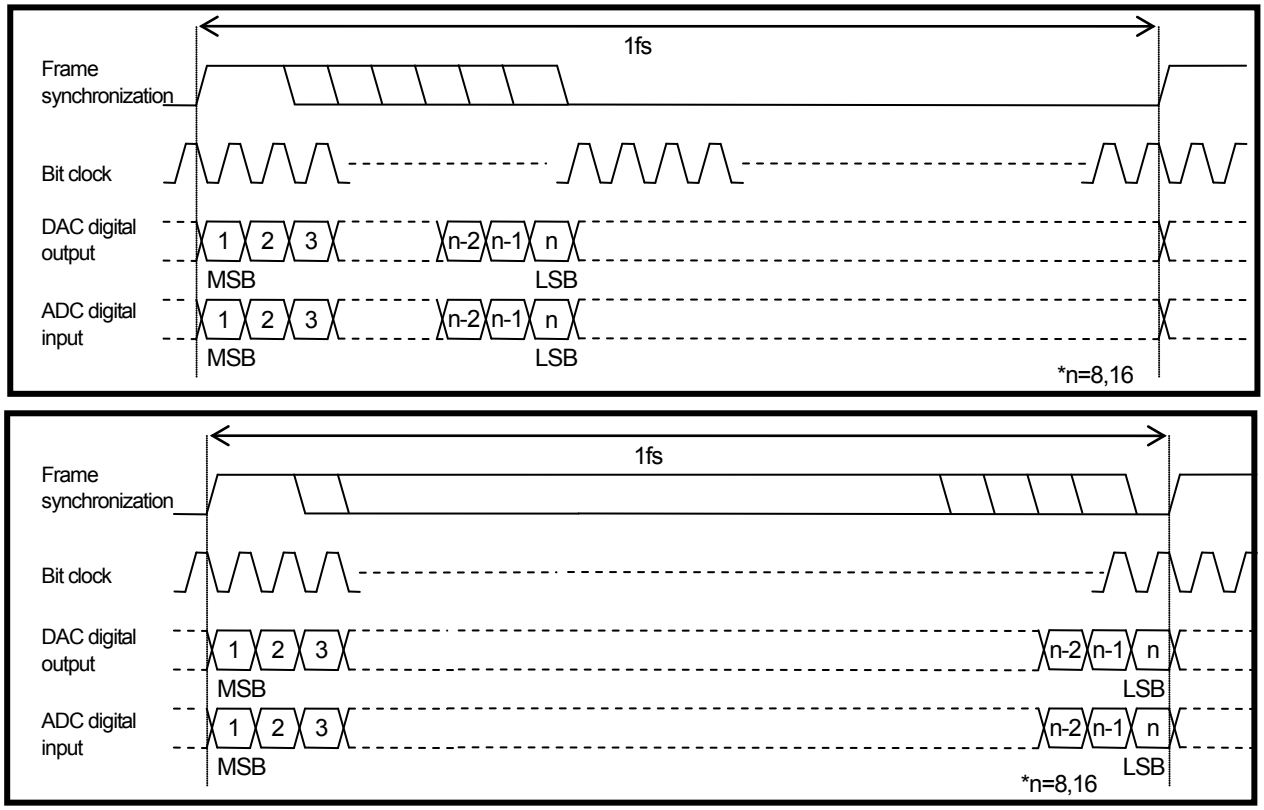

Figure 4-14 PCM digital long frame format

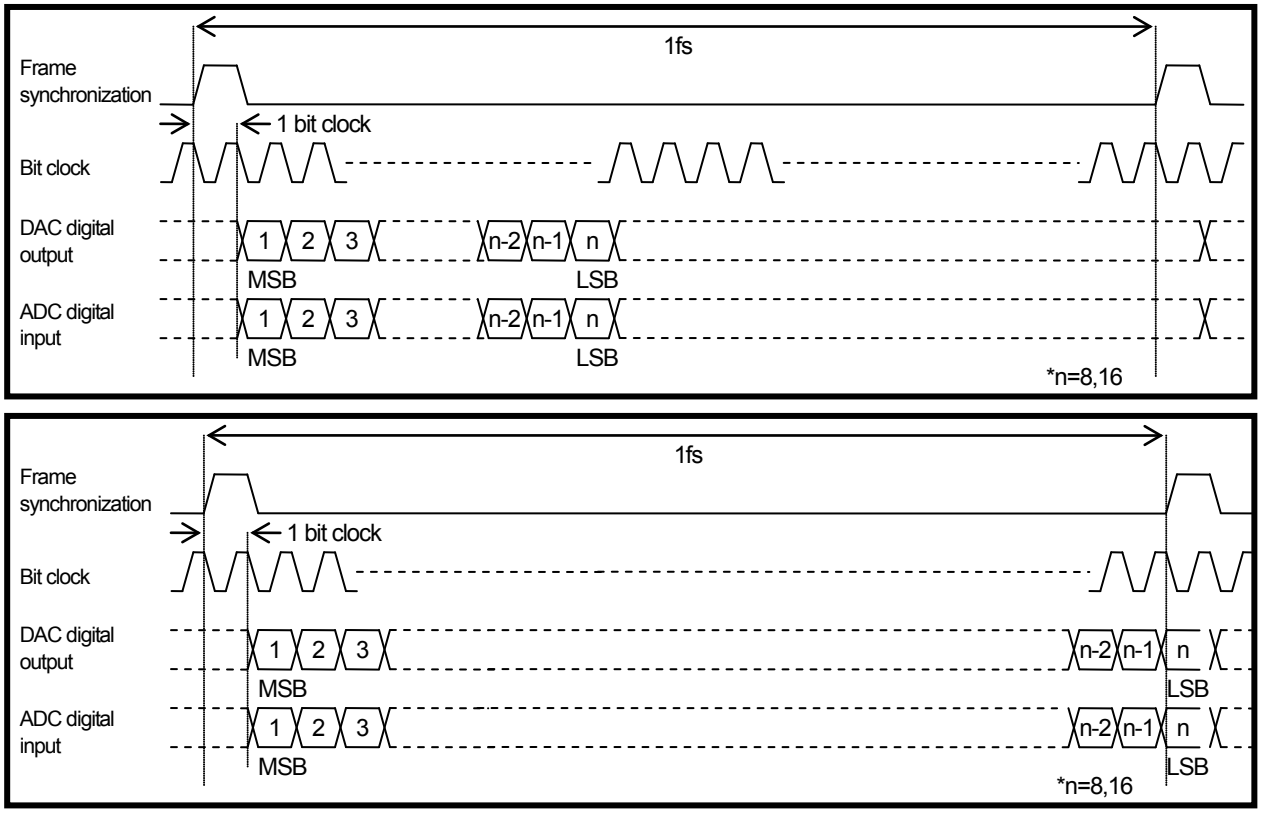

Figure 4-15 PCM digital short frame format

4.3.4. Programmable Polarity Changing

The audio CODEC digital interface can program the change of the polarity of the sampling edge and the polarity of the frame synchronization signal, respectively.
Data transmitting and receiving timings can be configured as shown in Figure 4-16.
Edge polarity can be settings of two types.

- A: transmission timing @ falling edge, reception sampling @ rising edge
- B: transmission timing @ rising edge, reception sampling @ falling edge (default)

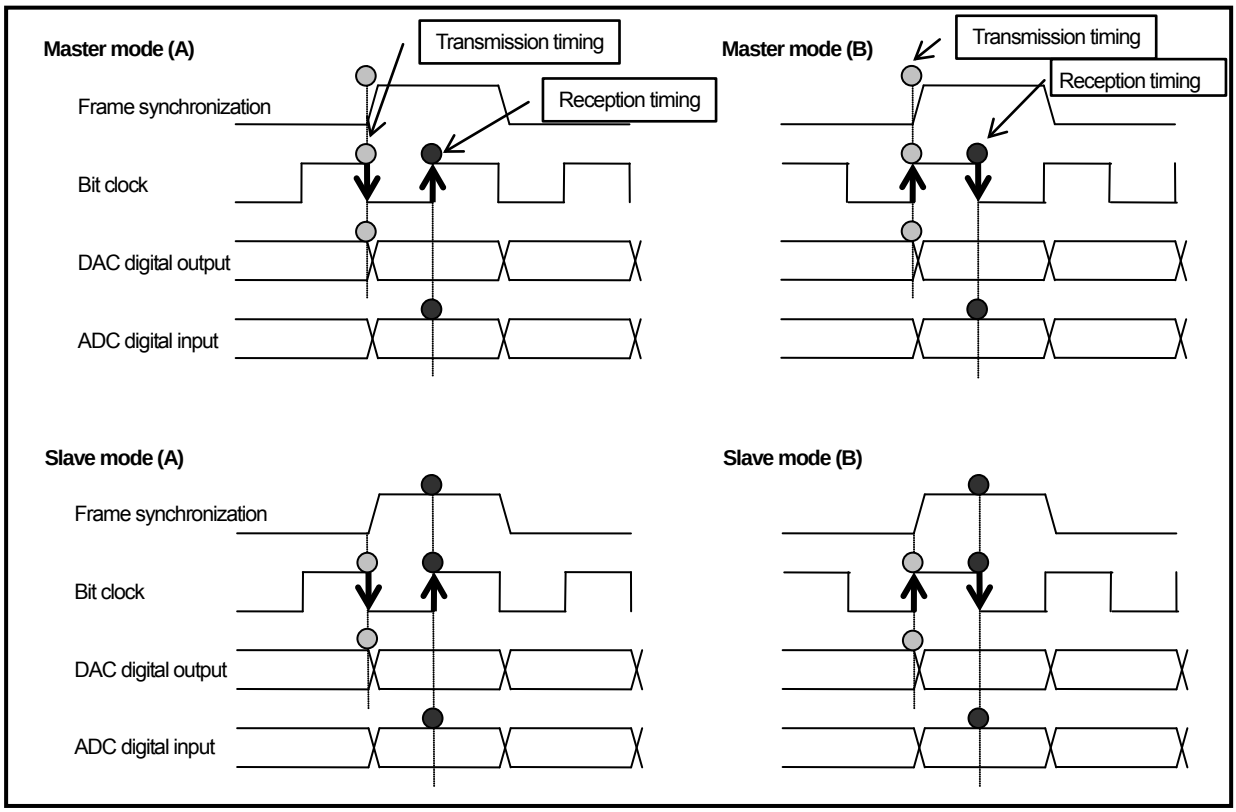

Figure 4-16 Transmission and reception sampling edges

Figure 4-17 shows the timing chart of the frame synchronization polarity and the data channel. 4 different settings can be done for the frame synchronization polarity and the stereo data L/R swap.

- A: Frame synchronization signal: Low (Lch) → High (Rch)
- B: Frame synchronization signal: High (Lch) → Low (Rch) (Default)
- C: Frame synchronization signal: Low (Rch) → High (Lch)
- D: Frame synchronization signal: High (Rch) → Low (Lch)

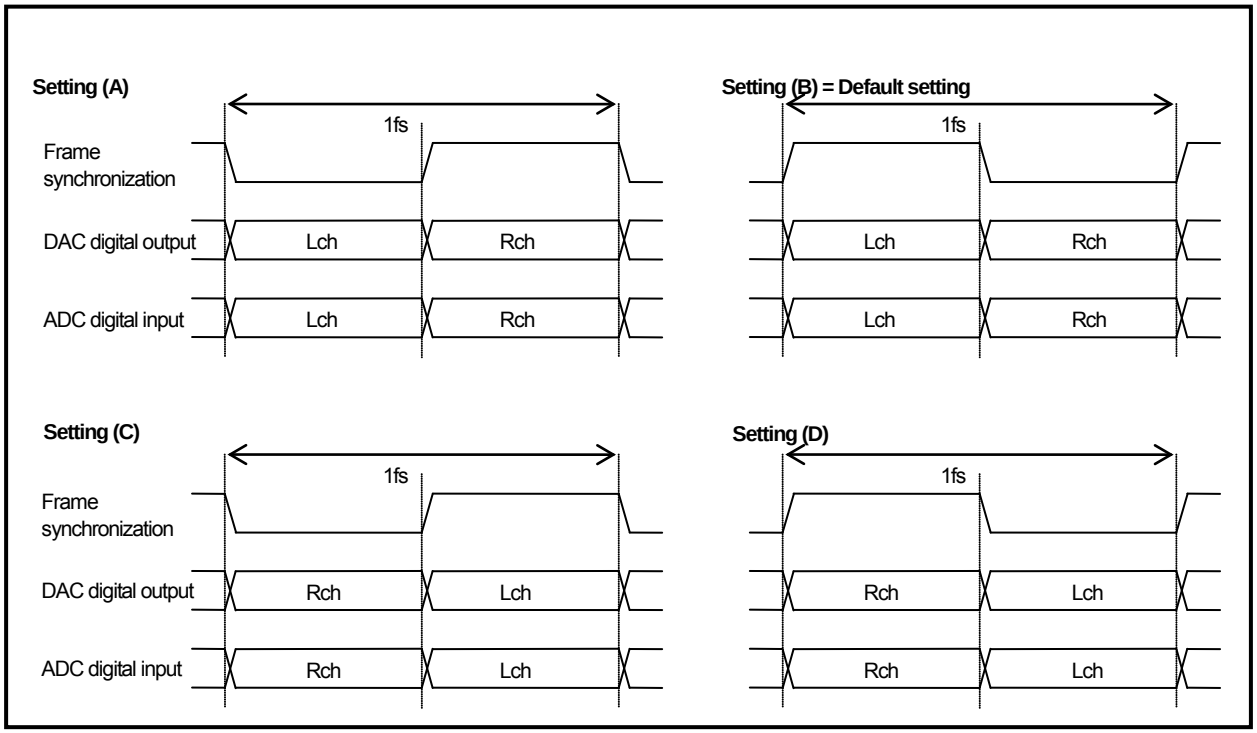

Figure 4-17 Frame synchronization polarity and data channels

4.3.5. Bit Clock Frequency in Master Mode

The audio CODEC digital interface has a bit clock and control function of the frame synchronization signal, and has Master mode and Slave mode. This section describes the Master mode.
TC35661 outputs the bit clock and the frame signal when it is a bit clock master device. The frequency of the bit clock is either fixed or switched between two frequencies. This can be done because the bit clock is generated by dividing the internal reference clock of TC35661. The examples of mixed frequencies are shown in Figure 4-18 and Figure 4-19.The example of a fixed frequency is shown in Figure 4-20.
In the bit clock slave mode, the frequency of the bit clock should be a frequency of the integral multiple of the sampling frequency.

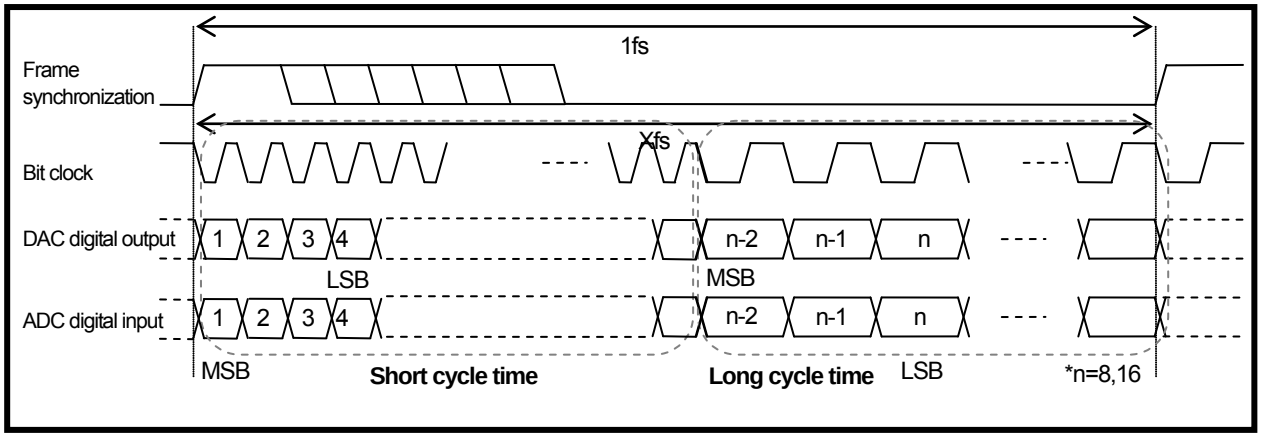

Figure 4-18 Bit clock whose frequency is switched (1)

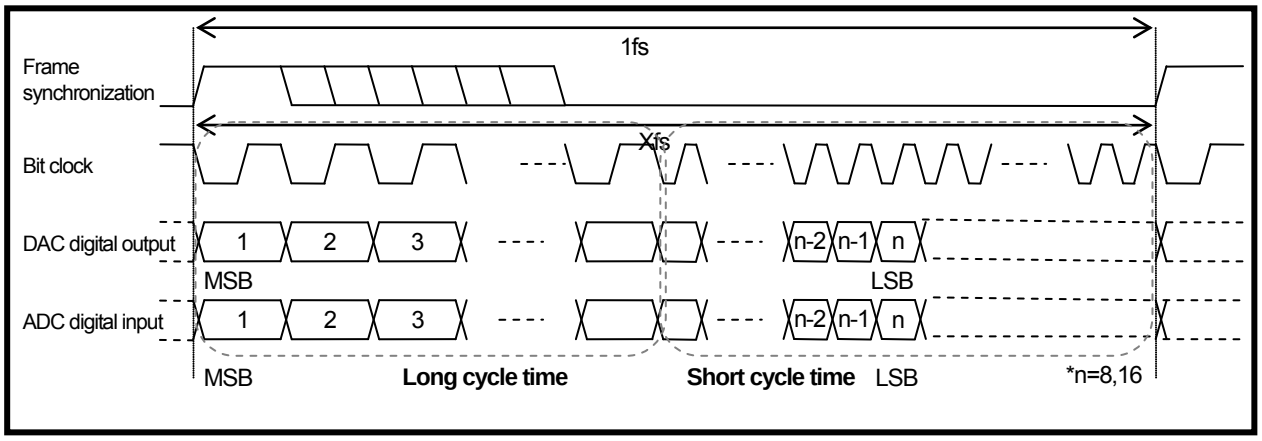

Figure 4-19 Bit clock whose frequency is switched (2)

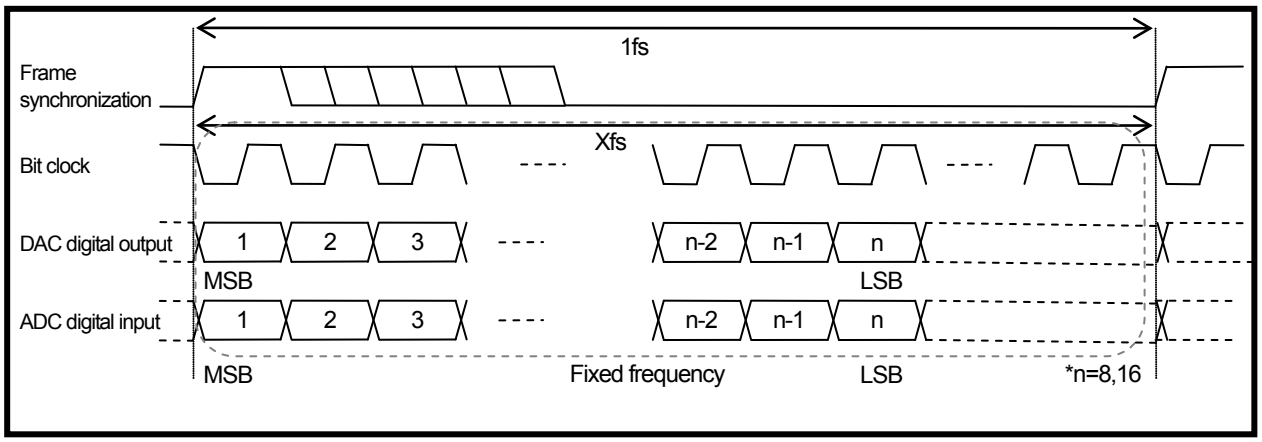

Figure 4-20 Bit clock of a fixed frequency

Table 4-2 shows examples of the bit clock frequency which can be generated.

Table 4-2 Examples of the generated bit clock frequency

Frame synch frequency [kHz]	Number of Bit clock [FS]	Bit clock frequency switching	Bit clock frequency for a short cycle time [kHz]	Bit clock frequency for a long cycle time [kHz]
8	50	No	400	—
	52		416	—
	100		800	—
	130		1040	—
	250		2000	—
	8	Yes	64.20	63.88
	16		128.71	127.45
	32		257.43	254.90
	64		520.00	500.00
	128		1040	1000.00
16	50	No	800	—
	130		2080	—
	250		4000	—
	32	Yes	509.80	514.85
	64		1040	1000.00
	128		2080	2000.00

4.4. Serial Memory Interface

4.4.1. Features

TC35661 has the following main features for a serial memory interface.

- Operation voltage: 3.3 V
- Supports two formats (One of either SPI interface or I^2C bus interface should be selected.)
  - ✓ SPI interface
    - Chip select: 2 channels
    - Chip select polarity: High-active or Low-active, selectable
    - Serial clock master function: Selectable clock polarity and phase (One is selected from among 4 cases.)
    - Serial clock frequency: 101.96 kHz to 26 MHz (CPU: 52 MHz)
    - Serial data transfer mode: MSB-first and LSB-first
  - ✓ I^2C bus interface
    - Serial clock master operation
    - Serial clock frequency: Standard mode (100 kHz or less) Fast mode (400 kHz or less)
    - Output mode: Open-drain output and CMOS output
    - Device address format: 7-bit address (10-bit address is not supported.)

4.4.2. Connection Example

A serial EEPROM and a serial Flash-ROM are connected to TC35661 using the serial memory interface. The interface frame format can be either I^2C bus or SPI format. SPI format can be used as a control interface for some voice CODEC devices, too.

Figure 4-21 shows a connection example of a serial EEPROM using I^2C bus interface of the open-drain mode. Each external pull-up resistor (Rext) is necessary for both the serial clock line and the serial data line.
Figure 4-22 shows another connection example where I^2C bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC35661 nor the serial EEPROM.

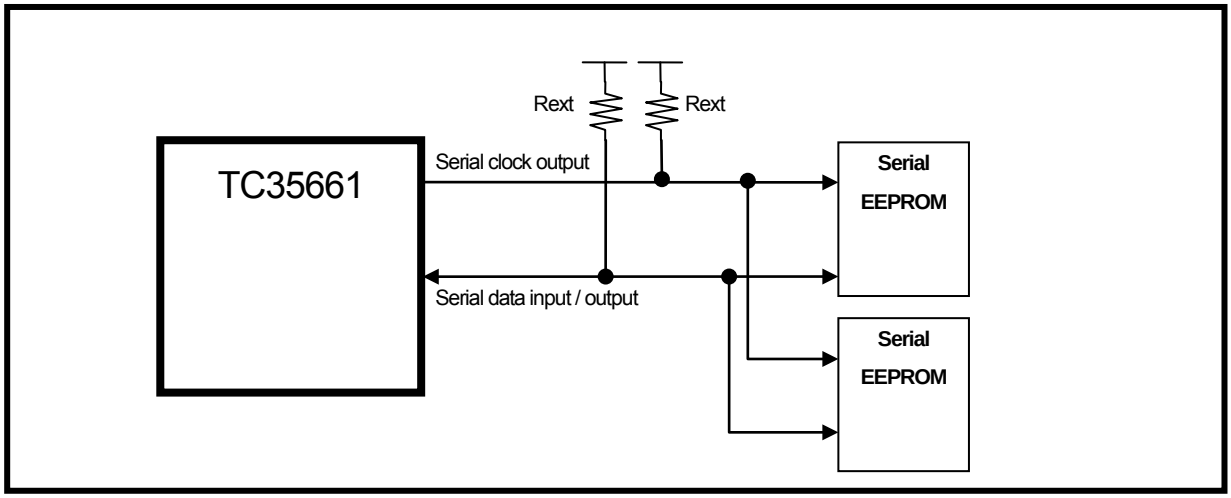

Figure 4-21 Connection example for serial EEPROM with I^2C-bus interface (Open-drain output)

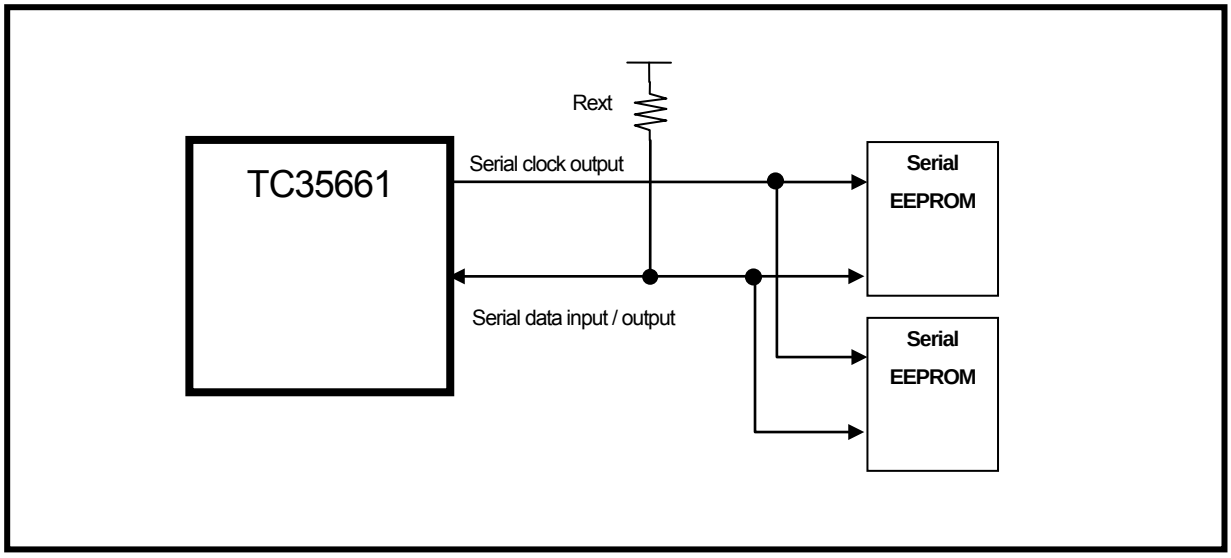

Figure 4-22 Connection example for serial EEPROM with I^2C-bus interface (CMOS output)

TC35661 has 2 Chip select ports for SPI interface.
Figure 4-23 shows a connection example, where both a serial Flash-ROM and a voice CODEC chip are connected to TC35661.

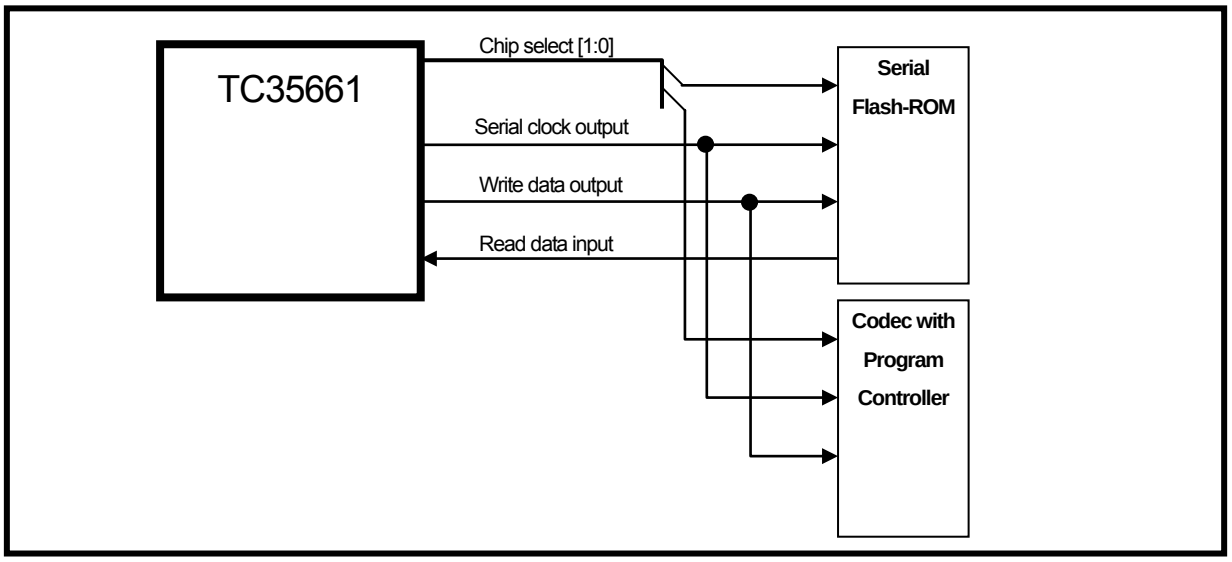

Figure 4-23 Connection example for serial Flash-ROM and CODEC using SPI interface

Figure 4-24 shows another connection example, where two serial Flash-ROM's are connected to TC35661.

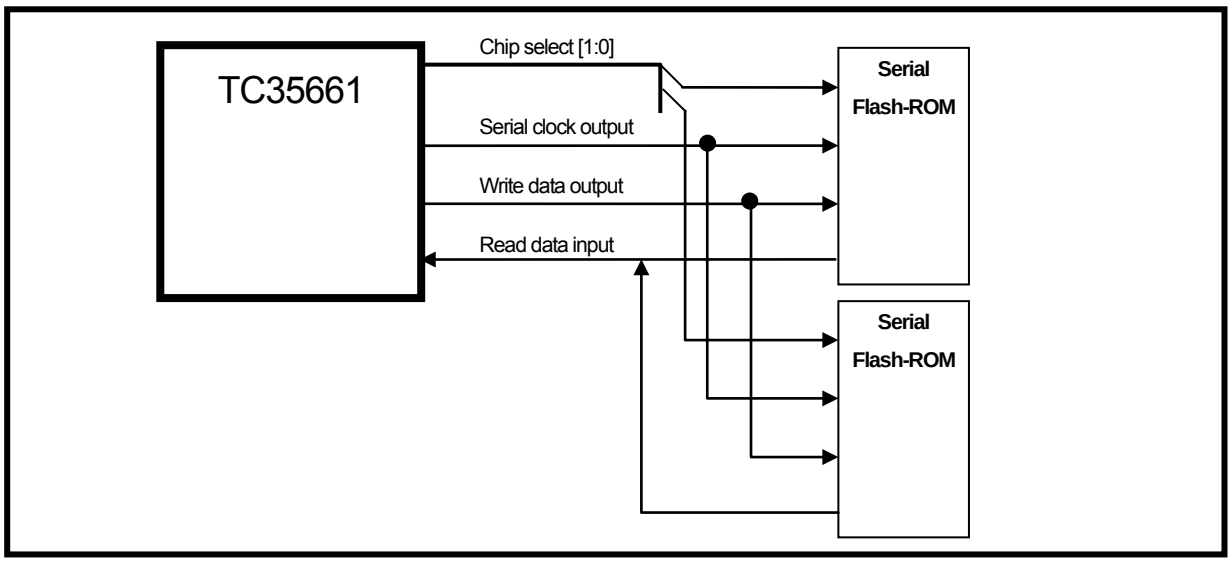

Figure 4-24 Connection example for two serial Flash-ROM's with SPI interface

Note: Some connections may need pull-up resistors on the data lines.

4.4.3. Selection of External Pull-up Resistor Value for I²C Bus Interface

The external pull-up resistor value needs to be selected by the following equations in case of I²C bus interface. Its maximum value is defined by the equation (1) in which t_r is a rise time of the serial clock and data, and C_b is I²C bus capacity. Its minimum value is defined by the equation (2) in which V_{dd} is a supply voltage for TC35661, V_{ol_max} is the maximum value of the low level output voltage, and I_{ol} is the low level output current.
Please select the value of the pull-up resistor in the range of the minimum value and the maximum value.

$$R_{ext\_max} = \frac{t_r}{0.8473 \times C_b} \quad (1)$$

$$R_{ext\_min} = \frac{V_{dd} - V_{ol\_max}}{I_{ol}} \quad (2)$$

TC35661 supports I²C bus standard mode (100 kHz or less) and I²C bus fast mode (400 kHz or less). The rise time t_r is 1000 ns for the standard mode and it is 300 ns for the fast mode. Cb value depends on a PCB and implementation on the board. Table 4-3 and Table 4-4 show examples when I²C bus capacity is 20 pF.

Table 4-3 External pull-up resistor value for I²C standard mode (Cb = 20 pF)

I²C bus frequency	100 kHz or less								
tr [ns]	1000								
Cb [pF]	20								
Vdd [V]	1.8			3.0			3.3		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	2.90	1.45	0.73
Rext_max [kΩ]	59.01								

Table 4-4 External pull-up resistor value for I²C fast mode (Cb = 20 pF)

I²C bus frequency	400 kHz or less								
tr [ns]	300								
Cb [pF]	20								
Vdd [V]	1.8			3.0			3.3		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	2.90	1.45	0.73
Rext_max [kΩ]	17.70								

4.4.4. Frame Format

There are several frame formats of the serial memory interface. TC35661 supports SPI and I^2C frame formats. These interfaces cannot be used simultaneously. Please select one appropriate interface.
When using SPI format serial memory, TC35661 sends a command identification code (C_k to C0) and an address (A_m to A0) in turn. For example, in the case of a read command (Figure 4-25), the serial memory transmits the byte data (a read data) specified by the address. TC35661 continues to assert Chip select until the read data amount reaches the expected byte count. In the case of a programming command (Figure 4-26), TC35661 continues to assert Chip select and transmits write byte data until the amount reaches the expected byte count.
The command identification code system and the address bit width will need to match the specifications of the serial memory to be used.

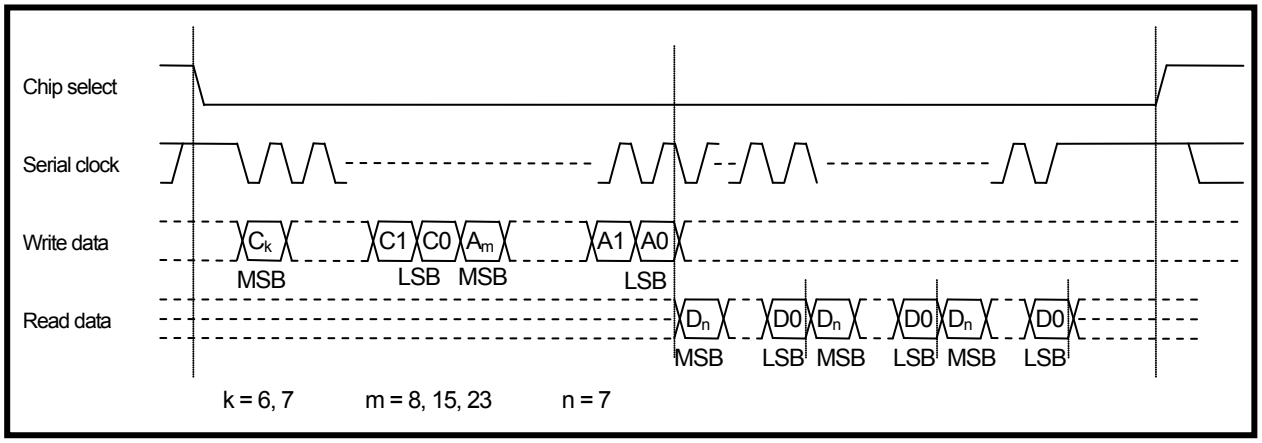

Figure 4-25 SPI format (Serial memory, read)

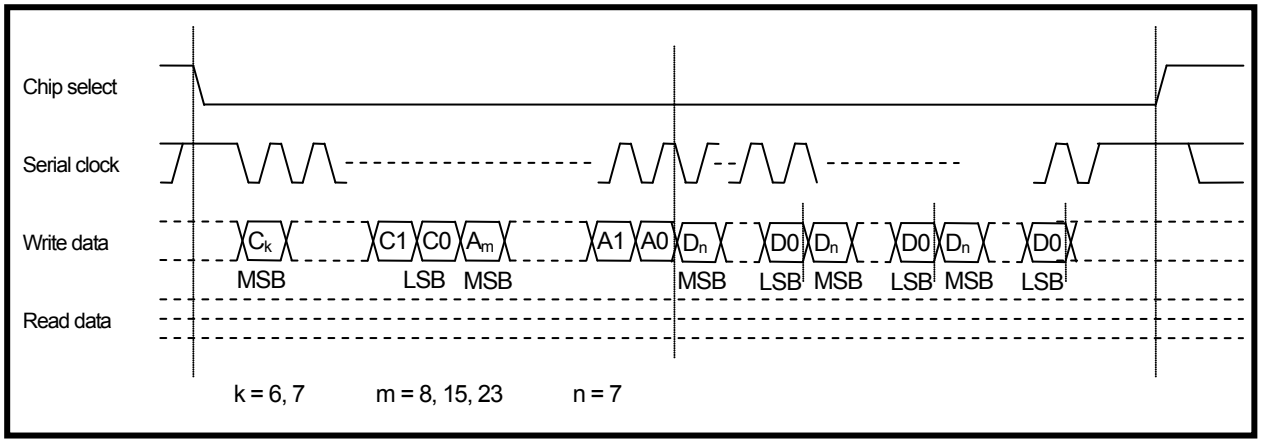

Figure 4-26 SPI format (Serial memory, programming)

When using I^2C format serial memory, TC35661 generates Start condition at first. Then it sends a device identification address (7 bits: [A6: A0]) and the first byte address of the access memory ([B7: B0]) to follow a read or write command bit. Any data in I^2C is transferred as MSB first. The value of the device identification address and how to specify the byte address are determined depending on the device to be connected, so they will need to match.
In case of read, TC35661 will return an acknowledgment bit (ACK: Acknowledge) or a reception denial bit (NACK: Not acknowledge) to the serial memory each time at 1 byte reception.
In case of write, TC35661 receives ACK or NACK from the serial memory each time at 1 byte transmission.
Multi-byte, not limited to 1 byte, is able to be handled continuously. TC35661 generates Stop condition after read or write of all bytes has been completed.

Figure 4-27 shows the case of 2-byte data read. Figure 4-28 shows the case of 2-byte data write. The gray signals and signal names are the output from the serial memory in those figures. In the read mode, TC35661 returns NACK after it receives the last byte data, which notifies the serial memory of the completion of the read.

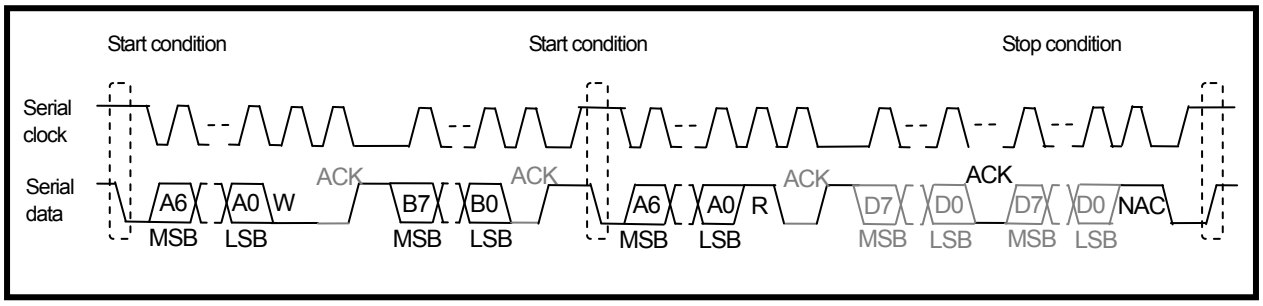

Figure 4-27 I^2C format (Serial memory, read)

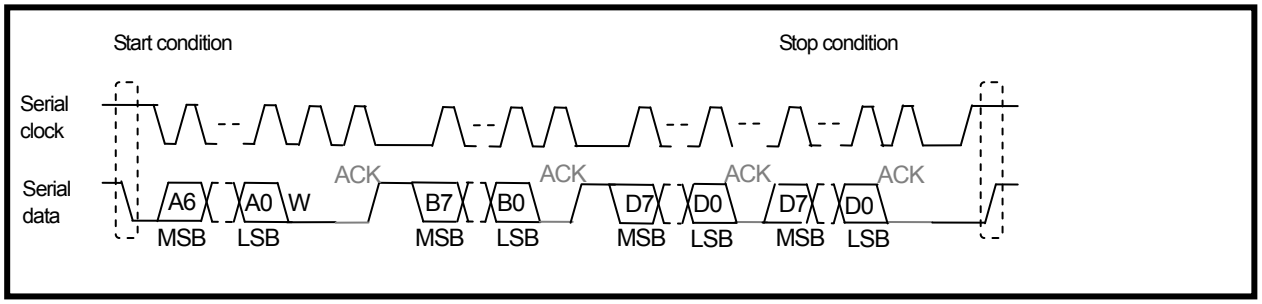

Figure 4-28 I^2C format (Serial memory, write)

When connecting the CODEC IC whose control interface is SPI interface, a specified address, the read or write type and so on are transmitted in the first 8 bits (X7 to X0). Please refer to each CODEC IC document for its format. Figure 4-29 shows an example to read a specified address byte data. Figure 4-30 shows an example to write data to a specified address. And Figure 4-31 shows an example to write continuously byte data to a specified address and the following addresses.

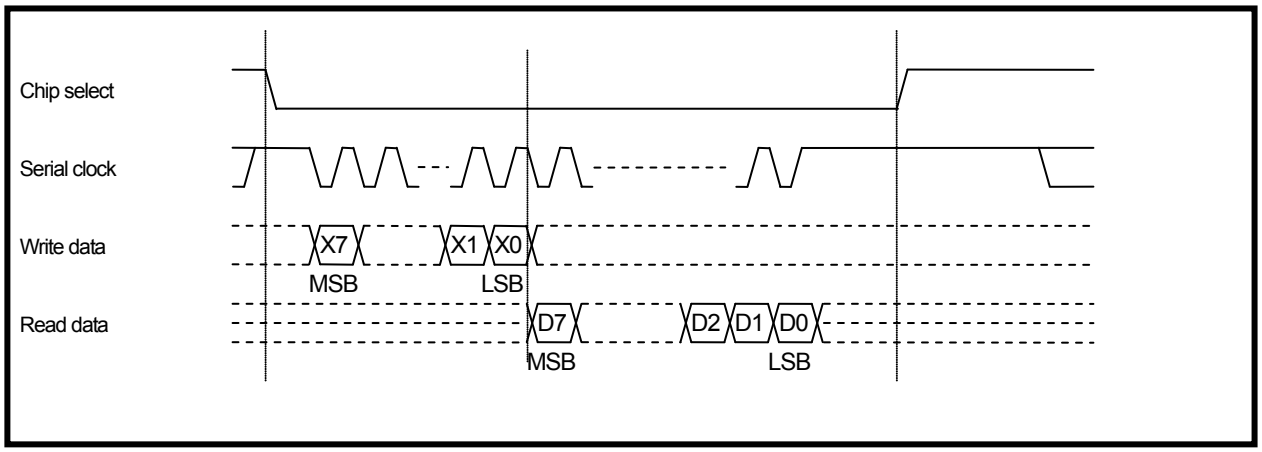

Figure 4-29 SPI format (CODEC IC, single byte read)

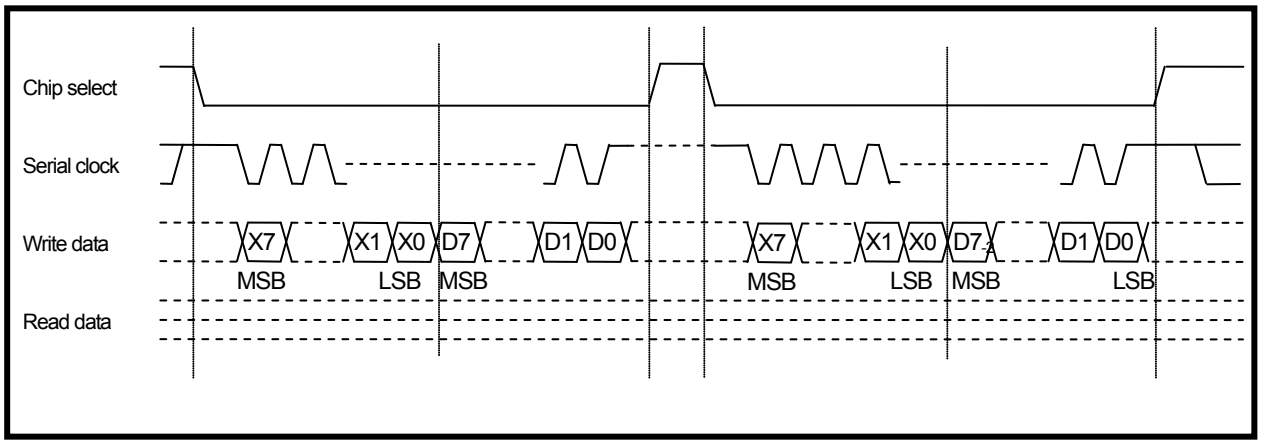

Figure 4-30 SPI format (CODEC IC, single byte write)

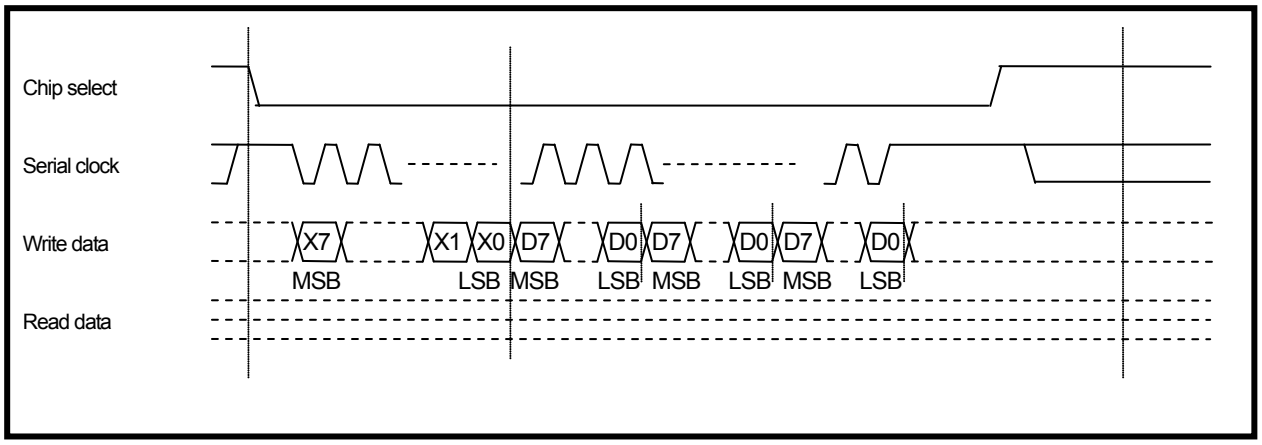

Figure 4-31 SPI format (CODEC IC, continuous byte write)

4.5. Wi-Fi Co-existence Interface

4.5.1. Features

TC35661 has a Wi-Fi co-existence interface. TC35661 can co-operate with the Wi-Fi IC which uses 2.4-GHz band in the same box and is connected by dedicated control lines to prevent from mutual interference.
This interface has the following features:

- Operation voltage: 3.3 V or 1.8 V
- Mode: 2-wire, 3-wire, and 4-wire

4.5.2. Connection Example

The connection examples are shown in Figure 4-32, Figure 4-33, and Figure 4-34.

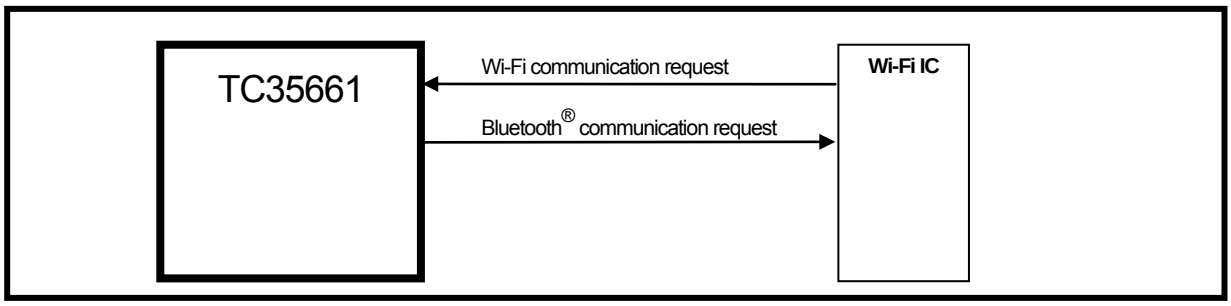

Figure 4-32 Connection example of 2-wire

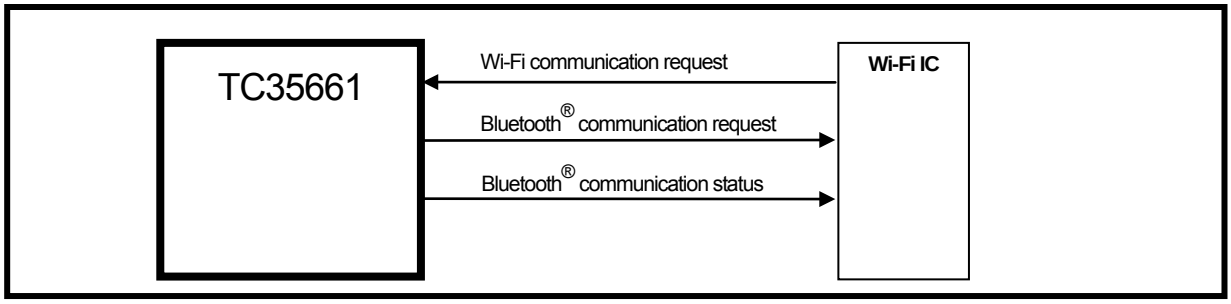

Figure 4-33 Connection example of 3-wire

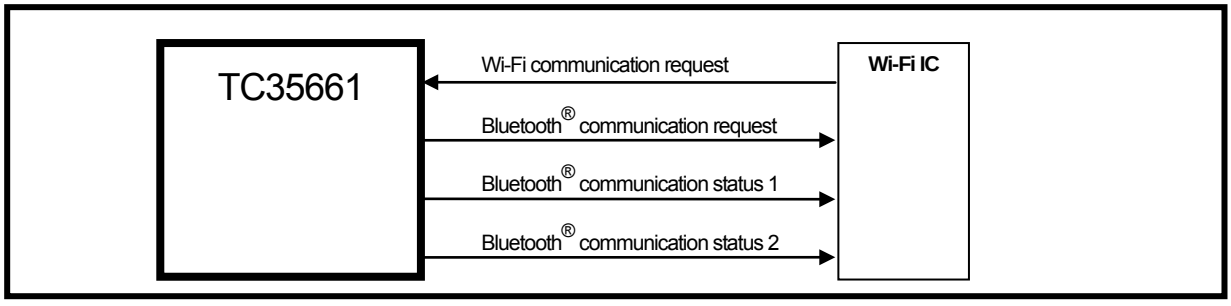

Figure 4-34 Connection example of 4-wire

4.6. Reference Clock Interface

4.6.1. Features

TC35661 has the following features for the reference clock interface.

- Type: Able to connect to a crystal oscillator or TCXO
- Clock frequency: 26 MHz (The frequency uncertainty should be 20 ppm or less in the range of the operation temperature.)

The crystal oscillator should be connected between XOIN pin and XOOUT pin. TC35661 has an internal feed-back resistor between them so that an external feed-back resistor is unnecessary. Please select external capacitors (C_{IN} and C_{OUT}) whose capacitance values should match the crystal oscillator specification. Note that the resistor value and the connection of an external output resistor should be selected according to implementation on a PCB with TC35661.
In case of an external clock, the input TCXO needs XOIN pin only. Please keep XOOUT pin open.

4.6.2. Connection Example

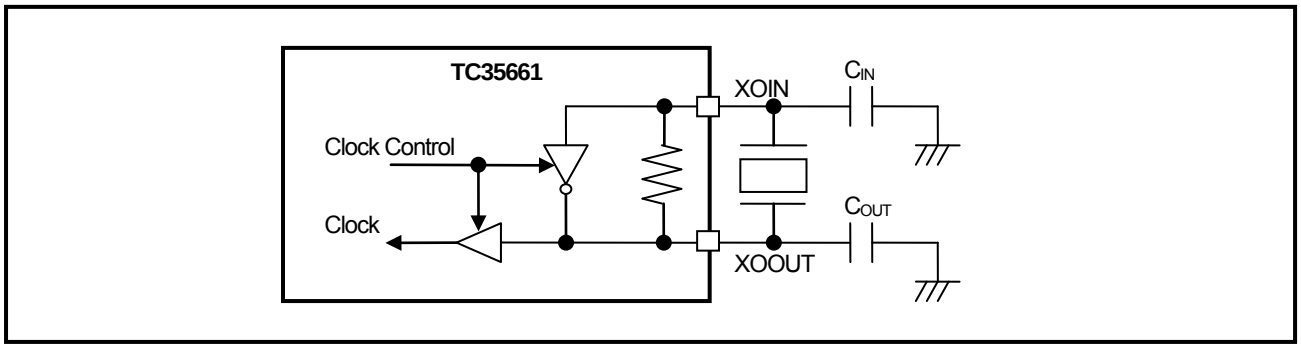

Figure 4-35 Crystal oscillator connection example

4.6.3. Fine Tuning Function for Crystal Oscillator

The crystal oscillator circuit has a built-in capacitor array, and the oscillator frequency can be trimmed by a register bit value. The bit value can take 0 to 31.
Figure 4-36 shows an example of trimming values using 26-MHz crystal oscillator on one of the Toshiba PCB's.
The trimming characteristics depend on a crystal oscillator, external capacitors, resistors, layout of a PCB, and others.

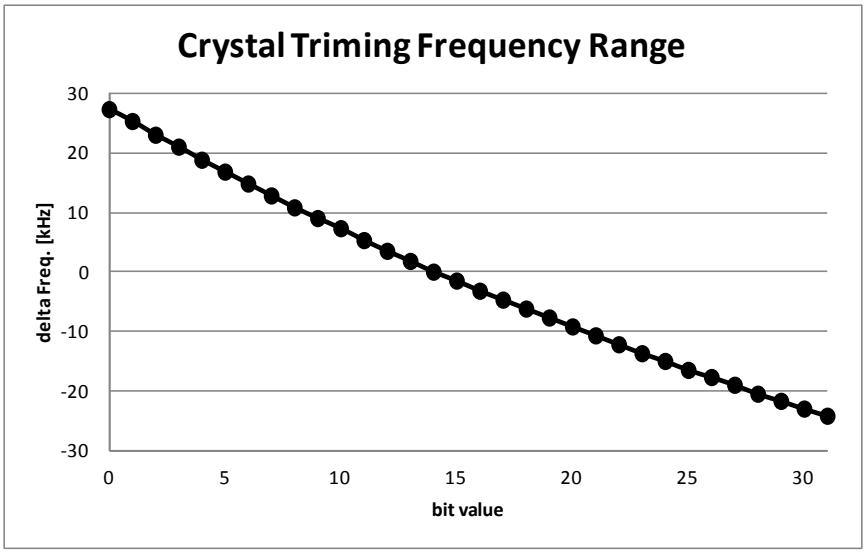

Figure 4-36 Trimming frequency range example

4.7. JTAG Interface

4.7.1. Features

Following shows features of TC35661 JTAG interface.

- Operation voltage: 3.3 V or 1.8 V
- ICE interface
- Chip boundary test function

4.7.2. Connection Example

Figure 4-37 shows an example of the connection between TC35661 and an ICE. For the timing chart of the connection between a JTAG interface and an ICE, refer to the related information produced by ARM.

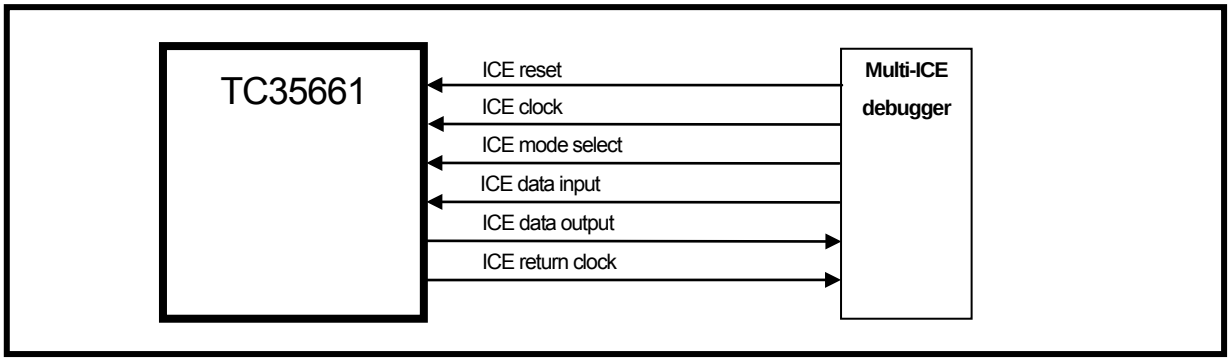

Figure 4-37 ICE connection example

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break-down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions.

Table 5-1 Absolute Maximum Ratings (CDVSS = AVSS* = LVSS33 = 0 V)

Item	Symbol (Power supply category)	Rating		Unit
		Min	Max	
Power supply	DVDD*	-0.3	+3.9	V
	LVDD33*	-0.3	+3.9	V
	AVDD12*	-0.3	+1.8	V
	AVDD33PA	-0.3	+3.9	V
	CVDD	-0.3	+1.8	V
Input voltage	VIN (DVDDA)	-0.3	DVDDA + 0.3	V
	VIN (DVDDB)	-0.3	DVDDB + 0.3	V
	VIN (AVDD12X)	-0.3	AVDD12X + 0.3	V
	GPIO*	-0.3	DVDD* + 0.3	V
	XOIN	-0.3	AVDD12X + 0.3	V
	Other IO pins	-0.3	DVDDA + 0.3	V
Output voltage	VOUT (DVDDA)	-0.3	DVDDA + 0.3	V
	VOUT (DVDDB)	-0.3	DVDDB + 0.3	V
	VOUT (AVDD12X)	-0.3	AVDD12X + 0.3	V
	VOUT (LDOOUT12A)	-0.3	CVDD + 0.3	V
	GPIO*	-0.3	DVDD* + 0.3	V
	XOOUT	-0.3	AVDD12X + 0.3	V
	Other IO pins	-0.3	DVDDA + 0.3	V
Input current	IIN (DVDD*)	-10	+10	mA
Input power	RFIO (AVDD12SG)	—	+6	dBm
Storage temperature	—	-40	+125	°C

Note: AVSS*: AVSS12X, AVSS12SYN, AVSS12ADC and AVSSSG.
DVDD*: DVDDA and DVDDB.
LVDD33*: LVDD33D and LVDD33A.
AVDD12*: AVDD12X, AVDD12SYN and AVDD12SG.
GPIO*: GPIO0 to GPIO18.

5.2. Operation Condition

The operation conditions are the conditions where this product can operate normally with enough good quality. Malfunction may occur when every condition is not kept at operation. Please keep all operation conditions when application equipment using this product is designed.

Table 5-2 Operating condition (CDVSS = AVSS* = LVSS33 = 0 V)

Item	Symbol (Pin Name)	Rating			Unit
		Min	Typ.	Max	
Power supply	DVDDA DVDDB LVDD33* AVDD33PA (Note1)	1.7 2.7	1.8 or 3.3	1.9 3.6	V
	AVDD12SG AVDD12SYN AVDD12X	—	1.2	—	V
	CVDD	—	1.2	—	V
Operating Temperature (Note2)	Ta	-40	+25	+85	°C

Note1: Please refer to different appropriate documents for the connection examples of each power pin.
CVDD is generated by a built-in regulator and supplied internally. Please connect a bypass capacitor to CVDD pin.
AVDD12X is generated by a built-in regulator and supplied internally. Please connect a bypass capacitor to AVDD12X pin.
AVDD12SYN and AVDD12SG are supplied by LDOOUT12A. LDOOUT12A cannot be used for a power supply to another device because it is a 1.2-V output from a built-in regulator.
Please supply the same voltage level at LVDD33* and DVDDA.
Please use less noise power supply voltage.

Note2: This item is the design value.

Note3: AVSS*: AVSS12X, AVSS12SYN, AVSS12ADC and AVSSSG.
LVDD33*: LVDD33D and LVDD33A.

5.3. DC Characteristics

5.3.1. Current consumption

The current consumption is shown in Table 5-3. The values in the table are operating average current consumption values with the recommended connections of the power supply pins in the ambient temperature of 25°C.
Some items in the table are not measured values at the design value.

Table 5-3 Current consumption (CDVSS = LVSS33 = AVSS* = 0 V)

Item	Symbol	Condition		Measured pin (Note2)	Rating			Unit
		Supply voltage	Note		Min	Typ.	Max	
Average current consumed by LVDD33D digital part	IDDDIG	3.3 V or 1.8 V	—	LVDD33D	—	6.5	—	mA
Average current consumed by X'tal OSC digital part	IDDANA	3.3 V or 1.8 V	—	LVDD33A	—	2.0	—	
Average current consumed by analog part during RX	IDDDRX	3.3 V or 1.8 V	—	LVDD33A	—	54	—	
Average current consumed by analog part during TX	IDDDTX	3.3 V or 1.8 V	—	LVDD33A	—	24	—	
		3.3 V or 1.8 V	—	AVDD33PA	—	30	—	
Average current consumed by IO part (Note1)	IDDDIOA	3.3 V or 1.8 V	—	DVDDA	—	0.40	—	
	IDDDIOB	3.3 V or 1.8 V	—	DVDDB	—	0.16	—	
Current consumed during SLEEPCLK, no clock input to XOIN	IDDPDIG	3.3 V or 1.8 V	—	LVDD33D	—	0.028	—	
	IDDPANA	3.3 V or 1.8 V		LVDD33A	—	0.000	—	
	IDDP33PA	3.3 V or 1.8 V		AVDD33PA	—	0.001	—	
	IDDPIO (Note1)	3.3 V or 1.8 V		DVDD*	—	—	—	
Stand-by current consumed during reset operation, no clock input to XOIN and no SLEEPCLK	IDDPDIG	3.3 V or 1.8 V	—	LVDD33D	—	0.37	—	
	IDDPANA	3.3 V or 1.8 V		LVDD33A	—	2.0	—	
	IDDP33PA	3.3 V or 1.8 V		AVDD33PA	—	0.020	—	
	IDDPIO (Note1)	3.3 V or 1.8 V		DVDD*	—	—	—	

Note1: Average current consumed by IO part changes depending on the buffer settings.
Note2: Each measured pin is an LDO output pin in Table 2-2.
Note3: AVSS*: AVSS12X, AVSS12SYN, AVSS12ADC and AVSSSG.
DVDD*: DVDDA and DVDDB.

The DC characteristics of each pin are shown in Table 5-4. The table shows the values in the ambient temperature of 25°C. Some items in the table are not measured values at the design value.

Table 5-4 DC characteristics (CDVSS = LVSS33 = AVSS* = 0 V)

Item	Symbol	Condition		Pin (Note1)	Rating			Unit
		Interface voltage	Others		Min	Typ.	Max	
High level input voltage	VIH	3.3 V	LVCMOS level input	DVDDA and DVDDB categories	0.8 x DVDD*	—	—	V
		1.8 V			0.8 x DVDD*	—	—	
Low level input voltage	VIL	3.3 V	LVCMOS level input	DVDDA and DVDDB categories	—	—	0.2 x DVDD*	
		1.8 V			—	—	0.2 x DVDD*	
High level input current	IIH	DVDD* = Interface voltage	Pull-down Off	DVDDA and DVDDB categories	- 10	—	10	µA
			Pull-down On		10	—	200	
Low level input current	IIL		Pull-up Off		- 10	—	10	
			Pull-up On		- 200	—	- 10	
High level output voltage	VOH	3.3 V	IOH = 1 mA	DVDDA and DVDDB categories	DVDD* - 0.6	—	—	V
			IOH = 2 mA		DVDD* - 0.6	—	—	
			IOH = 4 mA		DVDD* - 0.6	—	—	
		1.8 V	IOH = 1 mA		DVDD* - 0.3	—	—	
			IOH = 2 mA		DVDD* - 0.3	—	—	
			IOH = 4 mA		DVDD* - 0.3	—	—	
Low level output voltage	VOL	3.3 V	IOL = 1 mA	DVDDA and DVDDB categories	—	—	0.4	V
			IOL = 2 mA		—	—	0.4	
			IOL = 4 mA		—	—	0.4	
		1.8 V	IOL = 1 mA		—	—	0.3	
			IOL = 2 mA		—	—	0.3	
			IOL = 4 mA		—	—	0.3	
External reference clock input level (Note2)	VCLK	1.2 V	—	XOIN	—	1.0	—	Vpp
External 32 kHz reference clock high level input	V Sleep CLK H	3.3 V	—	SLEEPCLK	0.8 x DVDDA	—	DVDDA+ 0.2	V
External 32 kHz reference clock low level input	V Sleep CLK L	3.3 V	—	SLEEPCLK	—	—	0.2 x DVDDA	V

Note1: About each pin category, see Table 2-2.

Note2: In case of using an external clock, not use of a crystal oscillator.

Note3: AVSS *: AVSS12X, AVSS12SYN, AVSS12ADC and AVSSSG.

DVDD *: DVDDA and DVDDB.

5.4. Internal Regulator Characteristics

Table 5-5 Internal regulator characteristics

Item	Symbol	Pin	Rating			Unit
			Min	Typ.	Max	
Input Voltage Range	Vin	LVDD33*	2.7	3.3	3.6	V
			1.7	1.8	1.9	V
Output Voltage	Vout1	LDOOUT12A	—	1.2	—	V
	Vout2	AVDD12X	—	1.2	—	V
	Vout3	CVDD	—	1.2	—	V

Note: LVDD33*: LVDD33D and LVDD33A

5.5. RF Characteristics

The following conditons are applied unless special notations are described:

- Ta = 25°C
- DVDDA=DVDDB = LVDD33A =LVDD33D = 3.3 V
- f = 2441 MHz (RF channel = 39 channel)
- fx'tal = 26 MHz (tolerance: +/-2 ppm or less)
- PAOUT1 = +2.0 dBm
- Measurement points: Measuring pins of Toshiba's evaluation board.

5.5.1. Basic Rate

The RF reception characteristics and the RF transmission characteristics in Basic Rate are shown in Table 5-6 and Table 5-7, respectively.

Some items in the tables are not measured values at the design value.

Table 5-6 RF reception characteristics (Basic rate)

Item	Symbol	Conditions	Rating			Unit
			Min	Typ.	Max	
Sensitivity	Sense1	Bit error rate (BER): 0.1 % or less f = 2402 MHz, 2441 MHz, and 2480 MHz	—	-91.0	—	dBm
Max Input level	maxRange1	—	-20	-10	—	dBm
C/I Performance (Note1)	CI_Co	—	—	9	—	dB
	CI + 1 MHz	—	—	-4.5	—	dB
	CI - 1 MHz	—	—	-2.8	—	dB
	CI + 2 MHz	—	—	-36	—	dB
	CI - 2 MHz	—	—	-34	—	dB
	CI + 3 MHz	—	—	-28	—	dB
	CI - 3 MHz	—	—	-43	—	dB
	CI + 4 MHz	—	—	-40	—	dB
	CI + 5 MHz or greater	—	—	-45	—	dB
	CI - 4 MHz or less	—	—	-45	—	dB
Intermodulation	IM	|f1-f2| = 5 MHz	-39	-26	—	dBm
Out of band blocking (Note2)	OBB1	fTX = fRX = 2460 MHz, and 30 to 2000 MHz	-10	0	—	dBm
	OBB2	fTX = fRX = 2460 MHz, and 2 to 2.4 GHz	-27	—	—	dBm
	OBB3	fTX = fRX = 2460 MHz, and 2.498 to 3 GHz	-27	—	—	dBm
	OBB4	fTX = fRX = 2460 MHz, and 3 to 12.75 GHz	-10	0	—	dBm

Note1: Adopts the relaxed specification of Bluetooth® C/I Performance, -17 dB, at -3 MHz, +/-26 MHz and +/-52 MHz.

Note2: Adopts the relaxed specification of Bluetooth® Blocking Performance, -50 dBm, at 820 MHz, 1230 MHz, 2356 MHz, 2564 MHz, 4921 MHz and 4922 MHz.

Note3: Conditions are conformed to the specification of Bluetooth SIG Inc.

Table 5-7 RF transmission characteristics (Basic rate)

Item	Symbol	Conditions	Rating			Unit
			Min	Typ.	Max	
TX Output level (Note1)	PAOUT1	f = 2402 MHz, 2441 MHz, and 2480 MHz	—	2.0	—	dBm
Frequency range	Frange	—	2400	—	2483.5	MHz
20 dB Band Width	20 dBBW	—	—	915	1000	kHz
Frequency deviation1	Dev1(TX)	—	140	162	175	kHz
Frequency deviation2	Dev2(TX)	—	115	132	—	kHz
Frequency deviation ratio	Deviation(TX)	Δf2ave/ Δf1avg	0.8	0.93	—	—
Initial carrier Frequency Tolerance	ICFT	—	-75	-4.7	75	kHz
Frequency drift1 DH1	Fdrift1	DH1 packet	-25	2.5	25	kHz
Frequency drift2 DH5	Fdrift2	DH5 packet	-40	2.5	40	kHz
Frequency drift rate	Fdrift rate	—	-20	6.7	20	kHz/ 50 μs
Adjacent channel power	IBsp1	Frequency offset = 2 MHz	—	-47	-20	dBm
	IBsp2	Frequency offset = 3 MHz or greater	—	-52	-40	

Note1: Connecting the external filter whose insertion loss is 2 dB is supposed.

Note2: Conditions are conformed to the specification of Bluetooth SIG Inc.

5.5.2. Enhanced Data Rate

The RF reception characteristics and the RF transmission characteristics in Enhanced Data Rate are shown in Table 5-8 and Table 5-9, respectively.

Some items in the tables are not measured values at the design value.

Table 5-8 RF reception characteristics (Enhanced Data Rate)

Item		Symbol	Conditions	Rating			Unit
				Min	Typ.	Max	
Sensitivity	π/4DQPSK	Sense2	BER = 0.01 % or less	—	-92.0	—	dBm
	8DPSK	Sense3	BER = 0.01 % or less	—	-85.5	—	
Max Input level	π/4DQPSK	maxRange2	—	-20	—	—	dBm
	8DPSK	maxRange3	—	-20	—	—	
BER Floor Performance	π/4DQPSK	BERfloor2	RFin = -60 dBm	—	0	10^{-5}	BER
	8DPSK	BERfloor3	RFin = -60 dBm	—	0	10^{-5}	
C/I performance (Note1)	π/4DQPSK	CI_Co2	—	—	10.5	—	dB
		CI + 1 MHz_2	—	—	-10	—	
		CI - 1 MHz_2	—	—	-10	—	
		CI + 2 MHz_2	—	—	-37	—	
		CI - 2 MHz_2	—	—	-35	—	
		CI + 3 MHz_2	—	—	-28	—	
		CI - 3 MHz_2	—	—	-45	—	
		CI + 4 MHz_2	—	—	-46	—	
		CI + 5 MHz or greater_2	—	—	-47	—	
		CI - 4 MHz or less_2	—	—	-47	—	
	8DPSK	CI_Co3	—	—	18	—	dB
		CI + 1 MHz_3	—	—	-5	—	
		CI - 1 MHz_3	—	—	-5	—	
		CI + 2 MHz_3	—	—	-32	—	
		CI - 2 MHz_3	—	—	-30	—	
		C I + 3 MHz_3	—	—	-22	—	
		CI - 3 MHz_3	—	—	-40	—	
		CI + 4 MHz_3	—	—	-40	—	
		CI + 5 MHz or greater_3	—	—	-42	—	
		CI - 4 MHz or less_3	—	—	-42	—	

Note1: Adopts the relaxed specification of Bluetooth® C/I Performance, -15 dB for π/4DQPSK and -10 dB for 8DPSK, at -3 MHz, +/-26 MHz and +/-52 MHz.

Note2: Conditions are conformed to the specification of Bluetooth SIG Inc.

Table 5-9 RF transmission characteristics (Enhanced Data Rate)

Item		Symbol	Conditions	Rating			Unit
				Min	Typ.	Max	
Relative Transmit Power		Prtv	—	-4.0	-0.6	1.0	dB
Carrier Frequency Stability	π/4DQPSK	ωi_2	—	-75	-3.4	75	kHz
		ωi+ω0_2	—	-75	-3.1	75	
		ω0_2	—	-10	0.6	10	
	8DPSK	ωi_3	—	-75	-3.4	75	
		ωi+ω0_3	—	-75	-3.1	75	
		ω0_3	—	-10	0.6	10	
Modulation Accuracy	π/4DQPSK	DEVM_R2	RMS DEVM	—	6	20	%
		DEVM_P2	Peak DEVM	—	15	35	
		DEVM_99_2	99 % DEVM, DEVM = 30 % or less	99	100	—	
	8DPSK	DEVM_R3	RMS DEVM	—	6	13	
		DEVM_P3	Peak DEVM	—	15	25	
		DEVM_99_3	99 % DEVM, DEVM = 20 % or less	99	100	—	
In-band Spurious Emission (Note1)	|M-N| = 1	IBSE1	—	—	-39	-26	dB
	|M-N| = 2	IBSE2	—	—	-37	-20	dBm
	|M-N| = 3 or greater	IBSE3	—	—	-44	-40	
Differential Phase Encoding	π/4DQPSK	DFE_2	—	99	100	—	%
	8DPSK	DFE_3	—	99	100	—	

Note1: Connecting external filter whose insertion loss is 2 dB is supposed.

Note2: Conditions are conformed to the specification of Bluetooth SIG Inc.

5.5.3. Bluetooth® Low Energy

The RF reception characteristics and the RF transmission characteristics in Bluetooth® Low Energy are shown in Table 5-10 and Table 5-11, respectively.

Some items in the tables are not measured values at the design value.

Table 5-10 RF reception characteristics (Bluetooth® Low Energy)

Item	Symbol	Condition	Rating			Unit
			Min	Typ.	Max	
Sensitivity	Sense_4	f = 2402 MHz, 2426 MHz, 2440 MHz, and 2480 MHz PER = 30.8 % or less	—	-95.0	—	dBm
Max Input level	maxRange_4	PER = 30.8 % or less	-10	—	—	dBm
PER Report Integrity	PERReport_4	—	50.0	—	65.4	%
C/I performance	CI_Co_4	—	—	12	—	dB
	CI + 1 MHz_4	—	—	3	—	
	CI - 1 MHz_4	—	—	3	—	
	CI + 2 MHz_4	—	—	-34	—	
	CI - 2 MHz_4	—	—	-33	—	
	CI + 3 MHz_4	—	—	-28	—	
	CI + 4 MHz_4	—	—	-37	—	
	CI + 5 MHz or greater_4	—	—	-42	—	
	CI - 3 MHz or less_4	—	—	-42	—	
Intermodulation	IM_4	|f1-f2| = 5 MHz	-50	-38	—	dBm
Blocking Performance	OBB1_4	30 to 2000 MHz	-30	0	—	dBm
	OBB2_4	2003 to 2399 MHz	-35	—	—	
	OBB3_4	2484 to 2997 MHz	-35	—	—	
	OBB4_4	3.0 to 12.75 GHz	-30	0	—	

Note: Conditions are conformed to the specification of Bluetooth SIG Inc.

Table 5-11 RF transmission characteristics (Bluetooth® Low Energy)

Item		Symbol	Condition	Rating			Unit
				Min	Typ.	Max	
TX Output level		PAOUT_4	—	—	2.0	—	dBm
		PDiff_4	Differential between average and peak	—	0.5	—	dB
Carrier Frequency Offset and Drift	Carrier freq. offset	Cfreqoffset_4	fn ; n = 0,1,2,...,k	-150	0	150	kHz
	Drift	Fdrift1_4	f0 - fn ; n = 2,3,4...,k	-50	4.6	50	
	Drift rate	Fdrift rate_4	f1 - f0 , fn - f(n - 5) ;n = 6,7,8,...,k	-20	3.7	20	kHz
Modulation Characteristics	Δf1avg	Dev1_4	Δf1avg	225	247	275	kHz
	Δf2max	Dev2_4	Δf2max	185	218	—	
	Δf2avg/Δf1avg	Devratio_4	Δf2avg/Δf1avg	80	96	—	%
In-band Emission	|M-N|=2	IBE2_4	2 MHz offset	—	-47	-20	dBm
	|M-N|≥3	IBE3_4	≥ 3 MHz offset	—	-53	-30	

Note: Conditions are conformed to the specification of Bluetooth SIG Inc.

5.6. AC Characteristics

5.6.1. UART Interface

Table 5-12 UART Interface AC characteristics

Symbol	Item	Min	Typ.	Max	Unit
tCLDTDLY	Transmission Data ON from CTSX Low level	96	—	—	ns
tCHDTDLY	Transmission Data OFF from CTSX High level	—	—	2	byte
tTXDIV	Transmission Data Tolerance (Note)	-0.756	—	+0.756	%
tRLDTDLY	Received Data ON from RTSX Low level	0	—	—	ns
tRHDTDLY	Received Data OFF from RTSX High level	—	—	8	byte
tRXDIV	Received Data Acceptable Tolerance (Note)	-2.0	—	+2.0	%

Note: This is the tolerance of the internal baud rate for each item.

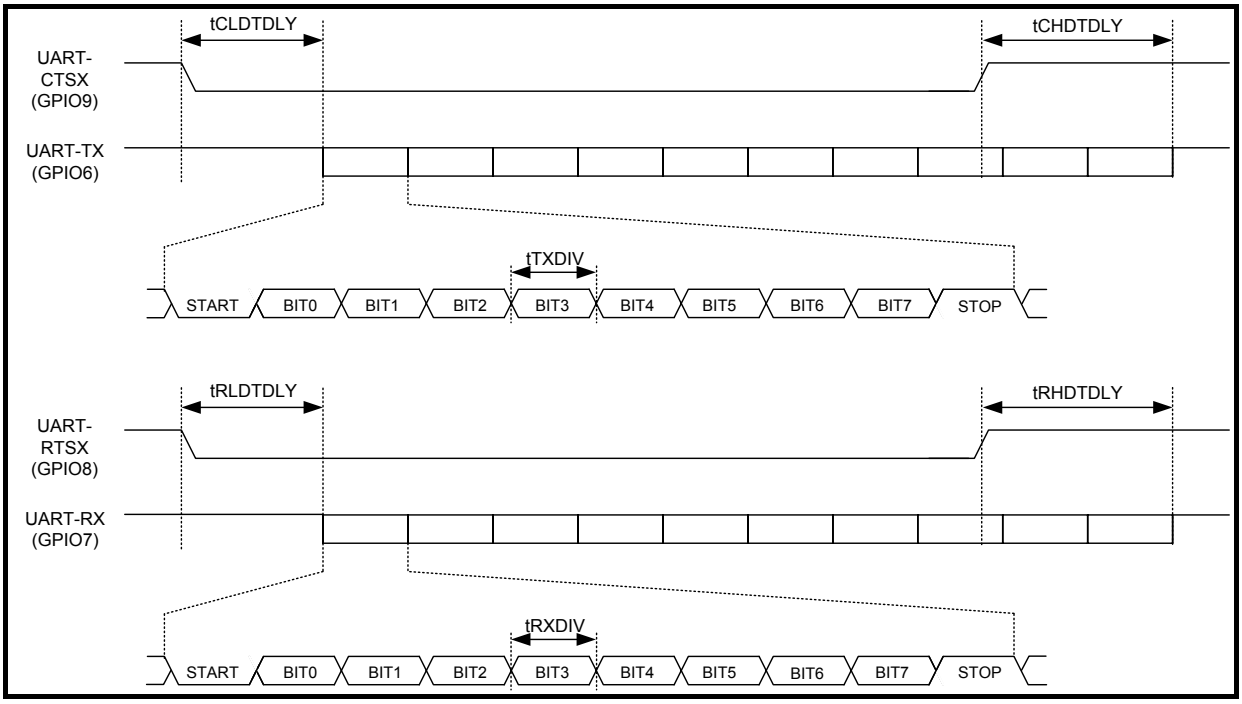

Figure 5-1 UART Interface Timing Diagram

5.6.2. I²C Interface

5.6.2.1. Normal Mode

Table 5-13 I²C Interface Normal mode AC Characteristics

Symbol	Item	Min	Typ.	Max	Unit
tDATS	Data set-up time	250	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	3450	ns
tACKVD	ACK validity period	—	—	3450	ns
tSTAS	Restart condition set-up time	4700	—	—	ns
tSTAH	Restart condition hold time	4000	—	—	ns
tSTOS	Stop condition set-up time	4000	—	—	ns
tBUF	Bus open period from Stop condition to Start condition	4700	—	—	ns
tr	Rise time	—	—	1000	ns
tf	Fall time	—	—	300	ns
tHIGH	Serial clock period of High	4000	—	—	ns
tLOW	Serial clock period of Low	4700	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

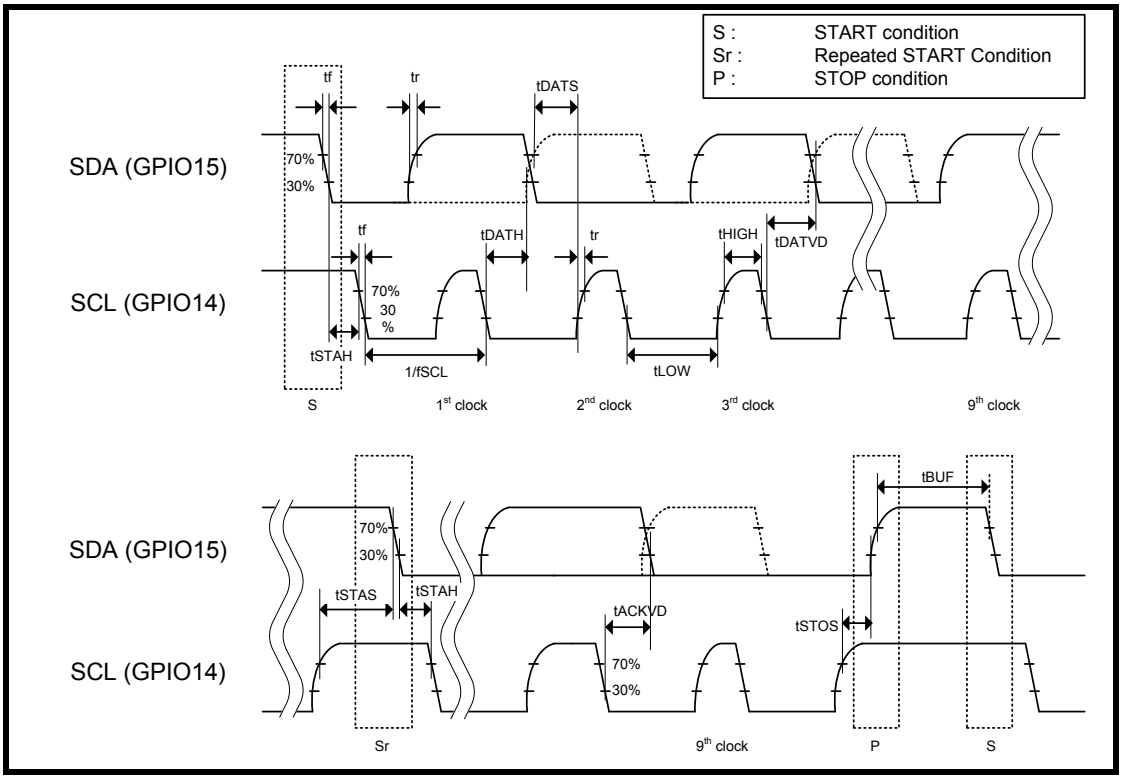

Figure 5-2 I²C Interface Normal mode Timing diagram

5.6.2.2. Fast mode

Table 5-14 I²C Interface Fast mode AC Characteristics

Symbol	Item	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	900	ns
tACKVD	ACK validity period	—	—	900	ns
tSTAS	Restart condition set-up time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition set-up time	600	—	—	ns
tBUF	Bus open period from Stop condition to Start condition	1300	—	—	ns
tr	Rise time	20 + 0.1 Cb	—	300	ns
tf	Fall time	20 + 0.1 Cb	—	300	ns
tSP	Spike pulse width that can be removed	0	—	50	ns
tHIGH	Serial clock period of High	600	—	—	ns
tLOW	Serial clock period of Low	1300	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

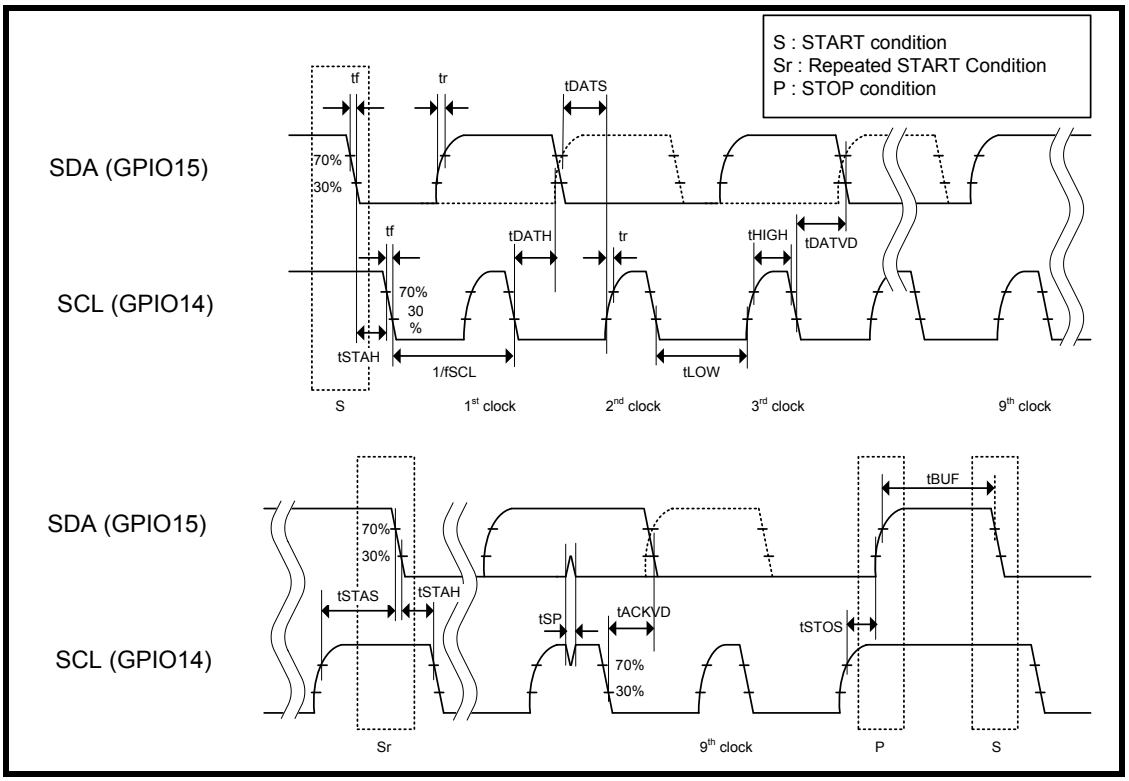

Figure 5-3 I²C Interface Fast mode Timing diagram

6. System Configuration Example

6.1. System Configuration Example

Figure 6-1 shows an example of system configuration.
[Case]
Host interface = UART, Reference Clock = OSC Connection, external EEPROM connection

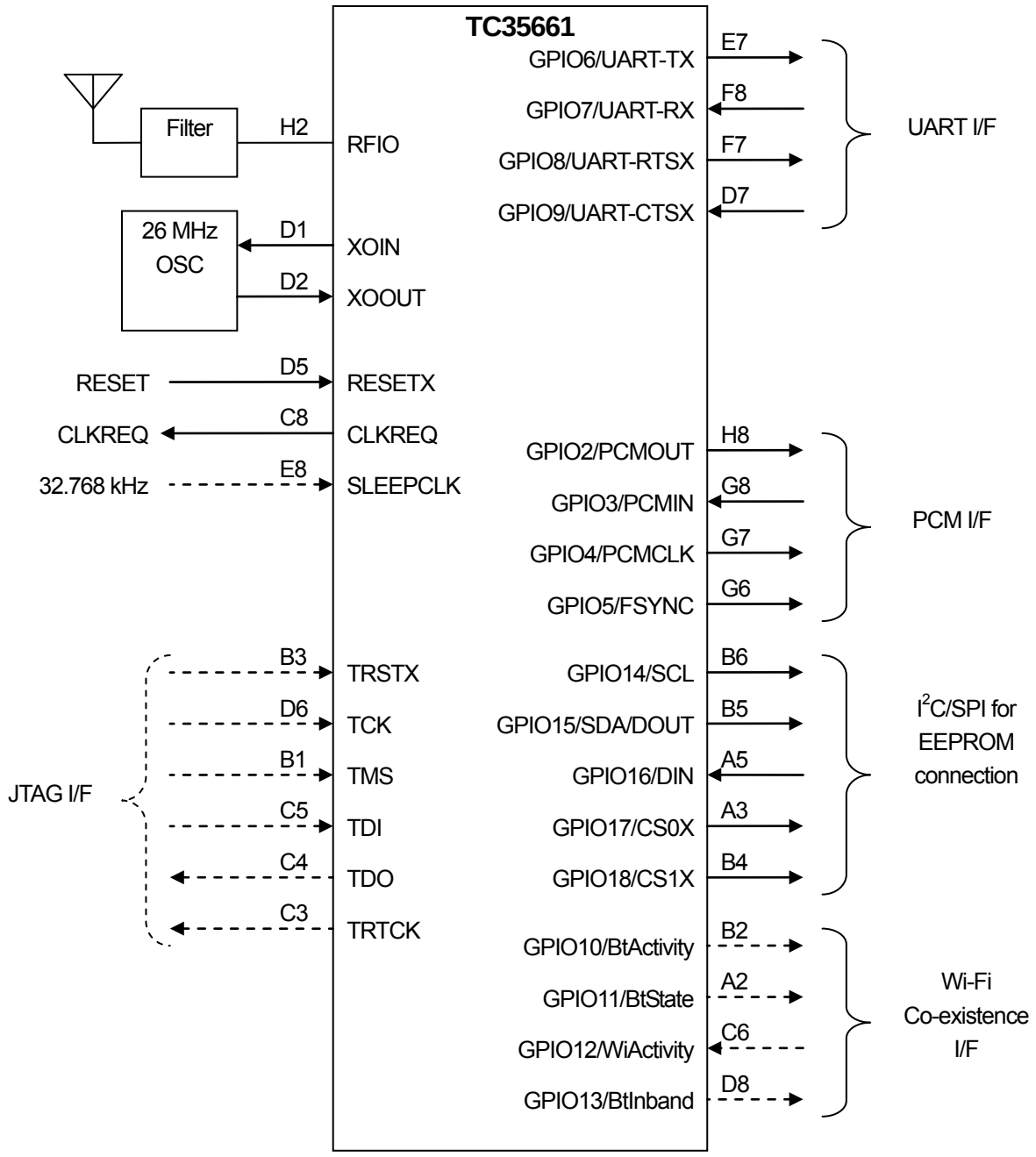

Figure 6-1 Connection example

6.2. Application Circuit Example

The application circuits shown in this document are provided for reference purpose only. Especially, thorough evaluation is required on the phase of mass production design. Toshiba dose not grant the use of any industrial property rights with these examples of application circuits.

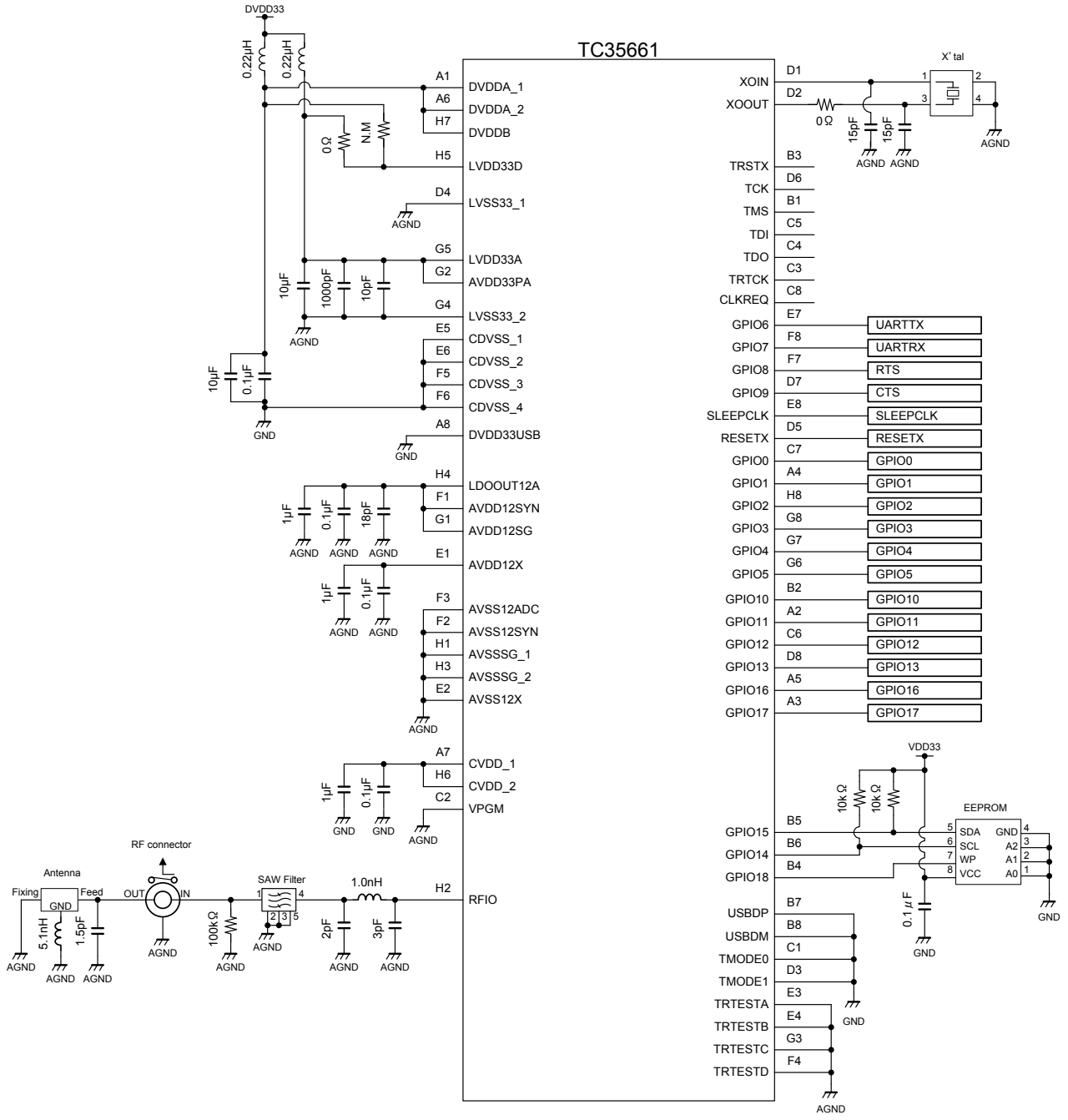

Figure 6-2 Application Circuit Example

7. Package

7.1. Package Outline

Unit: mm

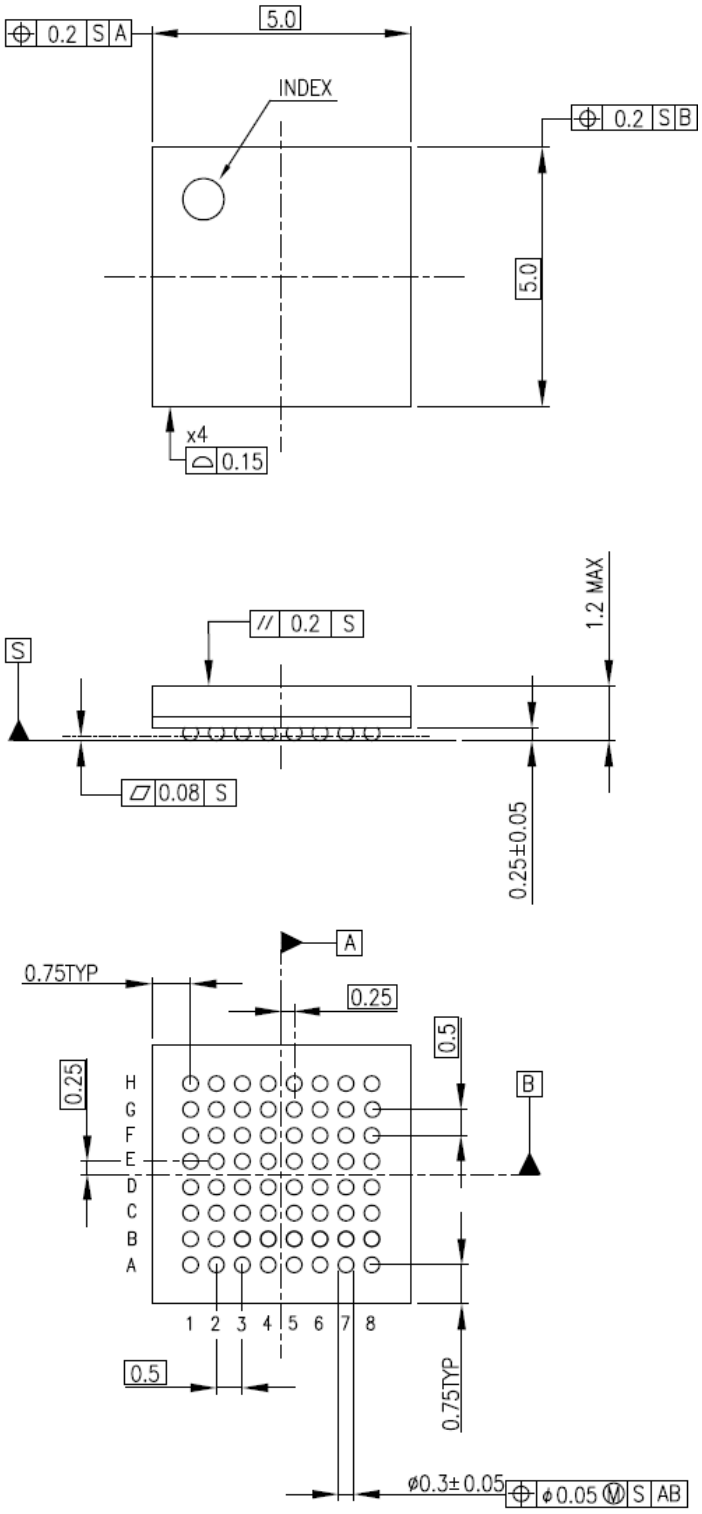

Figure 7-1 Package outline (P-TFBGA64-0505-0.50)

Weight: 0.049 g (typ.).

Note: This figure is for explanation. For the dimensions and the others that are not listed in the figure, please contact our representative.

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