TC35670FTG Bluetooth™ LE + NFC-Tag IC

Overview Document

Contents

1. General Description

1.1. Product Concept

TC35670FTG is IC based on a 2.4GHz wireless-communications Bluetooth™ V4.0 Low Energy standard, and has a built-in non-volatile memory (EEPROM) which can be accessed by communication based on NFC Forum Type 3 Tag standard. It includes an RF analog part and a Baseband digital part., provides Bluetooth™ HCI (Host Control Interface) function and LE (Low Energy) function specified in Bluetooth™ Specifications.

Connected with an external host processor, TC35670 easily realizes low energy consumption applications. And also it realizes stand-alone type low energy consumption applicatios with its internal ADC & GPIO functions.

The internal EEPROM is access-available through the wireless and wire interfaces and has 1520 byte general user areas. Access attribute can be set.

Data can be translated from the wireless interface to the wire interface or from the wire interface to the wireless interface by temporarily storing received data in RAM (Through mode function).

1.2. Features

- Compliant with Bluetooth™ Ver4.0 Low Energy
  - ✧ Built-in Bluetooth™ Baseband digital core, Built-in Bluetooth™ RF analog core
  - ✧ Built-in ARM7TDMI-S™ core

  Achieve low power consumption by a two-step switching of the operating clock frequency 1MHz / 13MHz
  - ✧ On-chip ProgramMask-ROM (320 KB)
  - ✧ On-chip Work RAM for Bluetooth™ Baseband process (96 KB), On-chip RAM for application program storing (32 KB)
  - ✧ Supports patch program loader function
  - ✧ Suports sleep, deep sleep function
- Built inEEPROM
  - ✧ Wireless interface based on NFC Forum Type 3 Tag standard

    Automatic detection of transmission speed 212kbps and 424kbps
  - ✧ I2C wire interface: Maximum operational clock 400kHz
  - ✧ General user area: 1520 bytes

    High reliable writing function: Protecting against defective data
  - ✧ Writing time: 5ms(typ.)
  - ✧ 1bit error automatic correction , CRC automatic addition, and error detection of read data
  - ✧ Security: Mutual authentication with Message authentication code (MAC)

    Writing prohibition, reading/writing, reading after authentication, writing after authentication, writing with MAC
  - ✧ External authentication is stored for the wireless interface and wire interface separately.
- General Purpose IO (8 pins)
  - ✧ General SPI / I2C / UART interface (1ch/General Purpose IO)
  - ✧ Bluetooth host CPU interface:UART (2.4 kbps to 921.6 kbps/General Purpose IO)
  - ✧ Built-in general purpose ADC : GPADC 2ch(General Purpose IO/ADC1ch for internal VDD detection)
  - ✧ Wake-up function from sleep (1ch/general Purpose IO)
  - ✧ PWM interface(1ch,/General Purpose IO)
- Base Clock Input
  - ✧ Built-in oscillator for external 26MHz resonator connection
  - ✧ Sleep clock(32.768kHz) External input supported/ Internal oscillation SiOSC
- Built-in DCDC converter and LDO
  - ✧ Wide range of input power supply voltage supported (1.8 to 3.6 V, Low voltage detection for battery, DCDC start from 1.9V)
- Package: QFN40-0606-0.50 [40pin,6x6mm2, 0.5mmpitch, 0.9mm thickness]

The NFC-F wireless interface is referred to the below standards.

- JIS X 6319-4: Specification of implementation for integrated circuit (s) cards - Part 4: High speed proximity cards
- ISO/IEC 18092: Information technology - Telecommunications and information exchange between systems - Near Field Communication - Interface and Protocol-1(NFCIP-1)
- NFC Forum: http://www.nfc-forum.org/

2. Pin Function

2.1. Pin Assignment (Top View) ver.QFN40-0606-0.50

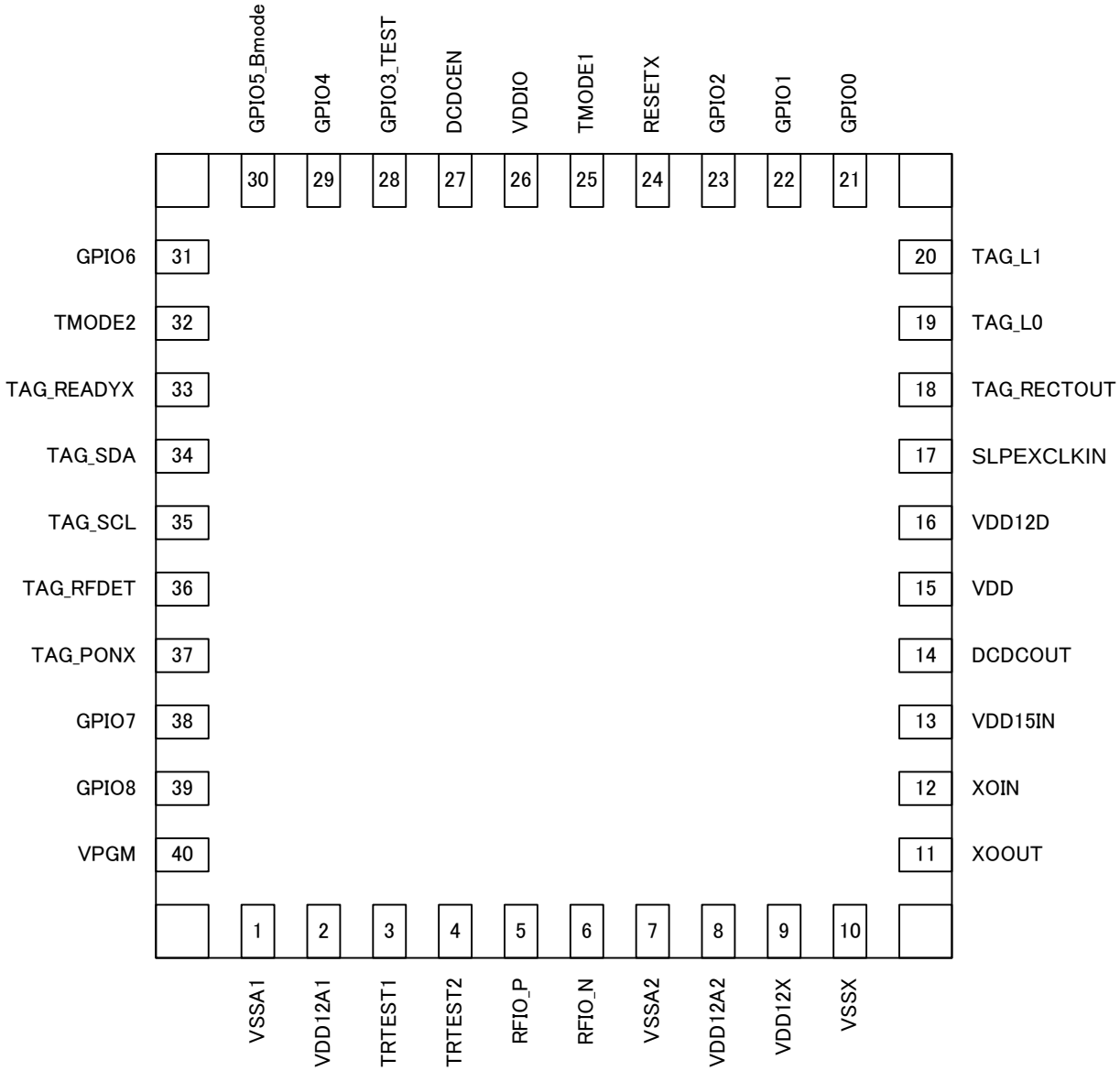

Figure 2-1 Pin Assignment (Top View)

2.2. Pin Function Descriptions

Table 2-1 shows attributes, input/output states for operating modes and descriptions for pin functions. Table 2-4 shows descriptions about power supply pins.

Table 2-1 Pin Functions

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
Reset interface				
RESETX	24	VDDIO IN Schmitt	IN	Hardware reset input pin. System initialization signal whose low level indicates reset.
Mode setting				
DCDCEN	27	VDD IN Schmitt	IN	DCDC enable pin. High level: internal DCDC is ON Low level: internal DCDC is OFF
Reference clock interface				
XOIN	12	VDD12X IN OSC	IN	Oscillator (OSC) or TCXO input pin for Baseband and RF reference clock (26 MHz) pin. OSC's frequency accuracy should be less than or equal to 50 ppm. A feedback resistor is built in between XOIN pin and XOUT pin. This pin needs to be connected with the appropriate resistor and capacitor for the connected X'tal.
XOOUT	11	VDD12X OUT OSC	OUT	Oscillator output for Baseband / RF reference clock (26 MHz) pin A feedback resistor is built in between XOIN pin and XOUT pin. This pin needs to be connected with the appropriate resistor and capacitor for the connected X'tal.
SLPEXCLKIN	17	VDDIO IN/OUT OSC	IN	Sleep clock input pin (32.768 kHz) for low power consumption operation. Frequency accuracy of sleep clock should be less than or equal to 500 ppm. When external clock is not supplied, this pin needs to be connected to the GND.
RF interface				
RFIO_P RFIO_N	5 6	VDD12A IN/OUT Analog	Hi-z	RF differential I/O pin. Connection example of RF signal is at accompanying sheet which describes System Configuration Example.
TAG interface				

Pin name	Pin No	Attribute VDD category Direction Type	Condition Default (during reset)	Functional description
TAG_L0 TAG_L1	19 20	- IN/OUT Analog	Hi-z	TAG antenna coil connection pin Connect antenna coil.
TAG_READYX	33	VDDIO OUT	OUT	TAG through mode ready output pin When data of Through mode is received through the wireless interface, this pin outputs low level. If response data is received through the wire interface, the level turns to the high level.
TAG_SDA	34	VDDIO IN/OUT Schmitt	IN	I2C data pin for wire interface of TAG. This pin can act as SDA terminal in I2C. If this function is not used, implement open process to this pin.
TAG_SCL	35	VDDIO OUT Schmitt	OUT Hi-z	I2C clock pin for wire interface of TAG. If this function is not used, this pin should be open circuit.
TAG_RFDET	36	VDD OUT	Pull-down OUT	TAG carrier detection pin. If no carrier, this pin becomes low level by Pull-down resistor. If wireless carrier is detected, this pin is cut off from Pull-down resistor and becomes high level.
TAG_PONX	37	VDDIO IN Schmitt	IN	TAG power supply control and wire interface enable pin In case of turning on power supply switch and using the wire interface, input low level. High level leads to turning off the power supply switch and disabling the wire interface.
General purpose I/O port				
GPIO0	21	VDDIO IN/OUT PullReg Schmitt	Hi-z	General purpose I/O pin 0. During a reset and right after the reset release, this pin is set input-disabled. After the reset release, the firmware configures the pin function as wake up pin or general purpose IO pin. For sleep and deep sleep modes, after settings by firmware and external input, wake up function can be selected, which activates the chip. When not used, this pin should be pulled down to the ground with 100 kohm resistor.

Pin name	Pin No	Attribute VDD category Direction Type	Condition Default (during reset)	Functional description
GPIO1	22	VDDIO IN/OUT PullReg Schmitt	Analog	ADC input/General purpose I/O pin1 During a reset, this pin is set input-disabled. After the reset is released, this pin is input-disabled with pull-up resistor off. After the reset release, the firmware configures pull-up or pull-down resistors, and the pin can function as general ADC input pin AIN0 or general purpose IO pin. When not used, this pin should be pulled down to the ground.
GPIO2	23	VDDIO IN/OUT PullReg Schmitt	Analog	ADC input/General purpose I/O pin 2 During a reset, this pin is set input-disabled. After the reset is released, this pin is input-disabled with pull-up resistor off. After the reset, the firmware configures pull-up or pull-down resistors, and the pin can function as general ADC input pin AIN1, PWM output pin PWM0, or general purpose IO pin. When not used, this pin should be pulled down to the ground.
GPIO3_TEST	28	VDDIO IN/OUT PullReg Schmitt	Pull-up	General purpose I/O pin 3. During a reset, this pin is set input-disabled with pull-up resistor on. Low input for this pin during power up sequence after reset enables Toshiba test mode. Please keep this pin high during power up sequence after reset. After reset, firmware configures pull-up or pull-down resistors, and the pin can function as UART data transfer pin UART1-TX (UART2-TX), SPI data output DOUT, or general purpose IO pin. When not used, this pin should be opened.

Pin name	Pin No	Attribute VDD category Direction Type	Condition Default (during reset)	Functional description
GPIO4	29	VDDIO IN/OUT PullReg Schmitt	Hi-z	General purpose I/O pin 4. During a reset, the pull up resistor is on, and the input is disabled. After reset, firmware configures the pin.When not used, this pin should be opened. GPIO pins can be assigned to UART I/Fs, serial memory I/Fs or some other functions by firmware in ROM or command from external Host. Please refer to Table 2-2, 2-3.
GPIO5_Bmode	30	VDDIO IN/OUT PullReg Schmitt	Pull-up	General purpose I/O pin 5. During a reset, the pull up resistor is on, and the input is disabled. High input during power up sequence after reset enables host program download mode (for more information, please refer to the firmware document). After normal power up sequence with low input during reset release after reset, firmware configures pull-up or pull-down resistors and the pin can function as UART request to send pin UART1-RTSX, UART data transfer pin UART1-TX (UART2-TX), SPI chip select output pin SCS, or general purpose IO pin. When not used, this pin should be opened.
GPIO6 GPIO7 GPIO8	31 38 39	VDDIO IN/OUT PullReg Schmitt	Hi-z	General purpose I/O pin 6~8. During a reset, the pull up resistor is on, and the input is disabled. After reset, firmware configures the pin. When not used, this pin should be opened. GPIO pins can be assigned to UART I/Fs, serial memory I/Fs or some other functions by firmware in ROM or command from external Host. Please refer to Table 2-2, 2-3.
IC test interface				
TMODE1 TMODE2	25 32	VDDIO IN Schmitt	-	Test mode setting pins These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
TRTEST1 TRTEST2	3 4	VDD12A IN/OUT Analog	-	Analog test pins. These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.
TAG_RECTOUT	18	- OUT Analog	Hi-z	TAG rectification circuit output pin Output from the rectification circuit can be monitored. If this function is not used, this pin should be open circuit.

2.3. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs or some other functions by firmware in ROM or command from external Hosts. Table 2-2 shows available functions for each GPIO pin, and Table 2-3 examples of GPIO function settings.

Table 2-2 Available functions for GPIO

Pin	Analog input	Function 1	Function 2	Function 3	Function 4	Function 5
GPIO0	-	GPIO1 Digital I/O	WakeUp Input	-	-	-
GPIO1	ADC0Input	GPIO Digital I/O	-	-	-	-
GPIO2	ADC1Input	GPIO Digital I/O	PWM0 Output	-	-	-
GPIO3_TEST	-	GPIO Digital I/O	UART1-TX Output	-	SPI-DOUT Output	UART2-TX Output
GPIO4	-	GPIO Digital I/O	UART1-RX Input	-	SPI-DIN Input	UART2-RX Input
GPIO5_Bmode	-	GPIO Digital I/O	UART1-RTSX Output	UART2-TX Output	SPI-SCS Output	UART1-TX Output
GPIO6	-	GPIO Digital I/O	UART1-CTSX Input	UART2-RX Input	SPI-SCLK Output	UART1-RX Input
GPIO7	-	GPIO Digital I/O	-	I2C-SCL Output	SPI-DOUT Output	-
GPIO8	-	GPIO Digital I/O	-	I2C-SDA I/O	SPI-DIN Input	-

Table 2-3 GPIO function list (example)

Pin name	Basic example	UART1+UART2+I2C Example	SPI+I2C Example	UART＋SPI Example
GPIO0	WakeUp	WakeUp	WakeUp	WakeUp
GPIO1	ADC- AIN0	ADC- AIN0	ADC- AIN0	ADC- AIN0
GPIO2	ADC-AIN1 / PWM0	ADC-AIN1 / PWM0	ADC-AIN1 / PWM0	ADC-AIN1 / PWM0
GPIO3_TEST	UART1-TX	UART1-TX	SPI-DOUT	UART1-TX
GPIO4	UART1-RX	UART1-RX	SPI-DIN	UART1-RX
GPIO5_Bmode	UART1-RTSX	UART2-TX	SPI-SCS	SPI-SCS
GPIO6	UART1-CTSX	UART2-RX	SPI-SCLK	SPI-SCLK
GPIO7	I2C-SCL	I2C-SCL	I2C-SCL	SPI-DOUT
GPIO8	I2C-SDA	I2C-SDA	I2C-SDA	SPI-DIN

There are other functions than the above examples. About the detail of the other functions, refer to the firmware specification.

2.4. Power Supply Pins

Table 2-4 shows the attributes and descriptions of power supply pins for normal operations.

Details available under NDA.

Table 2-4 Power supply pins

3. System Configuration Example

This figure shows an example of system configuration.

3.1. In case of Host CPU connection

Details available under NDA.

Figure 3-1 Example of TC35670FTG system configuration (HOST CPU connetion)

4. Package outline

4.1. Outline dimensional drawing

Unit: mm

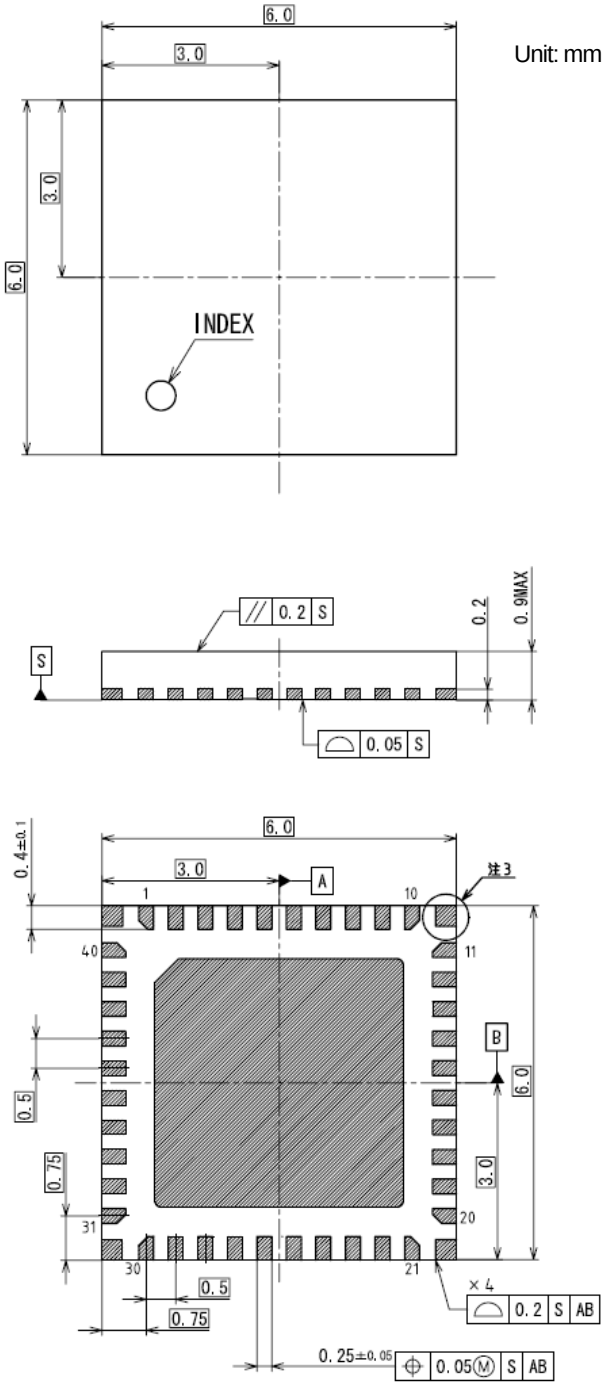

Figure 4-1 Package outline (QFN40-P-0606-0.5)

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

End of document.