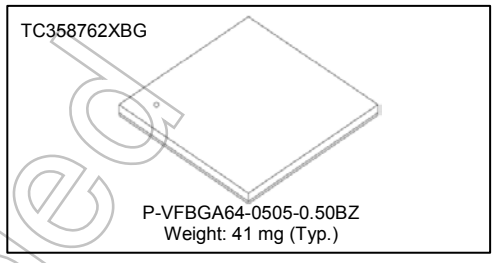
CMOS Digital Integrated Circuit Silicon Monolithic

TC358762XBG

Mobile Peripheral Devices



Overview

TC358762XBG chip de-serializes the stream into a parallel one. The parallel output bus can be either a DPI or a DBI bus. The usage of either DPI or DBI bus is mutually exclusive.

The DSI host controls/configures TC358762XBG chip via DSI's Generic Long Write packets. The host controls (commands) the peripheral display device by sending DSI packets to TC358762XBG. TC358762XBG routes the commands either through DBI host, SPI master or DBI-C host interface, I/F, block to the peripheral device. TC358762XBG supports both DCS and generic commands. The commands output through these interfaces are intended for the peripheral display device to interpret and execute; TC358762XBG does not interpret them, except a few DCS commands mentioned explicitly in this document.

TC358762XBG supports bi-directional DSI link. The host reads TC358762XBG's registers via DSI's Generic Read (2 parameter) packets. Host can also access the status registers of peripheral display device attached to TC358762XBG by issuing read commands. The read data is returned to host via DSI's reverse direction Low Power packets in Data Lane 0.

Depending on the output I/F ports chosen; TC358762XBG can be configured to operate with various peripheral display devices.

Features

- Standard followed:
  - ✧ MIPI DSI version 1.01, Feb 2008
  - ✧ MIPI D-PHY version 0.9, Oct 2007
  - ✧ MIPI DPI version 2.0, Sep, 2005
  - ✧ MIPI DBI-2 version 2.00, Nov 2005
  - ✧ MIPI DCS Command version 1.02, Dec 2008
- DSI Receiver
  - ✧ Dual Data Lane DSI Link with Bi-direction support at Data Lane 0
  - ✧ Maximum speed at 800 Mbps/lane
  - ✧ Video input data formats: RGB-565, RGB-666 and RGB-888
  - ✧ Video input frame rates: Up to 60 fps for WXGA (1366 × 768)
  - ✧ Support various DSI packet types
  - ✧ Provide the path for DSI host/transmitter to control TC358762XBG and its attached Display Device
- DPI Host
  - ✧ Bus speed up to 75 MHz burst rate with data rate up to 216 Mbytes/s
  - ✧ Support the following pixel formats:
    - RGB666 18 bit per pixel
    - RGB666 loosely packed 18 bit per pixel
    - RGB565 16 bit per pixel
    - RGB565 loosely packed 16 bit per pixel
    - RGB888 24 bit per pixel
      - ➢ With the Toshiba Magic Square algorithm, an RGB666 18-bit or 16-bit LCD panel can produce a display equivalent to that of an RGB888 24-bit LCD panel with up to 16-million colors
      - ➢ Programmable output polarity
      - ➢ Support up to frame size 1366 × 768 at 60 fps
- DBI Host
  - ✧ Read/Write Data/Command from the external DBI slave device
  - ✧ Support DCS commands, which is compliant with MIPI DBI-B standard
  - ✧ Support Intel 80xx CPU I/F with either 8-bit or 16-bit commands
  - ✧ Programmable Output Data Format and Bus Width
    - 8 bit Bus, RGB 565 (2 cycles/pixel)
    - 8 bit Bus, RGB 666 (3 cycles/pixel)
    - 8 bit Bus, RGB 888 (3 cycles/pixel)
    - 9 bit Bus, RGB 666 (2 cycles/pixel)
    - 16 bit Bus, RGB 565 (1 cycles/pixel)
    - 16 bit Bus, RGB 666 (3 cycles/2 pixel) note1
    - 16 bit Bus, RGB 888 (3 cycles/2 pixel) note1
    - 18 bit Bus, RGB 666 (1 cycles/pixel)
    - 24 bit Bus, RGB 888 (1 cycles/pixel)
      - ➢ Support up to 864×480 at 60 fps (or 1280×720 at 30 fps)

- SPI Master
  - ✧ 4-pin SPI master I/F, CSX[1:0], CLK, DI and DO
  - ✧ Support two SPI slaves
  - ✧ Data Rate up to 10 Mbps
  - ✧ The main purpose of this port is used to configure DPI slave display devices
  - ✧ Half Duplex data transfer support
- DBI-C host
  - ✧ 3-pin DBI-C host I/F, CSX, SCL and SDA
  - ✧ Shared pins with SPI I/F, only one can be active at a given time
  - ✧ Data Rate up to 10 Mbps
  - ✧ Programmable read delay
- I^2C compliant interface Slave Port
  - ✧ Data Rate up to 400 kHz
  - ✧ External I^2C master can access TC358762XBG internal registers via this port
  - ✧ Address auto increment is supported
  - ✧ TC358762XBG Slave Port address is “0001011”
  - ✧ During I^2C slave cycle, DSI host must not transmit any new DSI packet to TC358762XBG.
- A 1024 × 24 dual port Video Buffer is used to buffer the video data received from DSI link.
- System Operation
  - ✧ Register programming through DSI link via Generic Write Long packets.
  - ✧ Register read through DSI link via Generic Read, 2 parameters packets.
  - ✧ Write to WCMQUE and RCMDQUE registers enable host to configure and control peripheral display device
  - ✧ DCS commands are routed to peripheral display device to interpret
  - ✧ Provide Tearing Effect Trigger message after receiving set_tear_on command
- Clock source:
  - ✧ External reference clock: recommended 6 - 40 MHz
  - ✧ A programmable PLL is used to adjust the output video clock:
    - In DPI output mode with DSI link burst data, adjust output clock to the desired pixel clock frequency to assure no video is lost due to video buffer over/under flow.
    - In DBI output mode, adjust output clock frequency fast enough to prevent video buffer from over flow.
- Power supply
  - ✧ MIPI D-PHY: 1.2V
  - ✧ I/O: 1.8V – 3.3V (all IO pins must be same power level)
  - ✧ Core: 1.2V
- Power Consumption
  - ✧ Sleep State
    - PLL OFF mode - Sleep mode (DSI-CLK stops toggle)
      - ➢ IOs: 0.05 µW
      - ➢ CORE: 23 µW
      - ➢ D-PHYs: 3 mW
      - ➢ PLLs: Off (PLL power – 0V)
    - PLL ON mode - Sleep mode (DSI-CLK goes to ULPS state, REFCLK toggles)
      - ➢ IOs: 0.15 µW
      - ➢ CORE: 23 µW
      - ➢ D-PHYs: 9 µW
      - ➢ PLLs: 28 µW
  - ✧ Normal Operation:
    - PLLOFF mode (480×864 @60fps, DSI-CLK: 400 MHz – 2 data lanes)
      - ➢ 18 mW
      - ➢ PLLON mode (480×864 @60fps, DSI-CLK: 400 MHz, PLLCLK: 50.28MHz, PCLK=PLL/2)
      - ➢ 19 mW
- Packaging
  - ✧ BGA 64 pins
  - ✧ 5.0mm × 5.0mm × 1mm
  - ✧ 0.5mm ball pitch

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1. MIPI D-PHY, “MIPI Alliance Specification for D-PHY Version 0.91.00 – r0.01 14-March-2008"
2. MIPI Alliance Standard for DSI version 1.01, Feb 2008
3. MIPI Alliance Standard for DPI version 2.0, Sep, 2005
4. MIPI Alliance Standard for DBI-2 version 2.00, Nov 2005
5. MIPI Alliance Standard for DCS Command version 1.02, Dec 2008

1. Introduction

This Functional Specification defines operation of a de-serializer chip, TC358762XBG. The serial data stream is supplied by the baseband processor via the DSI 1.01 interface. TC358762XBG chip de-serializes the stream into a parallel one. The parallel output bus can be either a DPI or a DBI bus. The usage of either DPI or DBI bus is mutually exclusive.

The DSI host controls/configures TC358762XBG chip via DSI's Generic Long Write packets. The host controls (commands) the peripheral display device by sending DSI packets to TC358762XBG. TC358762XBG routes the commands either through DBI host, SPI master or DBI-C host interface, I/F, block to the peripheral device. TC358762XBG supports both DCS and generic commands. The commands output through these interfaces are intended for the peripheral display device to interpret and execute; TC358762XBG does not interpret them, except a few DCS commands mentioned explicitly in this document.

TC358762XBG supports bi-directional DSI link. The host reads TC358762XBG's registers via DSI's Generic Read (2 parameter) packets. Host can also access the status registers of peripheral display device attached to TC358762XBG by issuing read commands. The read data is returned to host via DSI's reverse direction Low Power packets in Data Lane 0.

Depending on the output I/F ports chosen; TC358762XBG can be configured to operate with various peripheral display devices. Four possible system configurations are listed in Table 1.1.

Table 1.1 Four Possible System Configurations

<table>
<tr><th></th><th>Mode</th><th>Pin MD[1:0]</th><th>Command Input I/F</th><th>Command Input Format</th><th>Video Input Packet</th><th>Command Output I/F</th><th>Video Output I/F</th></tr>
<tr><td>Config 1</td><td>DPI</td><td>2'b00</td><td rowspan="4">I²C Bus or DSI Link</td><td rowspan="2">Generic Commands</td><td rowspan="2">(Loosely) Packed Pixel Stream</td><td>SPI Master</td><td>DPI Host</td></tr>
<tr><td>Config 2</td><td>CPU</td><td rowspan="2">2'b01</td><td rowspan="2">DBI Host</td><td rowspan="3">DBI Host</td></tr>
<tr><td>Config 3</td><td>DBI-B</td><td rowspan="2">DCS Commands</td><td rowspan="2">DCS Long Write</td></tr>
<tr><td>Config 4</td><td>DBI-B/C</td><td>2'b10</td><td>DBI-C Host</td></tr>
</table>

1. Configuration 1, Figure 1.1:
   - DPI Mode: MD[1:0] pins are set to 2'b00 [note1].
   - DPI host (I/F block) is used to output video data. SPI master is chosen for transferring commands to the peripheral device. An external I²C master configures TC358762XBG via the I²C slave port. It can also issue commands to peripheral display device by writing to TC358762XBG register WCMDQUE or RCMDQUE for write or read commands, respectively [Note4].
   - The external I²C master can assert register bit SLEEP to put TC358762XBG in sleep mode. During the sleep mode, TC358762XBG shuts down all its internal blocks to consume minimum amount of power.
   - DSI link operates in either burst or non-burst mode with sync pulses; DSI host is responsible for generating all the timing required packets. TC358762XBG expects Vsync Start, Vsync End, Hsync Start and Hsync End packets from DSI host in order to run video data synchronously with DSI host.

2. Configuration 2, Figure 1.2:
   - CPU Mode: MD[1:0] pins are tied to 2'b01 [note2], Generic Commands are expected.
   - In this mode, both video data and commands are routed to DBI host I/F.
   - This mode supports LCD device drivers with Intel 80xx CPU I/F. Commands and their parameters can be either 8-bit or 16-bit in width, depending on the setting in register bit APLCNTL[CMD16].
   - In 16-bit command mode, both the command and its parameters are expected to be 16-bit aligned. The un-used byte should be filled with “0s”.
   - Video data are expected in Pixel Stream Packets.

3. Configuration 3, Figure 1.2:
   - DBI-B Mode: MD[1:0] pins are tied to 2'b01 note2, note3, DCS Command Packets are used.
   - In this mode, both video data and commands are routed to DBI host I/F.
   - TC358762XBG switches to this mode when DCS Command Packets are received from DSI link.
   - Only DCS commands are expected in this mode to communicate with peripheral display device, the command bus is set to be 8-bit, independent of register bit APLCNTL[CMD16].

4. Configuration 4, Figure 1.3:
   - DBI-B/C Mode: MD[1:0] pins need to be 2'b10 note2.
   - DBI host is used to output video data; DBI-C host is chosen to communicate with the peripheral device.
   - DSI host uses Generic Long Write packets to configure TC358762XBG and issues DCS command to communicate with peripheral device. In addition, the initialization of TC358762XBG could be done by the display system, too. After detecting the assertion of its interrupt, INTX (active low), pin driven by the peripheral display device; TC358762XBG starts DBI-C host read cycles to fetch desired configurations from the peripheral display device.
   - PWDNX is an active low output signal, which is used to turn off the DC power supplier to the display system as shown in Figure 1.3. TC358762XBG asserts/de-asserts PWDNX after receiving "enter_sleep_mode/exit_sleep_mode" command from DSI host. After asserting PWDNX, DSI host is expected to signal ULPS to put TC358762XBG into sleep mode. During this period, TC358762XBG shuts down the power of all the blocks while keeping DSI Rx port running in order to be woken up by detecting ULPS to LP transition on the DSI link.
   - The peripheral display device also provides a TE input to TC358762XBG, which is used with DCS commands set_tear_on/off to perform video line/frame timing synchronization.
   - DSI host can burst the video data on the link up to one video frame if it sets TC358762XBG's DBI output clock to fetch data faster than DSI link input data rate.
   - The following handshake is required at the beginning of each frame before the TC358762XBG starts sending video data out in DBI-B/C mode:
     - ✧ After receiving DCS command write_memory_start, TC358762XBG pulls down INTX pin for 5 pixel clock cycles and releases it to indicate the start of new frame.
     - ✧ When the peripheral device is ready to accept the new frame of data, it pulls down INTX signal for 5 cycles.
     - ✧ After detecting the falling edge of INTX, TC358762XBG starts pumping data out at DBI port.
   - Only DCS Command Packets are expected in this mode.

Note1: In DPI mode, there are other possible configurations, e.g.: DSI data can be burst, bi-directional DSI link is enabled or DBI-C could be chosen to interface with the peripheral display device.

Note2: Configuration 2, 3 and 4 use DBI host to output video data. They might be referred as DBI modes in this document if it does not cause any ambiguity.

Note3: Both CPU and DBI-B modes use the same pins. DBI-B mode uses DCS commands as specified in MIPI DBI-B standard. CPU mode uses generic commands which follows Intel 80xx CPU I/F specification.

Note4: When I^2C master access to TC358762XBG, DSI Host must not transmit any new DSI packet to TC358762XBG until I^2C access is completed.

The inputs/outputs and high level block diagram of TC358762XBG chip is depicted in Figure 1.4.

Note: BB in the next four figures could be a Baseband or Application Processor.

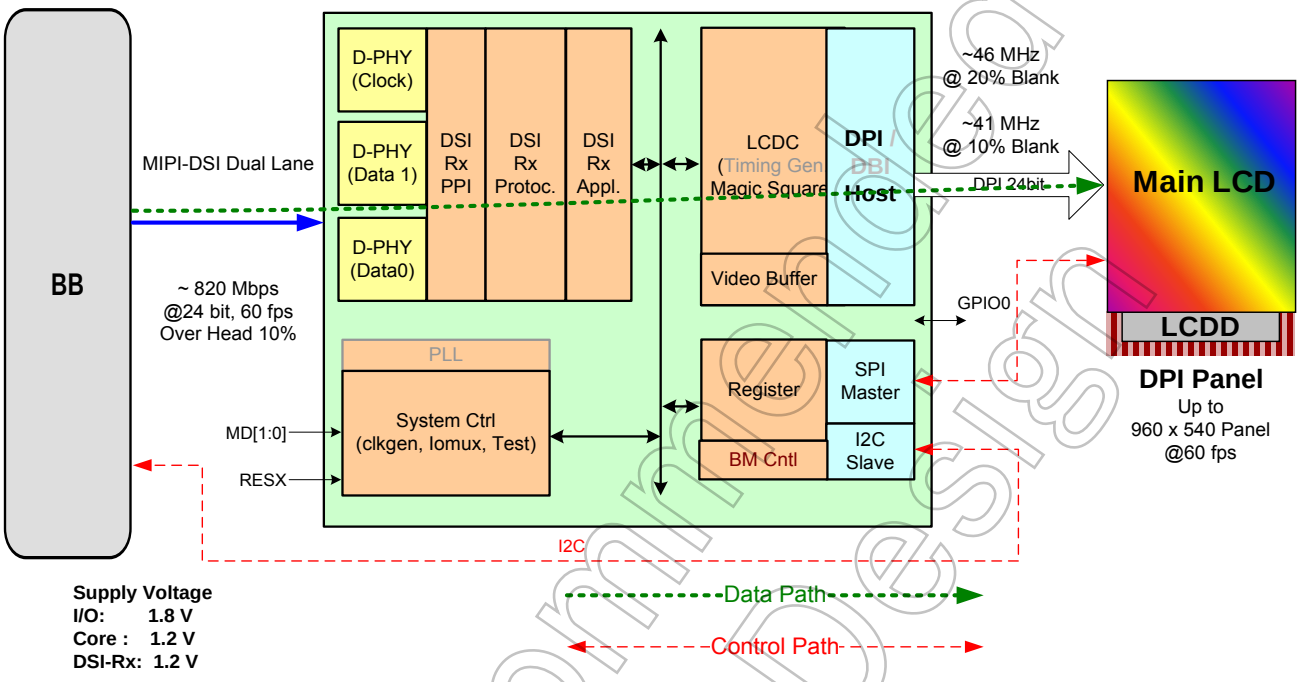


Figure 1.1 TC358762XBG in System Application – Output with DPI and SPI Master

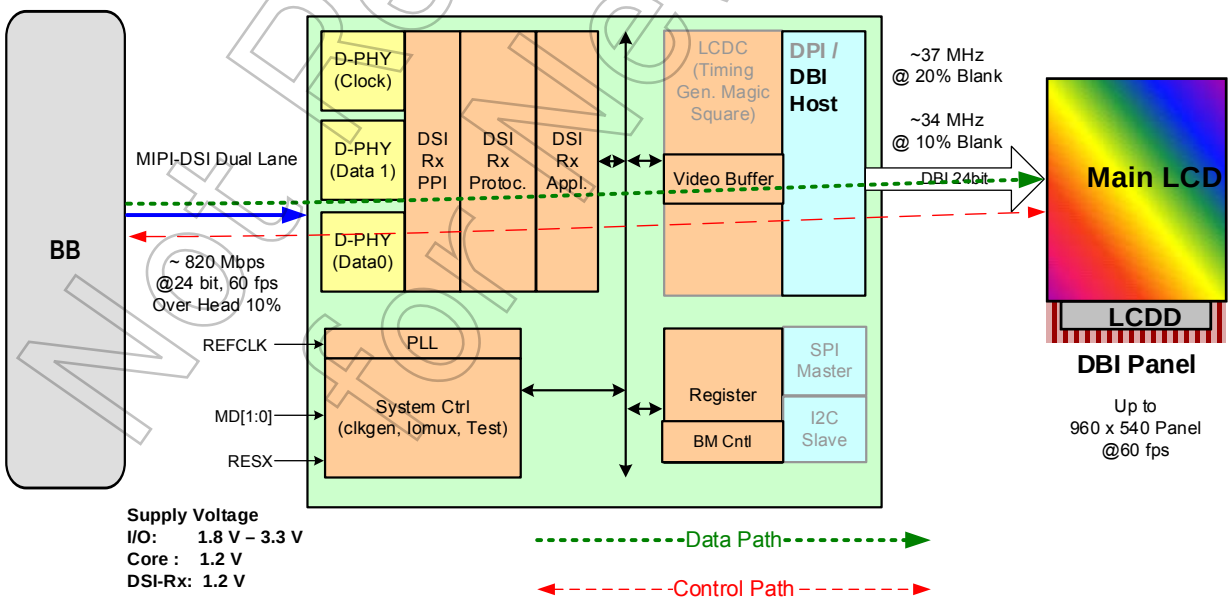


Figure 1.2 TC358762XBG in System Application – Output with DBI host only

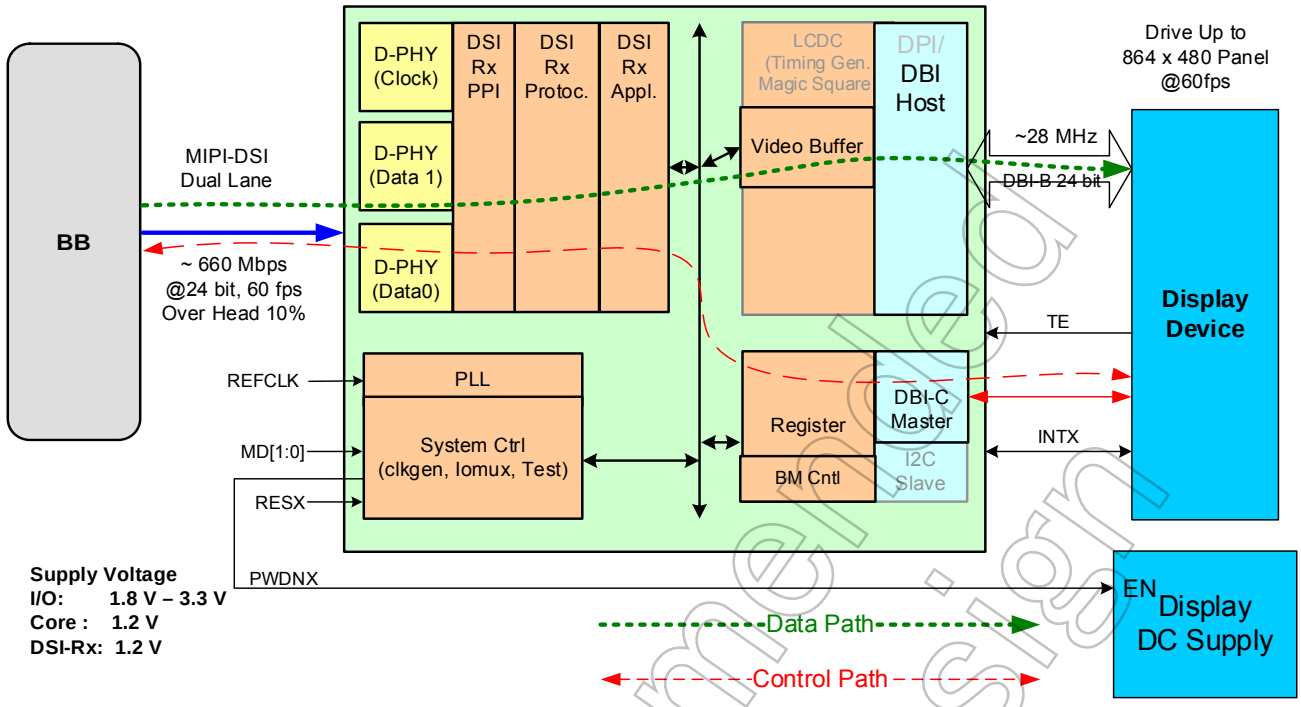


Figure 1.3 TC358762XBG in System Application – Output with DBI and DBI-C host

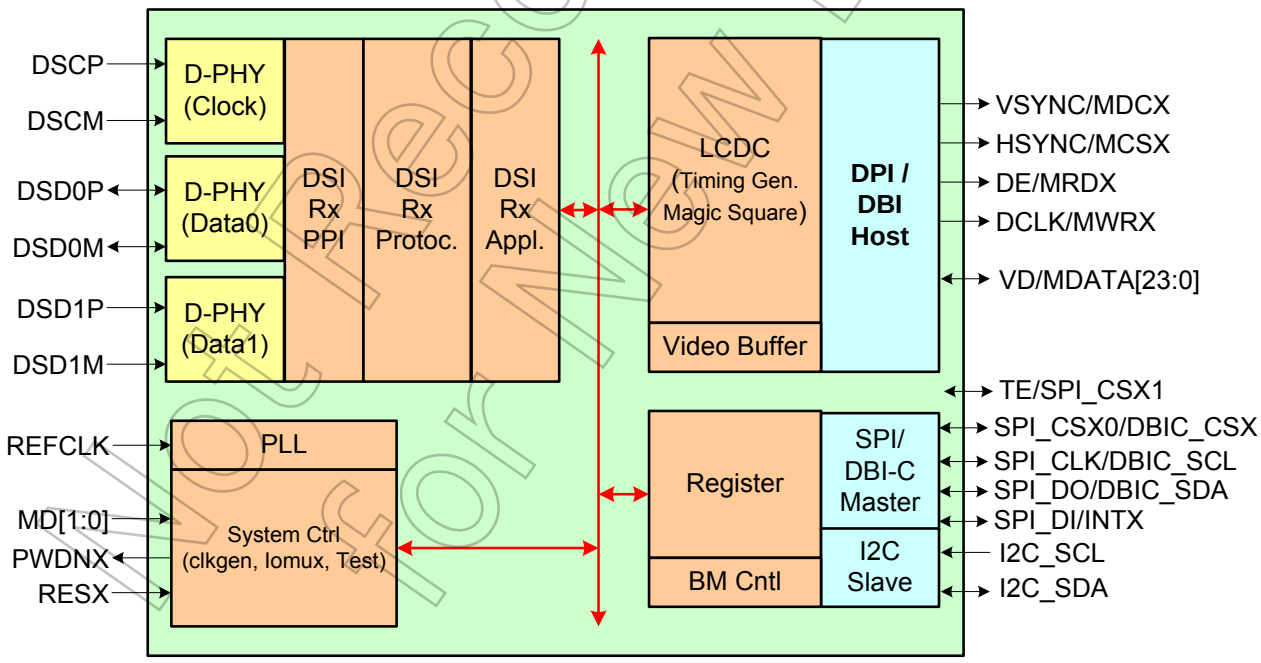


Figure 1.4 TC358762XBG Functional I/Os and Block Diagram

2. Features

- Standard followed:
  - ✧ MIPI DSI version 1.01, Feb 2008
  - ✧ MIPI D-PHY version 0.9, Oct 2007
  - ✧ MIPI DPI version 2.0, Sep, 2005
  - ✧ MIPI DBI-2 version 2.00, Nov 2005
  - ✧ MIPI DCS Command version 1.02, Dec 2008

- DSI Receiver
  - ✧ Dual Data Lane DSI Link with Bi-direction support at Data Lane 0
  - ✧ Maximum speed at 800 Mbps/lane
  - ✧ Video input data formats: RGB-565, RGB-666 and RGB-888
  - ✧ Video input frame rates: Up to 60 fps for WXGA (1366 × 768)
  - ✧ Support various DSI packet types
  - ✧ Provide the path for DSI host/transmitter to control TC358762XBG and its attached Display Device

- DPI Host
  - ✧ Bus speed up to 75 MHz burst rate with data rate up to 216 Mbytes/s
  - ✧ Support the following pixel formats:
    - RGB666 18 bit per pixel
    - RGB666 loosely packed 18 bit per pixel
    - RGB565 16 bit per pixel
    - RGB565 loosely packed 16 bit per pixel
    - RGB888 24 bit per pixel
      - ➢ With the Toshiba Magic Square algorithm, an RGB666 18-bit or 16-bit LCD panel can produce a display equivalent to that of an RGB888 24-bit LCD panel with up to 16-million colors
      - ➢ Programmable output polarity
      - ➢ Support up to frame size 1366 × 768 at 60 fps

- DBI Host
  - ✧ Read/Write Data/Command from the external DBI slave device
  - ✧ Support DCS commands, which is compliant with MIPI DBI-B standard
  - ✧ Support Intel 80xx CPU I/F with either 8-bit or 16-bit commands
  - ✧ Programmable Output Data Format and Bus Width
    - 8 bit Bus, RGB 565 (2 cycles/pixel)
    - 8 bit Bus, RGB 666 (3 cycles/pixel)
    - 8 bit Bus, RGB 888 (3 cycles/pixel)
    - 9 bit Bus, RGB 666 (2 cycles/pixel)
    - 16 bit Bus, RGB 565 (1 cycles/pixel)
    - 16 bit Bus, RGB 666 (3 cycles/2 pixel) note1
    - 16 bit Bus, RGB 888 (3 cycles/2 pixel) note1
    - 18 bit Bus, RGB 666 (1 cycles/pixel)
    - 24 bit Bus, RGB 888 (1 cycles/pixel)
      - ➢ Support up to 864x480 at 60 fps (or 1280×720 at 30 fps)

Note 1: When this format is selected, the horizontal image size must be multiple of four.

- SPI Master
  - ✧ 4-pin SPI master I/F, CSX[1:0], CLK, DI and DO
  - ✧ Support two SPI slaves
  - ✧ Data Rate up to 10 Mbps
  - ✧ The main purpose of this port is used to configure DPI slave display devices
  - ✧ Half Duplex data transfer support

- DBI-C host
  - ✧ 3-pin DBI-C host I/F, CSX, SCL and SDA
  - ✧ Shared pins with SPI I/F, only one can be active at a given time
  - ✧ Data Rate up to 10 Mbps
  - ✧ Programmable read delay

- I^2C compliant interface Slave Port
  - ✧ Data Rate up to 400 kHz
  - ✧ External I^2C master can access TC358762XBG internal registers via this port
  - ✧ Address auto increment is supported
  - ✧ TC358762XBG Slave Port address is “0001011”
  - ✧ During I^2C slave cycle, DSI host must not transmit any new DSI packet to TC358762XBG.

- A 1024 × 24 dual port Video Buffer is used to buffer the video data received from DSI link.

- System Operation
  - ✧ Register programming through DSI link via Generic Write Long packets.
  - ✧ Register read through DSI link via Generic Read, 2 parameters packets.
  - ✧ Write to WCMQUE and RCMDQUE registers enable host to configure and control peripheral display device
  - ✧ DCS commands are routed to peripheral display device to interpret
  - ✧ Provide Tearing Effect Trigger message after receiving set_tear_on command

- Clock source:
  - ✧ External reference clock: recommended 6 - 40 MHz
  - ✧ A programmable PLL is used to adjust the output video clock:
    - In DPI output mode with DSI link burst data, adjust output clock to the desired pixel clock frequency to assure no video is lost due to video buffer over/under flow.
    - In DBI output mode, adjust output clock frequency fast enough to prevent video buffer from over flow.

- Power supply
  - ✧ MIPI D-PHY: 1.2V
  - ✧ I/O: 1.8V – 3.3V (all IO pins must be same power level)
  - ✧ Core: 1.2V

- Power Consumption
  - ✧ Sleep State
    - PLL OFF mode - Sleep mode (DSI-CLK stops toggle)
      - ➢ IOs: 0.05 µW
      - ➢ CORE: 23 µW
      - ➢ D-PHYs: 3 mW
      - ➢ PLLs: Off (PLL power – 0V)

    - PLL ON mode - Sleep mode (DSI-CLK goes to ULPS state, REFCLK toggles)
      - ➢ IOs: 0.15 µW
      - ➢ CORE: 23 µW
      - ➢ D-PHYs: 9 µW
      - ➢ PLLs: 28 µW

  - ✧ Normal Operation:
    - PLLOFF mode (480x864 @60fps, DSI-CLK: 400 MHz – 2 data lanes)
      - ➢ 18 mW
      - ➢ PLLON mode (480x864 @60fps, DSI-CLK: 400 MHz, PLLCLK: 50.28MHz, PCLK=PLL/2)
      - ➢ 19 mW

- Packaging
  - ✧ BGA 64 pins
  - ✧ 5.0mm × 5.0mm × 1mm
  - ✧ 0.5mm ball pitch

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

3. External Pins

3.1. Pin Layout

The mapping of TC358762XBG signals to the external pins is shown in the figure below.

A1 DSD0P	A2 RESX	A3 VSSC	A4 DCLK	A5 VD01	A6 VD02	A7 VD04	A8 VD05
B1 DSD0M	B2 PWDNX	B3 VDDC	B4 VSYNC	B5 VD00	B6 VSSO	B7 VDDS	B8 VD06
C1 DSCP	C2 MD0	C3 MD1	C4 HSYNC	C5 VD20	C6 VD03	C7 VD07	C8 VSSC
D1 DSCM	D2 VSSA	D3 VDDS	D4 DE	D5 VD21	D6 VSSO	D7 VD08	D8 VD09
E1 DSD1P	E2 VSSC	E3 SPI_CSX1	E4 VSSO	E5 VD22	E6 VDDC	E7 VD11	E8 VD10
F1 DSD1M	F2 I2C_SCL	F3 SPI_CSX0	F4 SPI_DI	F5 VD23	F6 VD16	F7 VDDS	F8 VSSO
G1 VDDA	G2 I2C_SDA	G3 VDDPL	G4 VSSO	G5 VD19	G6 VSSO	G7 VD14	G8 VD12
H1 VSSPL	H2 REFCLK	H3 SPI_DO	H4 SPI_CLK	H5 VD18	H6 VD17	H7 VD15	H8 VD13

Figure 3.5 TC358762XBG Chip Pin Layout (Top view)

Pin Name Abbreviation:

VSYNC (B4): VSYNC/MDCX
HSYNC (C4): HSYNC/MCSX
DE (D4): DE/MRDX
DCLK (A4): DCLK/MWRX
VDn (n=0 to 23): VD[23:0]/MDATA[23:0]
SPI_CSX0 (F3): SPI_CSX0/DBIC_CSX/GPIO3
SPI_CLK (H4): SPI_CLK/DBIC_SCL/GPIO2
SPI_DO (F3): SPI_DO/DBIC_SDA/GPIO1
SPI_DI (F4): SPI_DI/INTX/
SPI_CSX1(E3): SPI_CSX1/TE/GPIO4

3.2. Pinout Description

The following table gives the signals of TC358762XBG and their function.

Table 3.2 TC358762XBG functional signal list

Group	Pin Name	Pin No.	Type	Buffer Type	Function	Power Supply
System	RESX	A2	I	SCH	System Reset – active Low	1.8V-3.3V
	REFCLK	H2	I	SCH	6MHz – 40MHz Reference Clock	1.8V-3.3V
	PWDNX	B2	O	N	Power Down signal (active low) H → L: TC358762XBG enter Power down state L → H : TC358762XBG exit Power down state	1.8V-3.3V
	MD[1:0]	C2 C3	I	N	Mode selection 00: DPI mode 01: CPU or DBI-B mode 10: DBI-B/C mode 11: Test mode	1.8V-3.3V
MIPI-DSI	DSCP	C1	I	MIPI-PHY	MIPI-DSI clock channel positive	1.2V
	DSCM	D1	I	MIPI-PHY	MIPI-DSI clock channel negative	1.2V
	DSD0P	A1	I/O	MIPI-PHY	MIPI-DSI Data 0 channel positive	1.2V
	DSD0M	B1	I/O	MIPI-PHY	MIPI-DSI Data0 channel negative	1.2V
	DSD1P	E1	I	MIPI-PHY	MIPI-DSI Data 1 channel positive	1.2V
	DSD1M	F1	I	MIPI-PHY	MIPI-DSI Data 1 channel negative	1.2V
DPI/ DBI	VSYNC/ MDCX	B4	O	Nps	DPI i/f: Vsync signal DBI i/f: Data/Command signal	1.8V-3.3V
	HSYNC/ MCSX	C4	O	Nps	DPI i/f: Hsync signal DBI i/f: Chip Select signal	1.8V-3.3V
	DE/ MRDX	D4	O	Nps	DPI i/f: Data Enable signal DBI i/f: Read Command signal	1.8V-3.3V
	DCLK/ MWRX	A4	O	Nps	DPI i/f: Clock signal DBI i/f: Write Command signal	1.8V-3.3V
	VD[23:0]/ MDATA[23:0]	-	I/O	Nps	VD[23:0] : 24-bit video data	1.8V-3.3V
SPI/ DBI-C/ Misc.	SPI_CSX0/ DBIC_CSX/ GPIO3	F3	I/O	N	DPI i/f: GPIO3 signal(default) or SPI Chip Select signal DBI i/f: GPIO3 signal DBI-B/C i/f: DBI-C Chip Select signal	1.8V-3.3V
	SPI_CLK/ DBIC_SCL/ GPIO2	H4	I/O	N	DPI i/f: GPIO2 signal(default) or SPI Clock signal DBI i/f: GPIO2 signal DBI-B/C i/f: DBI-C Clock signal	1.8V-3.3V
	SPI_DO/ DBIC_SDA/ GPIO1	H3	I/O	N	DPI i/f: GPIO1 signal(default) or SPI Output Data signal DBI i/f: GPIO1 signal DBI-B/C i/f: DBI-C Data signal	1.8V-3.3V
	SPI_DI/ INTX/ GPIO0	F4	I/O	N	DPI i/f: GPIOI0 signal(default) or SPI Input Data DBI i/f: GPIO0 signal DBI-B/C i/f: INTX signal	1.8V-3.3V
	SPI_CSX1/ TE/ GPIO4	E3	I/O	N	DPI i/f: GPIO4 signal(default) or SPI_CSX1 signal DBI i/f: TE signal DBI-B/C i/f: TE signal	1.8V-3.3V

I2C	I2C_SCL	F2	I	S-OD	I2C_SCL signal	1.8V-3.3V
	I2C_SDA	G2	I/O	S-OD	I2C_SDA signal Notes: if I2C i/f is not use, must pull LOW on this signal.	1.8V-3.3V
POWER & GROUND	See table below	-	-	-	-	-

Table 3.3 TC358762XBG Power signal list

PWR & GND PINS	PIN NAME	PIN NO	PIN DESCRIPTION	Power Supply Voltage
POWER	VDDC	(2)	VDD for Internal Core	1.2V
	VDDS	(3)	VDD for IO power supply	1.8V-3.3V
	VDDPL	(1)	VDD for PLL	1.2V
	VDDA	(1)	VDD for MIPI-DSI PHY	1.2V
GROUND	VSSA	(1)	VSS for MIPI-DSI PHY	-
	VSSPL	(1)	VSS for PLL	-
	VSSC	(3)	Core VSS	-
	VSSO	(6)	IO VSS	-

Buffer Type Abbreviation:

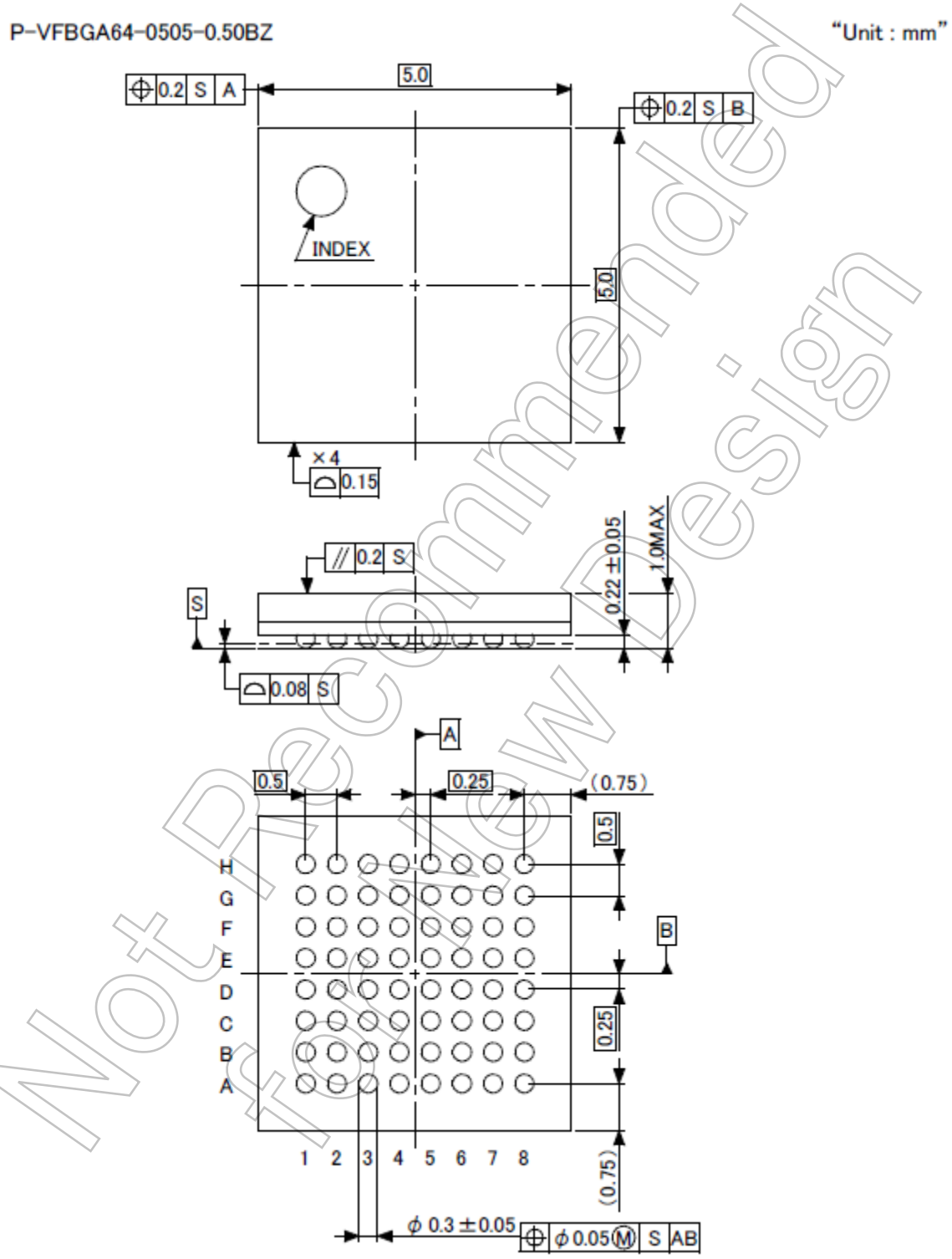
N: Normal IO (2mA)
Nps: Normal IO with Programmable Output Strength (1/2/3/4 mA)
S-OD: Pseudo open-drain output, schmitt input
SCH: Fail Safe schmitt input buffer
MIPI-PHY: front-end analog IO for MIPI
APAD: Analog pad

Table 3.4 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	5	-
MIPI-DSI	6	-
DPI/DBI	28	-
SPI/DBI-C/Misc.	5	-
I2C	2	-
POWER & GROUND	18	-
Total Pin Count	**64**	

4. Package

TC358762XBG housed in a P-VFBGA64-0505-0.50BZ package (5 mm by 5 mm size), 0.5mm ball pitch. The detailed package drawing is shown below.



Weight: 41 mg (Typ.)

Figure 4.6 P-VFBGA64-0505-0.50BZ Package Dimension

5. Electrical characteristics

5.1. Absolute Maximum Ratings

Operating ambient Temperature range: Ta = -20°C - +85°C

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 5.5 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V-3.3V – Digital IO)	VDDS	-0.3 to +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 to +2.0	V
Supply voltage (1.2V – MIPI DSI PHY)	VDDA	-0.3 to +2.0	V
Supply voltage (1.2V – PLL)	VDDPL	-0.3 to +2.0	V
Input voltage (DSI I/O)	V_{IN_DSI}	-0.3 to VDDA+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDS+0.3	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-40 to +125	°C

5.2. Operating Conditions

Table 5.6 Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V – Digital IO)	VDDS	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDS	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – PLL)	VDDPL	1.1	1.2	1.3	V
Supply voltage (1.2V – MIPI-DSI PHY)	VDDA	1.12	1.2	1.28	V
Operating temperature (ambient temperature with voltage applied)	T_a	-20	-	+85	°C

5.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

5.3.1. Normal CMOS I/Os

Table 5.7 DC Electrical Specification - Normal CMOS IO

Parameter – CMOS I/Os	Symbol	Min	Typ.	Max	Unit
Input voltage, High level CMOS input Note1	V_{IH}	0.7 VDDS	-	VDDS	V
Input voltage, Low level CMOS input Note1	V_{IL}	0	-	0.3 VDDS	V
Input voltage High level CMOS Schmitt Trigger Note 1,2	VIHS	0.7 VDDS	-	VDDS	V
Input voltage Low level CMOS Schmitt Trigger Note 1,2	VILS	0	-	0.3 VDDS	V
Output voltage, High level Note1, 2	V_{OH}	0.8 VDDS	-	VDDS	V
Output voltage, Low level Note1, 2	V_{OL}	0	-	0.2 VDDS	V
Input leakage current, High level	I_{ILH} (Note3)	-10	-	10	µA
Input leakage current, Low level	I_{ILL} (Note4)	-10	-	10	µA

Note1: Each power source is operating within recommended operating condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.
V_{OH}, V_{OL} values above are specification when current, which is defined in type column of Table 3.1, flows at corresponding I/O pin.

Note3: Normal pin or Pull-up I/O pin applied VDDS supply voltage to Vin (input voltage)

Note4: Normal pin or Pull-down I/O pin applied VSS (0V) to Vin (input voltage)

5.3.2. DSI Differential Inputs

5.3.2.1. Low power transmitter

The low power transmitter is used for driving the lines in all low-power operating modes. The DC characteristics of the LP transmitter are given below.

Table 5.8 MIPI DSI LP transmitter DC characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V
Thevenin output low level	V_{OL}	-50	-	50	mV
Output impedance of the LP transmitter	Z_{OLP}	110	-	-	Ω

5.3.2.2. High speed receiver

The HS receiver is a differential line receiver with a switch able parallel input termination. It will be used to receive data during high speed transmission from the host. The DC characteristics of the HS receiver are given below.

Table 5.9 MIPI DSI HS receiver DC characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV
Differential input impedance	Z_{ID}	80	100	125	Ω

5.3.2.3. Low power receiver

The LP receiver is used to detect the Low-Power state on each pin. The LP will be used to receive data during low speed transmission from the host. The DC characteristics of the LP receiver are given below.

Table 5.10 MIPI DSI LP receiver DC characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage, not in ULP state	V_{IL}	-	-	550	mV
Logic 0 input voltage, ULP state	$V_{IL-ULPS}$	-	-	300	mV
Input hysteresis	V_{HYST}	25	-	-	mV

6. Revision History

Table 6.11 Revision History

Revision	Date	Description
1.412	2016-04-01	Newly released
1.412	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.45	2016-06-03	Added Figure 1.1. Updated Figure 1.4 to have I2C_SCL as input. Changed D6 pin name of Figure 3.1.
1.46	2017-09-25	Modified PIN NO of Table 3.2. Changed header, footer and the last page. Changed corporate name and descriptions.

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