

LCD Module User Manual

Customer : _____
Ordering CODE : TC4004A-01XA0_A00
DRAWING NO. : m-TC4004A-01XA0_A00

Approved By Customer:

Date:

| Approved By | Checked By | Prepared By |
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1. Precautions in Use of LCD Module

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD Module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.

Storage: please storage in anti-static electricity container and clean environment.

2. General Specification

| ITEM | STANDARD VALUE | UNIT |
|-------------------|--|------|
| Number of dots | 40X4 CHARS | Dots |
| Outline dimension | 190.0(W)X54.0(H)X13.0MAX.(T) | mm |
| View area | 147.0(W)X29.5(H) | mm |
| Active area | 140.45(W)X23.16(H) | mm |
| Dot size | 0.50(W)X0.55(H) | mm |
| Dot pitch | 0.57(W)X0.62(H) | mm |
| LCD type | STN, Yellow-green, positive, Transflective | |
| View direction | 6 o'clock | |
| Backlight | Yellow-green LED | |
| Controller | SPLC780D1-001, Parallel interface | |

3. Absolute Maximum Ratings

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------------------------------|------|------|-----------------|------|
| Operating Temperature | T _{OP} | -20 | - | +70 | |
| Storage Temperature | T _{ST} | -30 | - | +80 | |
| Input Voltage | V _I | 0 | - | V _{DD} | V |
| Supply Voltage For Logic | V _{DD} | 0 | - | 5.5 | V |
| Supply Voltage For LCD | V _{DD} -V _{EE} | 0 | - | 5 | V |

4. Electrical Characteristics

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---------------------|-----------------|-----------------|------|------|----------|------|
| Logic Voltage | $V_{DD}-V_{SS}$ | - | 4.7 | 5.0 | 5.2 | V |
| Supply Volt.For LCD | $V_{DD}-V_O$ | Ta=25 | --- | 4.7 | --- | V |
| Input High Volt. | V_{IH} | - | 2.0 | - | V_{DD} | V |
| Input Low Volt. | V_{IL} | - | -0.3 | - | 0.8 | V |
| Output High Volt. | V_{OH} | $I_{OH}=-0.2mA$ | 2.4 | - | V_{DD} | V |
| Output Low Volt. | V_{OL} | $I_{OL}=1.6mA$ | 0 | - | 0.4 | V |
| Supply Current | I_{DD} | - | --- | --- | 2.0 | mA |

5. Backlight Information

Absolute Maximum ratings (Ta=25)

| Item | Symbol | Conditions | Rating | Unit |
|----------------------------------|------------|----------------------------|---------|------|
| Reverse voltage | V_r | - | 5.0 | V |
| Reverse Current | I_r | $V_r=5.0V$ | 80 | uA |
| Absolute maximum forward Current | I_{fm} | | 100 | mA |
| Peak forward current | I_{fp} | 1 msec plus 10% Duty Cycle | 240 | mA |
| Power dissipation | P_d | | 340 | mW |
| Operating Temperature Range | T_{oper} | | -30~+70 | |
| Storage Temperature Range | T_{st} | | -40~+80 | |

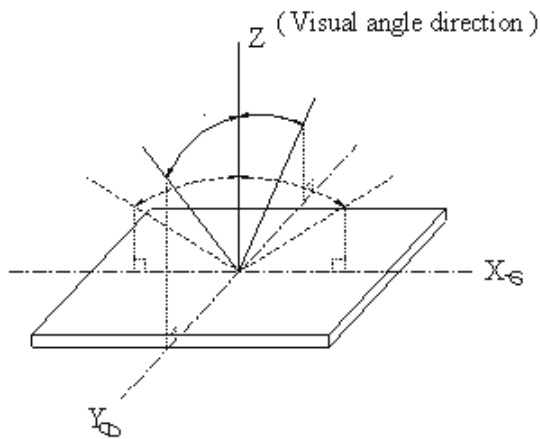
Electrical/Optical Characteristics (Ta=25°C, If=120mA)

| Color | Wavelength p(nm) | Spectral line half width (nm) | Operating Voltage(v) (± 0.15V) | Forward Current (mA) |
|--------------|---------------------|----------------------------------|-----------------------------------|----------------------------|
| Yellow-green | --- | --- | 3.1 | 120 |

6. Optical Characteristics

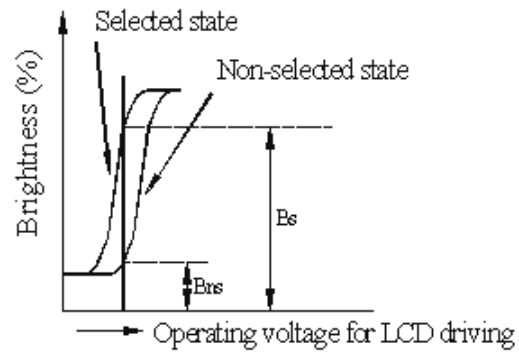
| ITEM | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|----------------|--------|-----------|-----|-----|-----|------|
| View Angle | (V) | CR 2 | 10 | - | 120 | deg. |
| | (H) | CR 2 | -45 | - | 45 | deg. |
| Contrast Ratio | CR | - | - | 5 | - | - |
| Response Time | T rise | - | - | 200 | 300 | ms |
| | T fall | - | - | 150 | 200 | ms |

View Angles

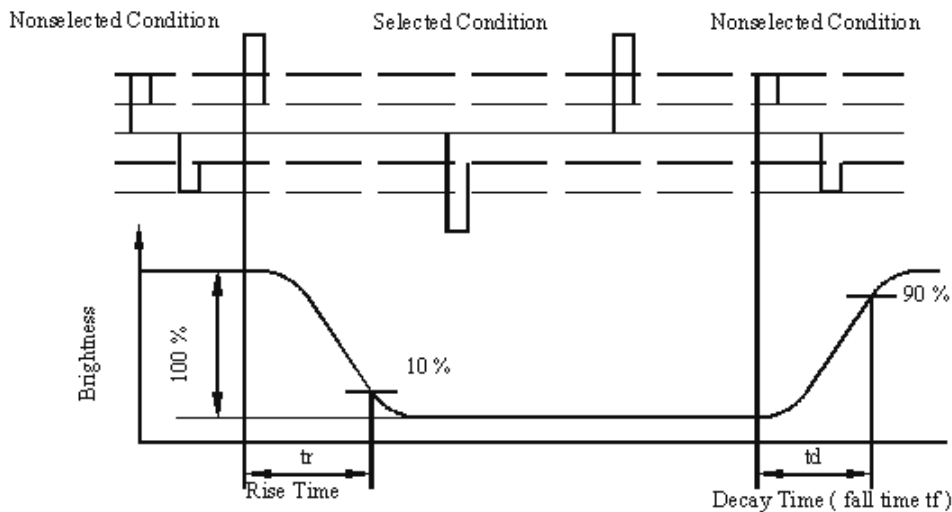


Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



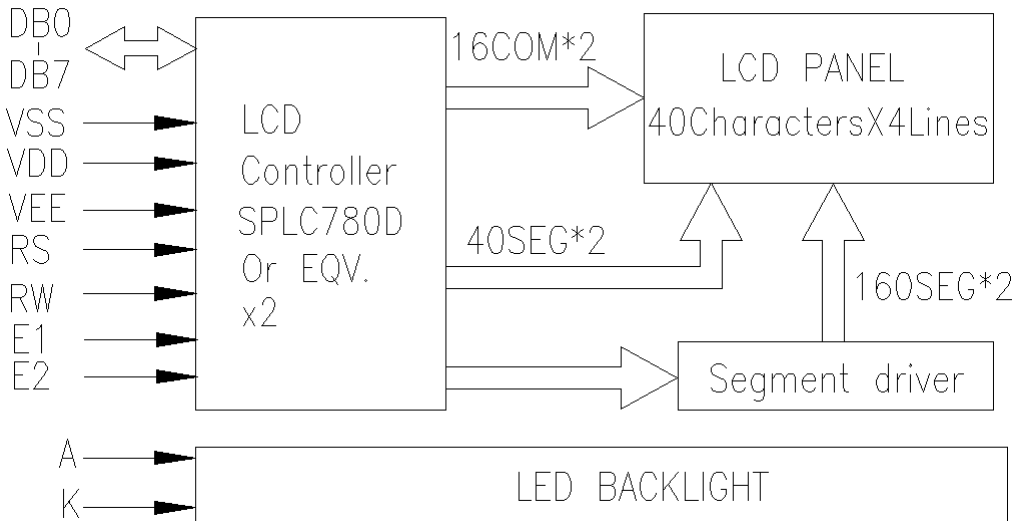
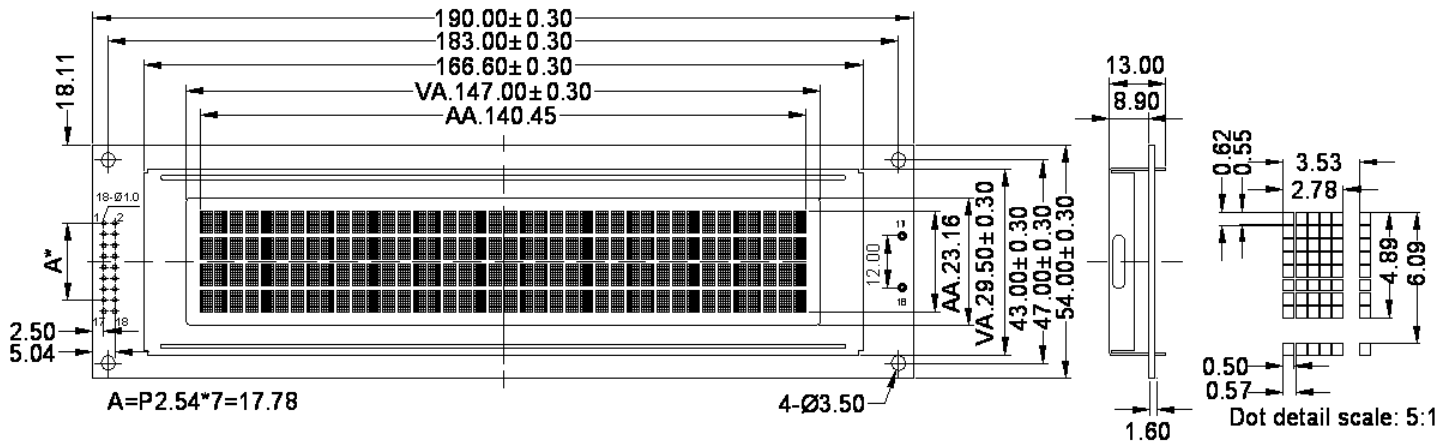
Response time



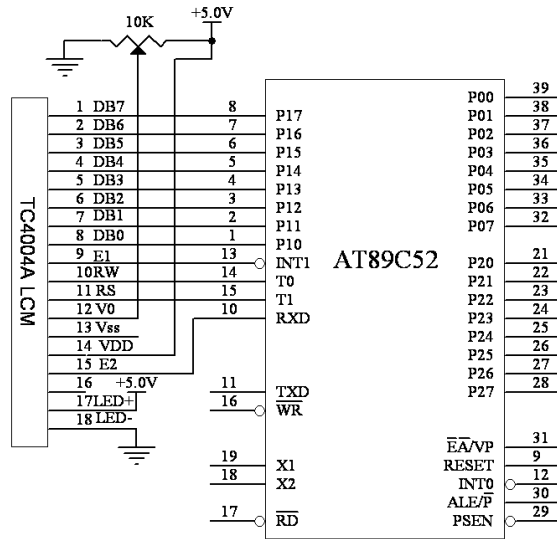
7.Interface Description

| Pin No. | Symbol | Level | Description |
|---------|-----------------|------------|---------------------------------------|
| 1~8 | DB7~DB0 | H/L | Data bus. DB7 is used for Busy Flag . |
| 9 | E1 | H/L | Enable signal for CHIP1 |
| 10 | RW | H/L | H:Read L:Write |
| 11 | RS | H/L | H:Data L :Instruction |
| 12 | V0 | (Variable) | Driving voltage for LCD |
| 13 | V _{SS} | 0V | Ground |
| 14 | V _{DD} | +5.0V | Power supply for Logic |
| 15 | E2 | H/L | Enable signal for CHIP2 |
| 16 | NC | --- | No connection |
| 17 | A(LED+) | +5.0V | Anode of LED Backlight |
| 18 | K(LED-) | 0V | Cathode of LED Backlight |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

8. Contour Drawing & Block Diagram



9. Application circuit



10. LCM Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

Various Kinds of Operations according to RS and R/W Bits

| RS | R/W | Operation |
|----|-----|---|
| 0 | 0 | IR write as an internal operation (display clear, etc.) |
| 0 | 1 | Read busy flag (DB7) and address counter (DB0 to DB7) |
| 1 | 0 | Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM) |
| 1 | 1 | Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR) |

Busy Flag (BF)

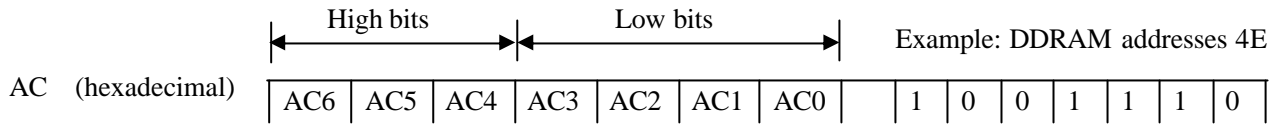
When the **BF= "High"**, it indicates that the LCM internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is **not High**.

Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



LCD DDRAM Address

| 40 Chars X 4 Lines Display | | | | | | | | | | | | | | | | | |
|----------------------------|----------------------|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|----|
| Character No. | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | ... | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 |
| Chip1 | 1 st Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | ... | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| | 2 nd Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | ... | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 |
| Chip2 | 3 rd Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | ... | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| | 4 th Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | ... | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 |

Character Generator ROM (CGROM)

The CGROM generate 5x8 dot or 5x10 dot character patterns from 8-bit character codes. See “Standard Character pattern”.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM) shown as below.

| Char Code(DDRAM data) | | | | | | | | CGRAM address | | | CGRAM data | | | | | | | | Pattern number | | | |
|-----------------------|----|----|----|----|----|----|----|---------------|----|----|------------|----|----|----|----|----|----|----|----------------|----|----|-----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | | P2 | P1 | P0 |
| 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 0 | 1 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 1 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 1 | 1 | . | . | . | 1 | 1 | 1 | 1 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 0 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 0 | 1 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 1 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 1 | 1 | . | . | . | 0 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 0 | X | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 0 | 1 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 1 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 0 | 1 | 1 | . | . | . | 1 | 1 | 1 | 1 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 0 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 0 | 1 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 1 | 0 | . | . | . | 1 | 0 | 0 | 0 | 1 | |
| . | . | . | . | . | . | . | . | . | . | . | 1 | 1 | 1 | . | . | . | 0 | 0 | 0 | 0 | 0 | |

“X”: don't care

11. User instruction Definitions

11.1 Instruction table

| Instruction | Instruction Code | | | | | | | | | | Description | Execution time f _{osc} =270KHz) | |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------------|--|--------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM and set DDRAM address to "00H" from AC. | 1.52ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.52ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction and make shift of entire display enable. | 37μ s |
| Display ON/OFF control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display(D), cursor(C), and blinking of cursor(B) on/off control bit. | 37μ s |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 37μ s |
| Function Set | 0 | 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X | Set interface data length(DL:4-bit/8-bit), numbers of display line(N: 1-line/2-line), display font type(F: 5X8 dots/ 5X11 dots) | 37μ s |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set CGRAM address in address counter. | 37μ s |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set DDRAM address in address counter. | 37μ s |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Whether during internal operation or can not be known by reading BF. The contents of address counter can also be read. | 0μ s |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Write data into internal RAM (DDRAM/CGRAM). | 43μ s |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Read data from internal RAM (DDRAM/CGRAM). | 43μ s |

Remark: ' X ' don't care

11.2 Instruction Description

1) Clear Display

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status. Namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

3) Entry Mode Set

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH |

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read / write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value:

I/D = "1" : shift left,

I/D = "0" : shift right.

4) Display ON/OFF Control

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display / cursor / blink ON / OFF 1 bit register.

D: Display ON / OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON / OFF control bit

When C = "High", cursor is turned on.

When C = "Low", Cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON / OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = "Low", blink is off.

5) Cursor or Display Shift

| | | | | | | | | | |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - |

Shifting of right/left cursor position or display Without Writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. (refer to Table 4) During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

| S/C | R/L | Operation |
|-----|-----|--|
| 0 | 0 | Shift the cursor to the left, AC is decreased by 1. |
| 0 | 1 | Shift the cursor to the right, AC is increased by 1. |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display. |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display. |

6) Function Set

| | | | | | | | | | |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - |

DL: Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

F: Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

7) Set CGRAM Address

| | | | | | | | | | |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

| | | | | | | | | | |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether LCM is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

10) Write data to RAM

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

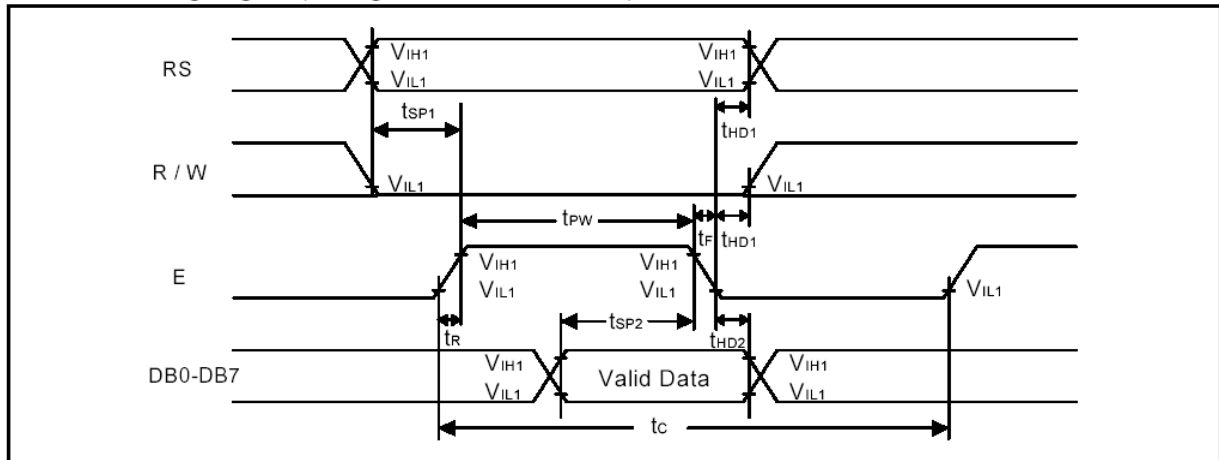
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address

set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

12. Timing Characteristics

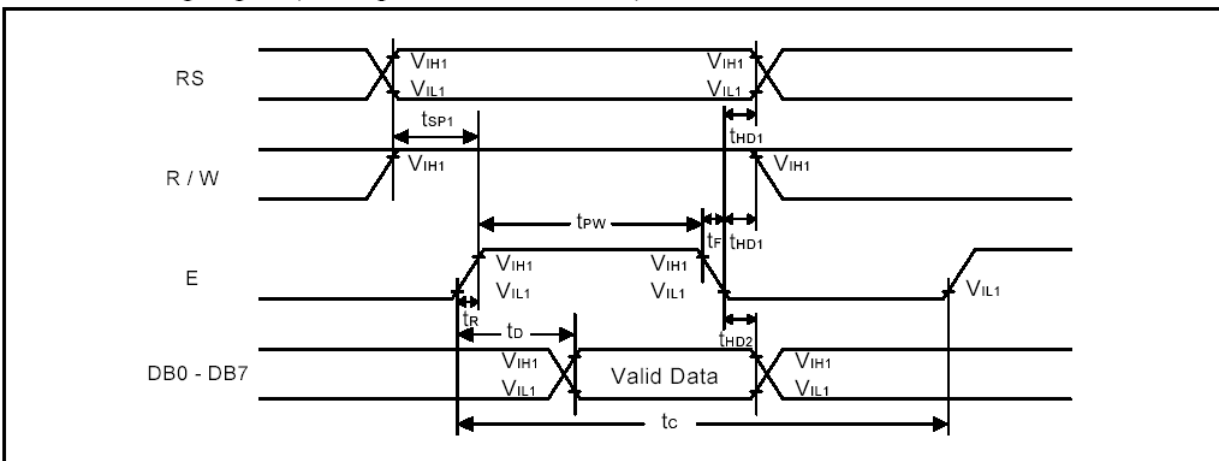
Write mode timing diagram (Writing Data from MPU to LCM)



Write mode (Writing Data from MPU to LCM)

| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|--------------------|------------|-------|------|------|------|------------------|
| | | Min. | Typ. | Max. | | |
| E Cycle Time | t_C | 500 | - | - | ns | Pin E |
| E Pulse Width | t_{PW} | 230 | - | - | ns | Pin E |
| E Rise/Fall Time | t_R, t_F | - | - | 20 | ns | Pin E |
| Address Setup Time | t_{SP1} | 40 | - | - | ns | Pins: RS, R/W, E |
| Address Hold Time | t_{HD1} | 10 | - | - | ns | Pins: RS, R/W, E |
| Data Setup Time | t_{SP2} | 80 | - | - | ns | Pins: DB0 - DB7 |
| Data Hold Time | t_{HD2} | 10 | - | - | ns | Pins: DB0 - DB7 |

Read mode timing diagram (Reading Data from LCM to MPU)

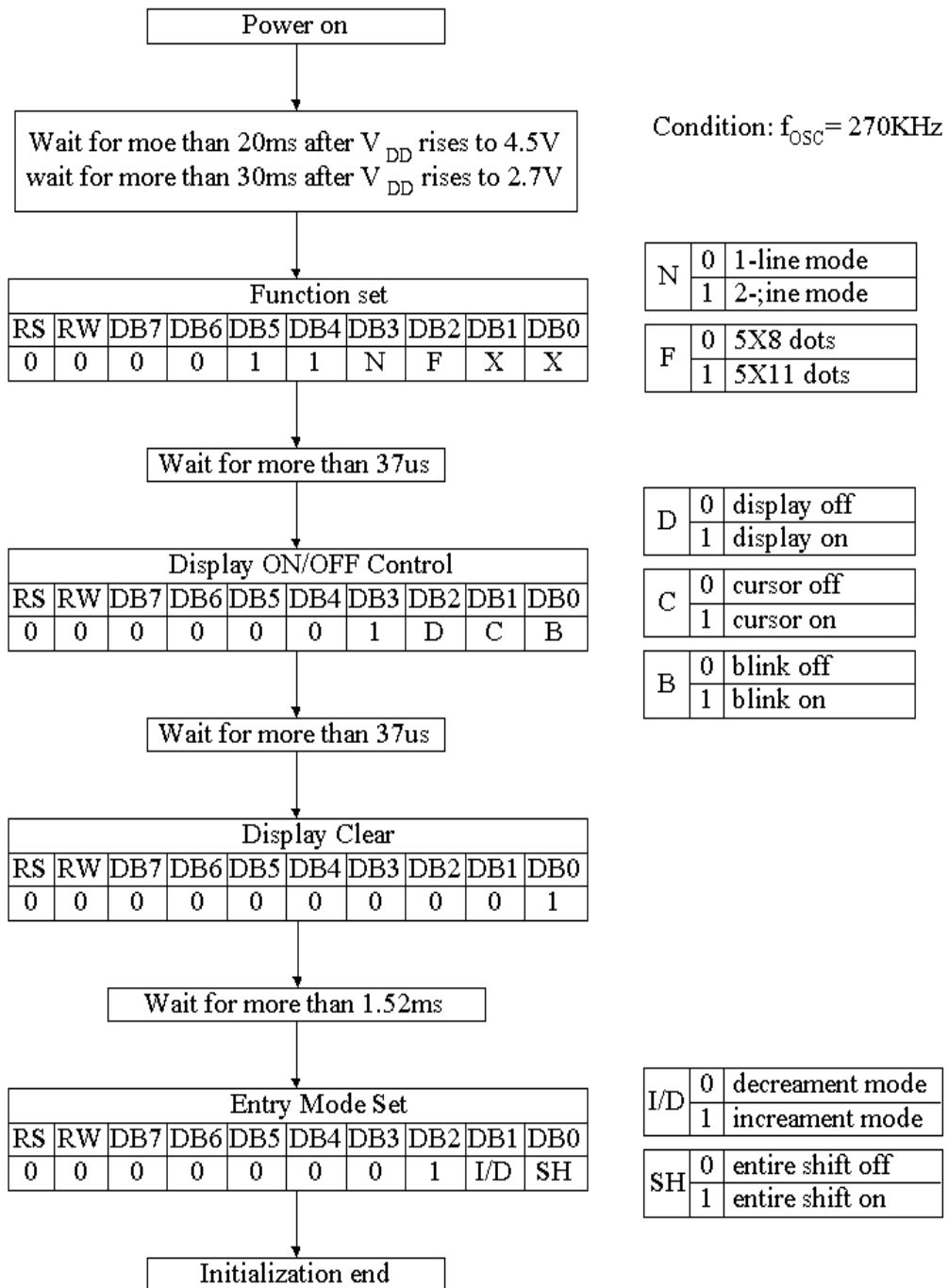


Read mode (Reading Data from LCM to MPU)

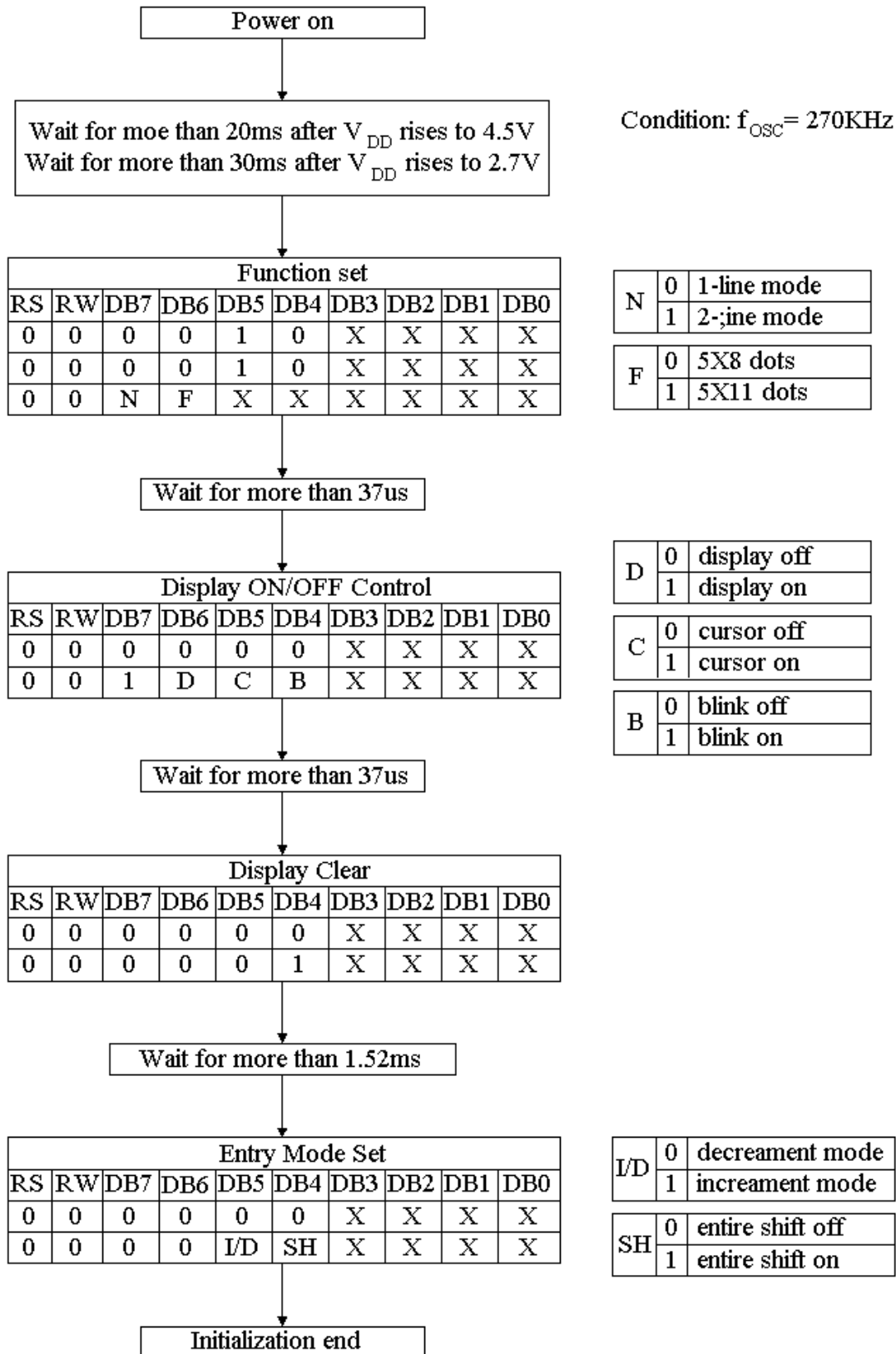
| Characteristics | Symbol | Limit | | | Unit | Test Condition |
|------------------------|------------|-------|------|------|------|------------------|
| | | Min. | Typ. | Max. | | |
| E Cycle Time | t_C | 500 | - | - | ns | Pin E |
| E Pulse Width | t_W | 230 | - | - | ns | Pin E |
| E Rise/Fall Time | t_R, t_F | - | - | 20 | ns | Pin E |
| Address Setup Time | t_{SP1} | 40 | - | - | ns | Pins: RS, R/W, E |
| Address Hold Time | t_{HD1} | 10 | - | - | ns | Pins: RS, R/W, E |
| Data Output Delay Time | t_D | - | - | 120 | ns | Pins: DB0 - DB7 |
| Data hold time | t_{HD2} | 5.0 | - | - | ns | Pin DB0 - DB7 |

13. Initializing flow chart

- 8-bit interface mode



● 4-bit interface mode



14. Standard Character pattern

Higher 4-bit of character code (Hex.)

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|-----------------------|---|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 CG RAM (1) | | | 0 | 1 | P | Q | R | | | | - | 9 | 3 | α | p | |
| 1 (2) | | ! | 1 | A | Q | a | 9 | | | 0 | 7 | チ | 4 | ä | q | |
| 2 (3) | | " | 2 | B | R | b | r | | | 「 | イ | ツ | × | ß | θ | |
| 3 (4) | | # | 3 | C | S | c | s | | | 」 | ウ | テ | ε | ε | ∞ | |
| 4 (5) | | \$ | 4 | D | T | d | t | | | 、 | エ | ト | ト | μ | Ω | |
| 5 (6) | | % | 5 | E | U | e | u | | | ・ | オ | ナ | 1 | ö | ü | |
| 6 (7) | | & | 6 | F | V | f | v | | | ヲ | カ | ニ | ヨ | ρ | Σ | |
| 7 (8) | | ' | 7 | G | W | g | w | | | ア | キ | ヌ | ラ | g | π | |
| 8 (1) | | (| 8 | H | X | h | x | | | ィ | ク | ネ | リ | ς | Σ | |
| 9 (2) | |) | 9 | I | Y | i | y | | | ク | ケ | ル | ル | γ | γ | |
| A (3) | | * | : | J | Z | j | z | | | エ | コ | ン | レ | j | 〒 | |
| B (4) | | + | ; | K | C | k | c | | | オ | サ | ヒ | ロ | × | π | |
| C (5) | | , | < | L | ¥ | l | l | | | カ | シ | フ | フ | φ | π | |
| D (6) | | - | = | M | J | m |) | | | ユ | ヌ | へ | ン | も | ÷ | |
| E (7) | | . | > | N | ^ | n | → | | | ヨ | セ | ホ | ° | ñ | | |
| F (8) | | / | ? | O | _ | o | + | | | ッ | リ | マ | ° | ö | ■ | |

Lower 4-bit of character code (Hex.)

15. Revision records

| Version | Ref.pages | Revision Items | Date |
|----------------|------------------|-----------------------|-------------------|
| A00 | All pages | New release | 2012.04.27 |
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