

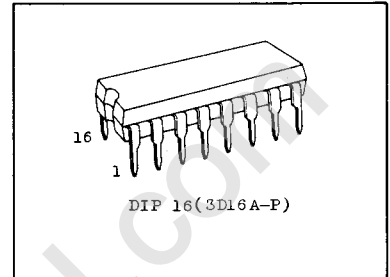
TC40104BP 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH 3-STATE OUTPUTS

TC40194BP 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH ASYNCHRONOUS MASTER RESET

The TC40104BP and TC40194BP are 4-bit shift registers with parallel output, parallel input, shift right and shift left inputs.

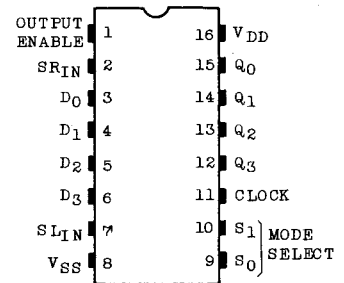
To the TC40104BP is attached OUTPUT ENABLE input which can place output terminal into high impedance. Also, to the TC40194BP is attached RESET input which can clear the contents of registers asynchronously. In parallel data preset mode, data of D<sub>0</sub>~D<sub>3</sub> are not only preset in the internal register, but output to each Q output, at the rise of clock, Shift right and shift left inputs are inhibited during the time. In shift right and shift left modes, data from shift right and shift left inputs are shifted to the right and to the left by 1 bit, respectively, synchronously with the rise of clock.

The TC40194BP is function and pin compatible with the 74194 of TTL.

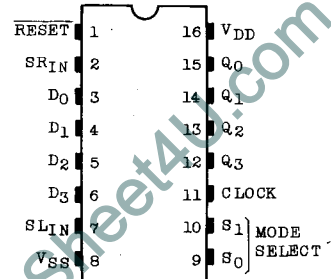


PIN ASSIGNMENT (TOP VIEW)

TC40104BP



TC40194BP

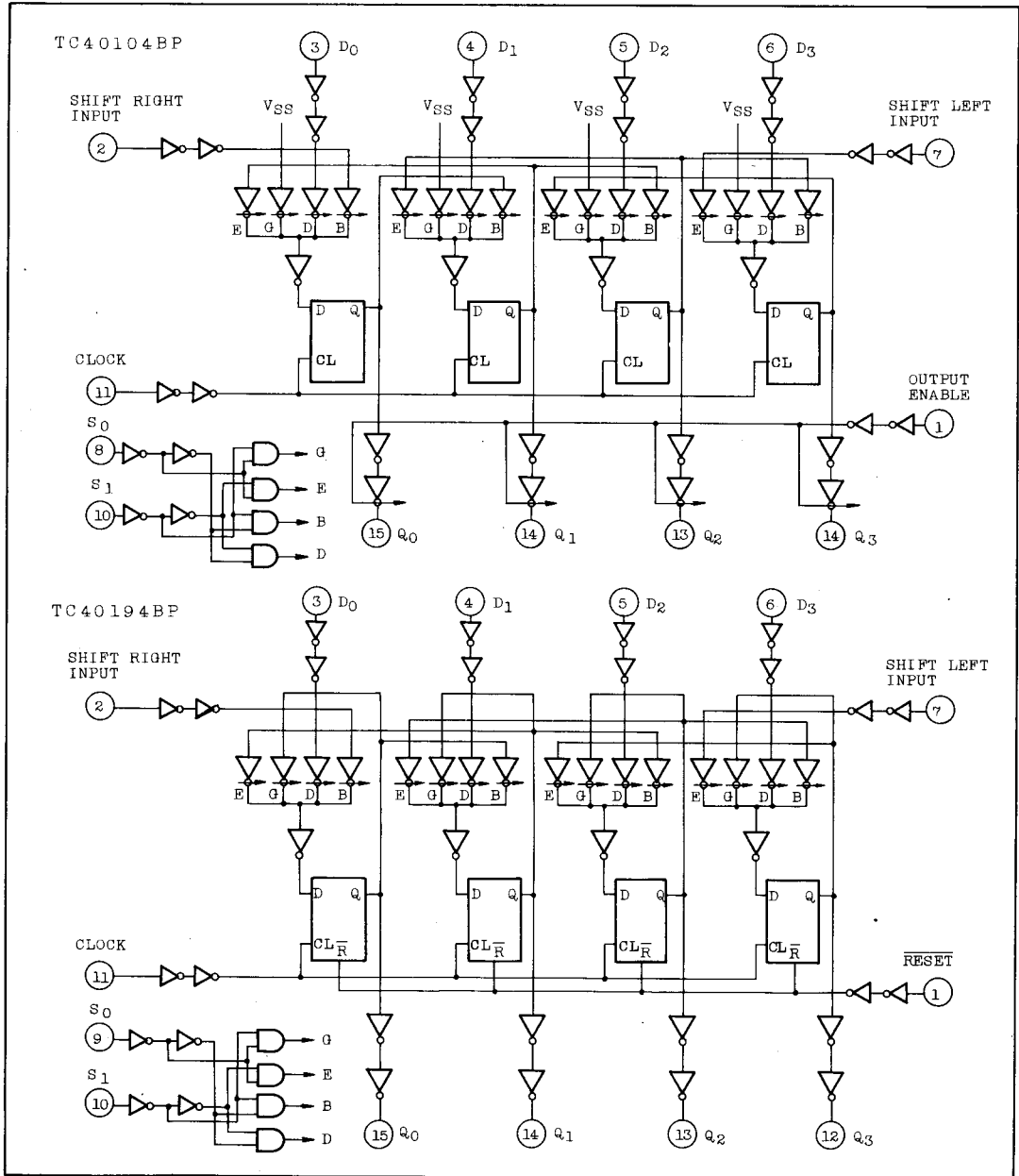


TRUTH TABLE

TC40104BP				
CLOCK	MODE SELECT		OUTPUT ENABLE	OPERATION MODE
	S <sub>0</sub>	S <sub>1</sub>		
	L	L	H	RESET
	H	L	H	SHIFT RIGHT(Q <sub>0</sub> →Q <sub>1</sub> →Q <sub>2</sub> →Q <sub>3</sub> )
	L	H	H	SHIFT LEFT(Q <sub>3</sub> →Q <sub>2</sub> →Q <sub>1</sub> →Q <sub>0</sub> )
	H	H	H	PARALLEL DATA PRESET
*	*	*	L	OUTPUT HIGH IMPEDANCE
* : Don't care				
TC40194BP				
CLOCK	MODE SELECT		RESET	OPERATION MODE
	S <sub>0</sub>	S <sub>1</sub>		
*	L	L	H	HOLD
	H	L	H	SHIFT RIGHT(Q <sub>0</sub> →Q <sub>1</sub> →Q <sub>2</sub> →Q <sub>3</sub> )
	L	H	H	SHIFT LEFT(Q <sub>3</sub> →Q <sub>2</sub> →Q <sub>1</sub> →Q <sub>0</sub> )
	H	H	H	PARALLEL DATA PRESET
*	*	*	L	RESET
* : Don't care				

# TC40104BP, TC40194BP

## LOGIC DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
DC Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	PD	300	mW
Operating Temperature Range	T <sub>A</sub>	-40 ~ 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C · 10sec	

RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V <sub>DD</sub>	3	-	18	V
Input Voltage	V <sub>IN</sub>	0	-	V <sub>DD</sub>	V

STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-	0.05	-	0.00	0.05	-	0.05	V
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> =4.6V V <sub>OH</sub> =2.5V V <sub>OH</sub> =9.5V V <sub>OH</sub> =13.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			5	0.61	-	0.51	1.5	-	0.42	-	
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>OL</sub> =0.5V V <sub>OL</sub> =1.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	0.61	-	0.51	1.5	-	0.42	-	mA
			10	1.5	-	1.3	3.8	-	1.1	-	
			15	4.0	-	3.4	15.0	-	2.8	-	
			5	0.61	-	0.51	1.5	-	0.42	-	

# TC40104BP, TC40194BP

## STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
Input High Voltage	V <sub>IH</sub>	V <sub>OUT</sub> =0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V	
		V <sub>OUT</sub> =1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-		
		V <sub>OUT</sub> =1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.0	-		
		I <sub>OUT</sub>   < 1μA										
Input Low Voltage	V <sub>IL</sub>	V <sub>OUT</sub> =0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V	
		V <sub>OUT</sub> =1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0		
		V <sub>OUT</sub> =1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0		
		I <sub>OUT</sub>   < 1μA										
Input Current	"H" Level	I <sub>IH</sub>	V <sub>IH</sub> =18V	18	-	0.1	-	10-5	0.1	-	1.0	μA
	"L" Level	I <sub>IL</sub>	V <sub>IL</sub> =0V	18	-	-0.1	-	-10-5	-0.1	-	-1.0	
3-State Output Leakage Current	"H" Level	I <sub>DH</sub>	V <sub>DH</sub> =18V	18	-	0.4	-	10-4	0.4	-	12	μA
	"L" Level	I <sub>DL</sub>	V <sub>DL</sub> =0V	18	-	-0.4	-	-10-4	-0.4	-	-12	
Quiescent Device Current	I <sub>DD</sub>	V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub> *	5	-	5	-	0.005	5	-	150	μA	
			10	-	10	-	0.010	10	-	300		
			15	-	20	-	0.015	20	-	600		

© Only TC40104BP \* All valid input combinations.

## DYNAMIC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C, V<sub>SS</sub>=0V, C<sub>L</sub>=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t <sub>TLH</sub>		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t <sub>THL</sub>		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t <sub>pLH</sub> t <sub>pHL</sub>		5	-	220	440	ns
			10	-	90	200	
			15	-	60	140	
Three State Disable Time (OUTPUT ENABLE - Q) ©	t <sub>pZH</sub> t <sub>pZL</sub>	R <sub>L</sub> =1kΩ	5	-	80	160	ns
			10	-	35	70	
			15	-	25	50	

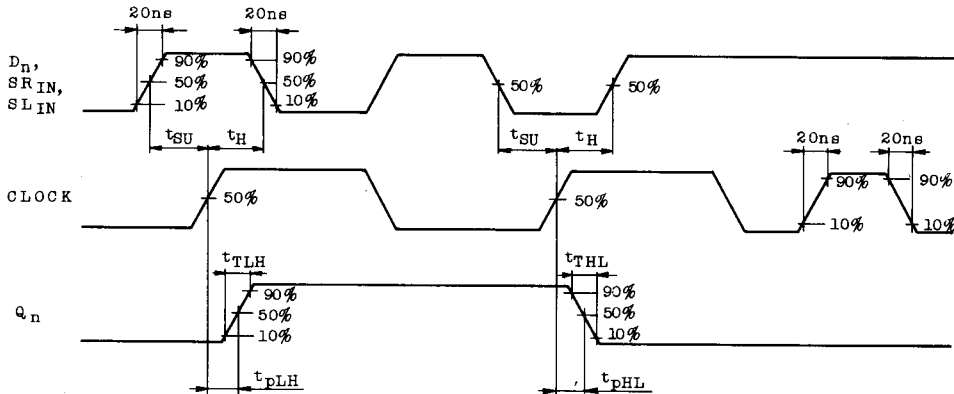
## DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD(V)	MIN.	TYP.	MAX.	UNIT
Three State Disable Time (OUTPUT ENABLE - Q) ©	$t_{pLZ}$ $t_{pHZ}$	$R_L=1k\Omega$	5	-	55	110	ns
			10	-	30	60	
			15	-	25	50	
Propagation Delay Time (RESET - Q) *	$t_{pHL}$		5	-	160	460	ns
			10	-	65	180	
			15	-	50	130	
Min. Clock Pulse Width	$t_w$		5	-	70	180	ns
			10	-	40	80	
			15	-	25	50	
Min. Pulse Width (RESET) *	$t_{WL}$		5	-	100	200	ns
			10	-	40	80	
			15	-	25	50	
Max. Clock Frequency	$f_{CL}$		5	1.5	3	-	MHz
			10	4	8	-	
			15	6	11	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	$t_{rCL}$ $t_{fCL}$		5	20	-	-	$\mu s$
			10	2.5	-	-	
			15	1.0	-	-	
Min. Set-up Time (D0~D3, SRIN, SLIN - CLOCK)	$t_{SU}$		5	-	160	320	ns
			10	-	65	170	
			15	-	40	80	
Min. Set-up Time (S0, S1 - CLOCK)	$t_{SU}$		5	-	200	400	ns
			10	-	80	160	
			15	-	60	120	
Min. Hold Time (D0~D3, SRIN, SLIN - CLCOK)	$t_H$		5	-	-145	0	ns
			10	-	-55	0	
			15	-	-35	0	
Min. Hold Time (S0, S1 - CLOCK)	$t_H$		5	-	-185	0	ns
			10	-	-70	0	
			15	-	-55	0	
Input Capacitance	$C_{IN}$			-	5	7.5	pF

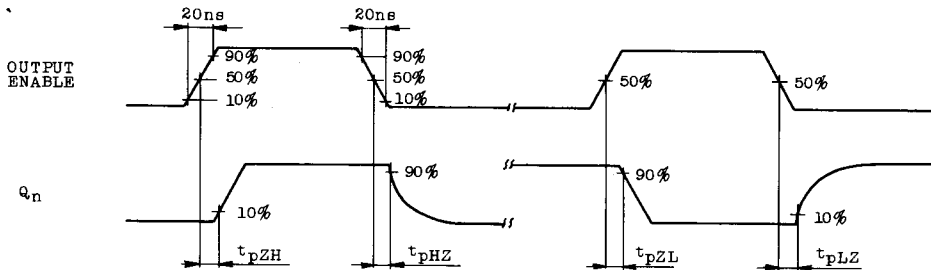
© Only TC40104BP      \* Only TC40194BP

## WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1



WAVEFORM 2



WAVEFORM 3

