TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4021BP,TC4021BF,TC4021BFN

TC4021B 8-Stage Static Shift Register

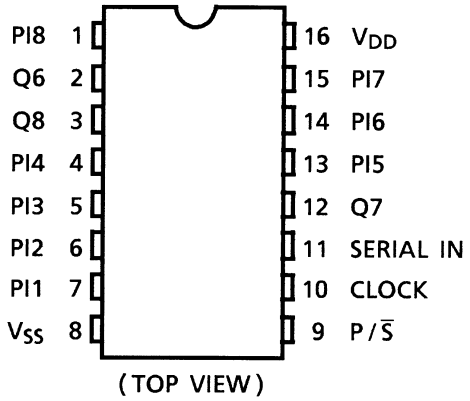
(asynchronous parallel input or synchronous serial input/serial output)

Note: xxxFN (JEDEC SOP) is not available in Japan.

TC4021B is 8 stage parallel in/serial out shift register, which can be used also for serial in/serial out operations. In the case of parallel operation, the data of PARALLEL IN is input to each F/F asynchronously with CLOCK and the output is obtained. In the case of serial operations, each F/F is triggered by rising edge of CLOCK. (asynchronous parallel or synchronous serial input)

Switching of PARALLEL operation and SERIAL operation is achieved by P/$\overline{S}$ CONTROL input. When P/$\overline{S}$ CONTROL input is "H", PARALLEL operation is designated and when it is "L", SERIAL operation is designated.

Pin Assignment



Truth Table

Inputs					Outputs△	
CLOCK△△	P/$\overline{S}$	PI1	Pln	SI	Q1	Qn
↑	L	*	*	L	L	Qn – 1
↑	L	*	*	H	H	Qn – 1
↓	L	*	*	*	No Change	
*	H	L	L	*	L	L
*	H	L	H	*	L	H
*	H	H	L	*	H	L
*	H	H	H	*	H	H

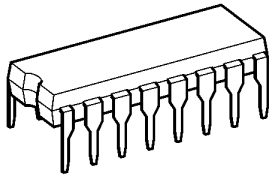
n: 2~8

△: Q1~Q5 internal

△△: Level change

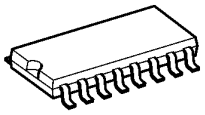
*: Don't care

TC4021BP

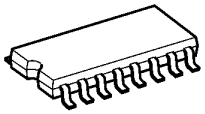


DIP16-P-300-2.54A

TC4021BF

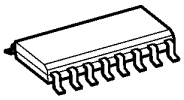


SOP16-P-300-1.27A



SOP16-P-300-1.27

TC4021BFN



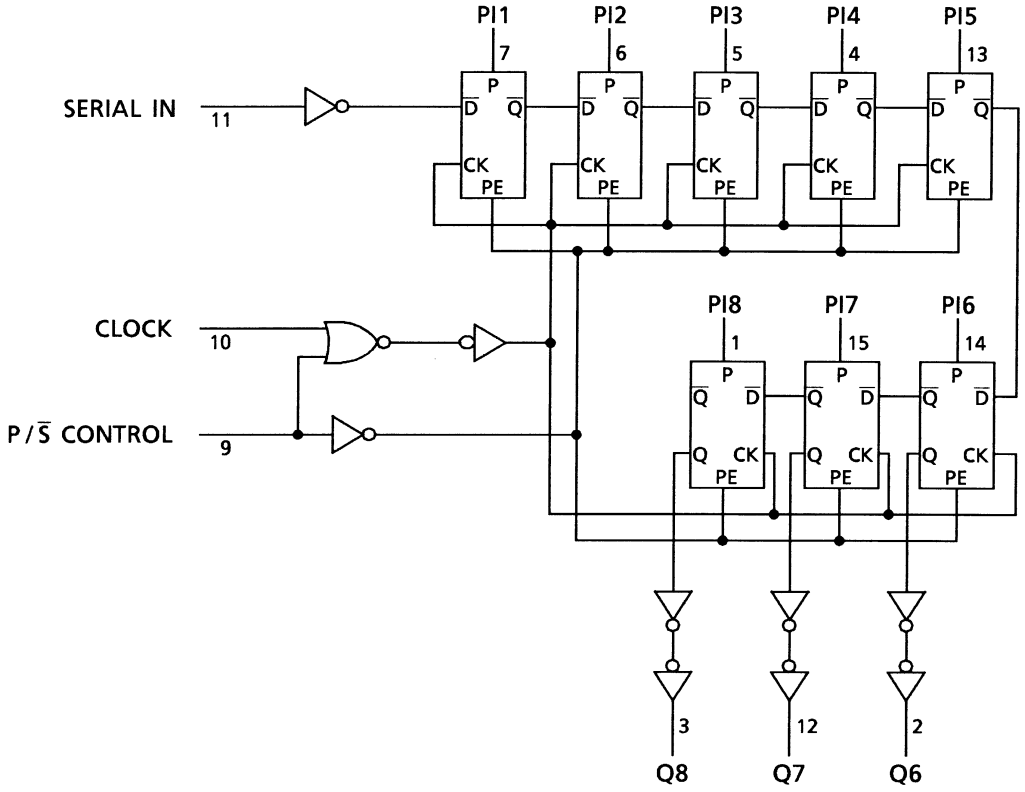
SOL16-P-150-1.27

Weight

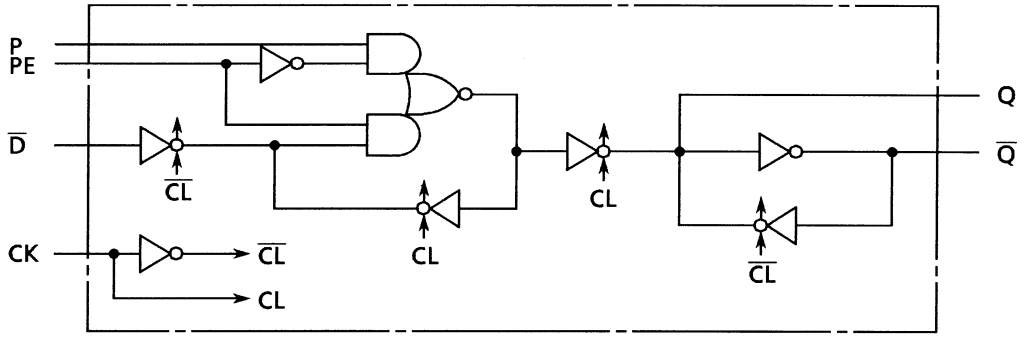
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOP16-P-300-1.27	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

Logic Diagram

Parallel



Internal Flip Flop



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V_{SS} − 0.5~V_{SS} + 20	V
Input voltage	V_{IN}	V_{SS} − 0.5~V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS} − 0.5~V_{DD} + 0.5	V
DC input current	I_{IN}	±10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{opr}	−40~85	°C
Storage temperature range	T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Static Electrical Characteristics (V_{SS} = 0 V)

Characteristics		Sym-bol	Test Condition		−40°C		25°C			85°C		Unit
				V_{DD} (V)	Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage		V_{OH}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
				10	9.95	—	9.95	10.00	—	9.95	—	
				15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage		V_{OL}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
				10	—	0.05	—	0.00	0.05	—	0.05	
				15	—	0.05	—	0.00	0.05	—	0.05	
Output high current		I_{OH}	V_{OH} = 4.6 V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
			V_{OH} = 2.5 V	5	−2.50	—	−2.10	−4.0	—	−1.70	—	
			V_{OH} = 9.5 V	10	−1.50	—	−1.30	−2.2	—	−1.10	—	
			V_{OH} = 13.5 V	15	−4.00	—	−3.40	−9.0	—	−2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Output low current		I_{OL}	V_{OL} = 0.4 V	5	0.61	—	0.51	1.5	—	0.42	—	mA
			V_{OL} = 0.5 V	10	1.50	—	1.30	3.8	—	1.10	—	
			V_{OL} = 1.5 V	15	4.00	—	3.40	15.0	—	2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage		V_{IH}	V_{OUT} = 0.5 V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
			V_{OUT} = 1.0 V, 9.0 V	10	7.0	—	7.0	5.50	—	7.0	—	
			V_{OUT} = 1.5 V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
			$\|I_{OUT}\| < 1$ μA									
Input low voltage		V_{IL}	V_{OUT} = 0.5 V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
			V_{OUT} = 1.0 V, 9.0 V	10	—	3.0	—	4.50	3.0	—	3.0	
			V_{OUT} = 1.5 V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
			$\|I_{OUT}\| < 1$ μA									
Input current	"H" level	I_{IH}	V_{IH} = 18 V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" level	I_{IL}	V_{IL} = 0 V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent supply current		I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	5	—	0.005	5	—	150	μA
				10	—	10	—	0.010	10	—	300	
				15	—	20	—	0.020	20	—	600	

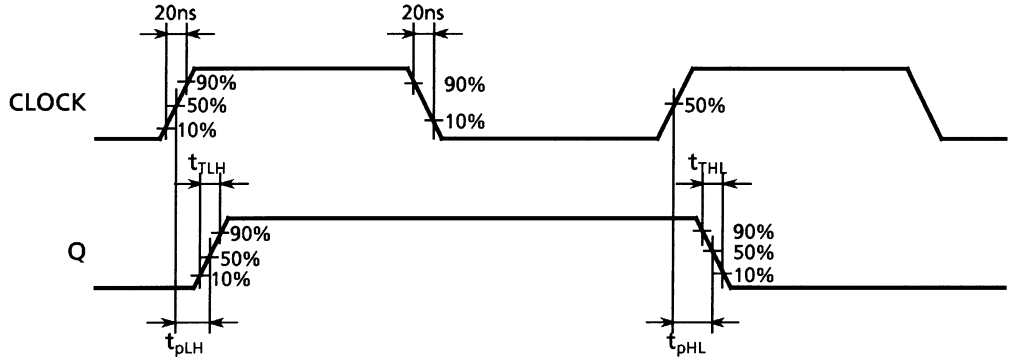
Note: All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

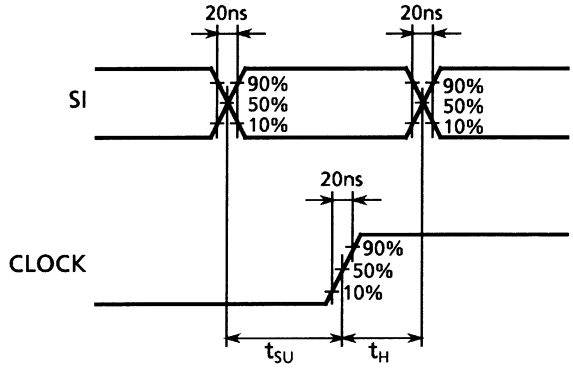
Characteristics	Symbol	Test Condition	V_{DD} (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t_{TLH}	—	5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Output transition time (high to low)	t_{THL}	—	5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation delay time (CLOCK-Q)	t_{pLH} t_{pHL}	—	5	—	150	320	ns
			10	—	65	160	
			15	—	45	120	
Propagation delay time ($P/\overline{S}$ -Q)	t_{pLH} t_{pHL}	—	5	—	230	460	ns
			10	—	90	180	
			15	—	60	120	
Max clock frequency	f_{CL}	—	5	3.0	6.5	—	MHz
			10	6.0	18.0	—	
			15	8.5	24.0	—	
Min clock pulse width	t_W	—	5	—	80	180	ns
			10	—	30	80	
			15	—	20	50	
Max clock rise time Max clock fall time	t_{rCL} t_{fCL}	—	5	20.0	—	—	μs
			10	2.5	—	—	
			15	1.0	—	—	
Min set-up time (SI-CLOCK)	t_{SU}	—	5	—	40	120	ns
			10	—	20	80	
			15	—	15	60	
Min set-up time (PI- $P/\overline{S}$)	t_{SU}	—	5	—	25	50	ns
			10	—	15	30	
			15	—	10	20	
Min hold time (SI-CLOCK), (PI- $P/\overline{S}$)	t_H	—	5	—	35	70	ns
			10	—	20	40	
			15	—	15	30	
Min pulse width ($P/\overline{S}$ -CONTROL)	t_{WH}	—	5	—	90	180	ns
			10	—	30	80	
			15	—	10	50	
Min removal time ($P/\overline{S}$ -CLOCK)	t_{rem}	—	5	—	45	280	ns
			10	—	20	140	
			15	—	15	100	
Input capacitance	C_{IN}	—		—	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics

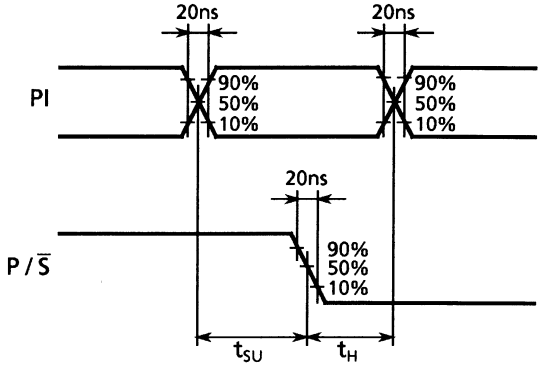
Waveform 1



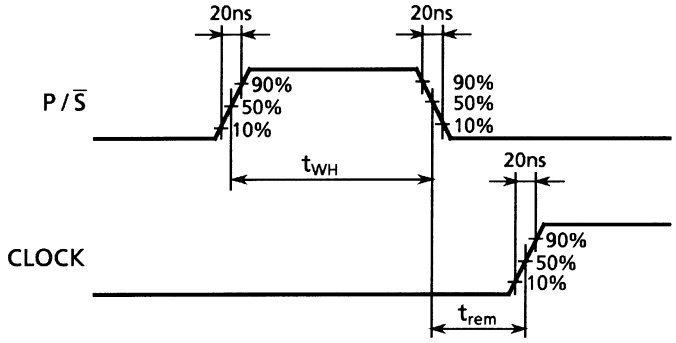
Waveform 2



Waveform 3

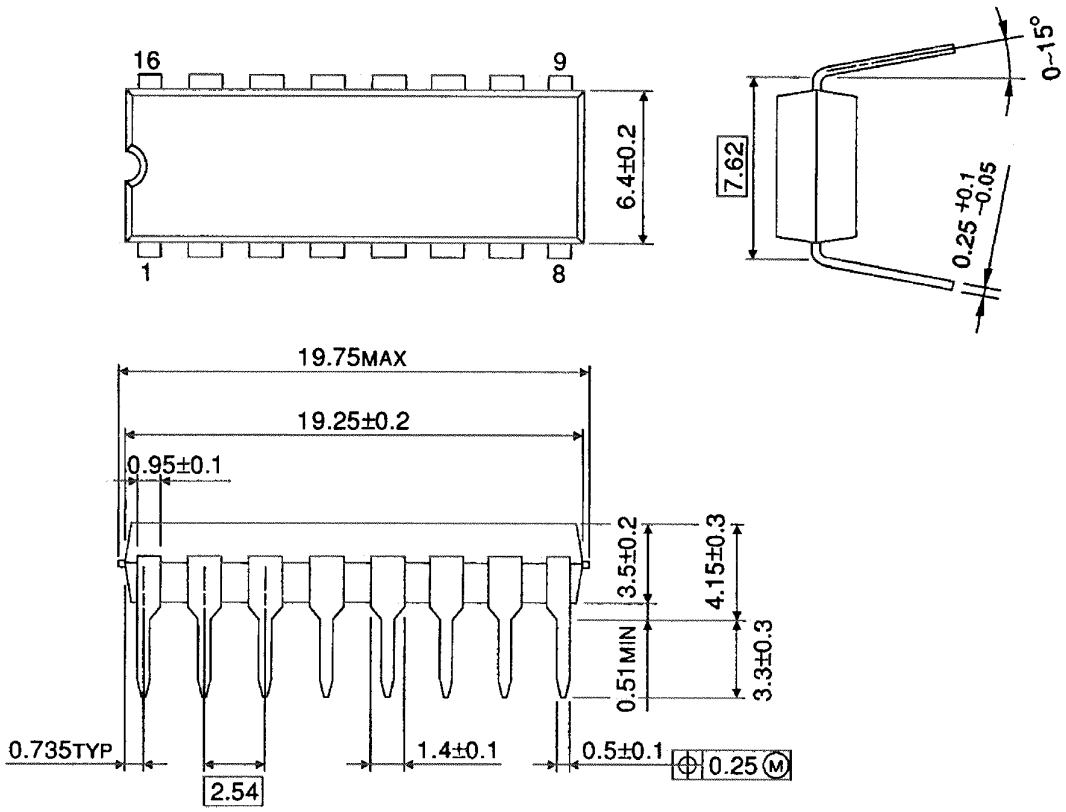


Waveform 4



Package Dimensions

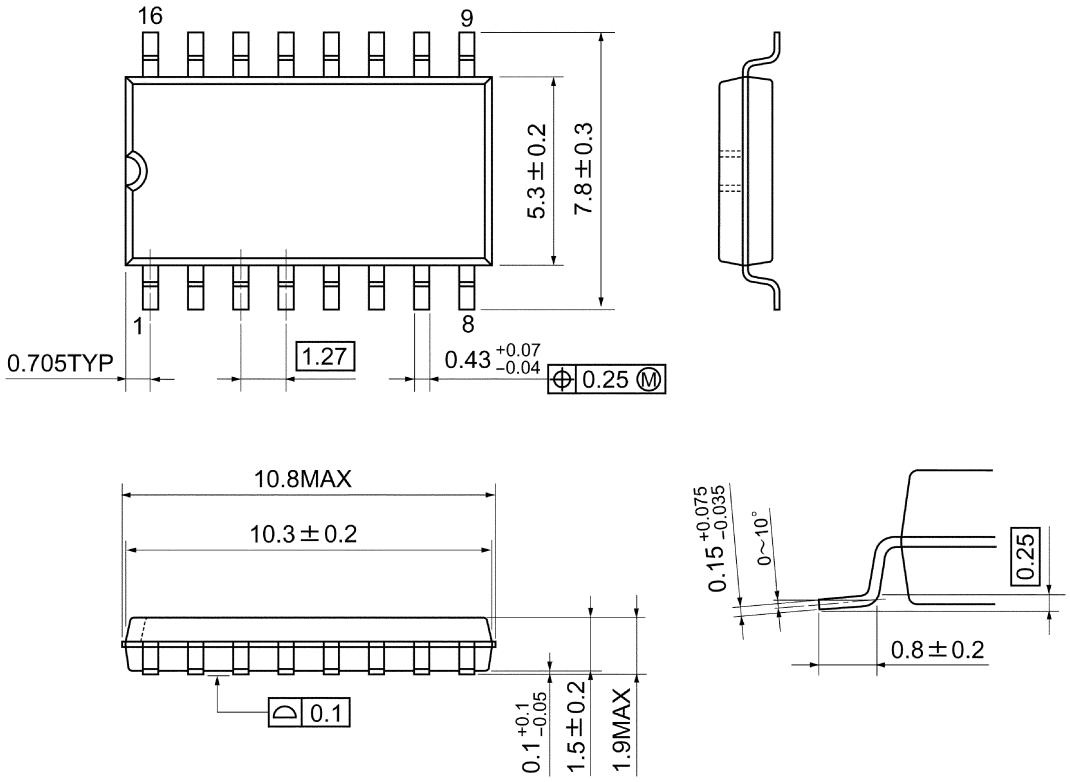
DIP16-P-300-2.54A Unit : mm



Weight: 1.00g (typ.)

Package Dimensions

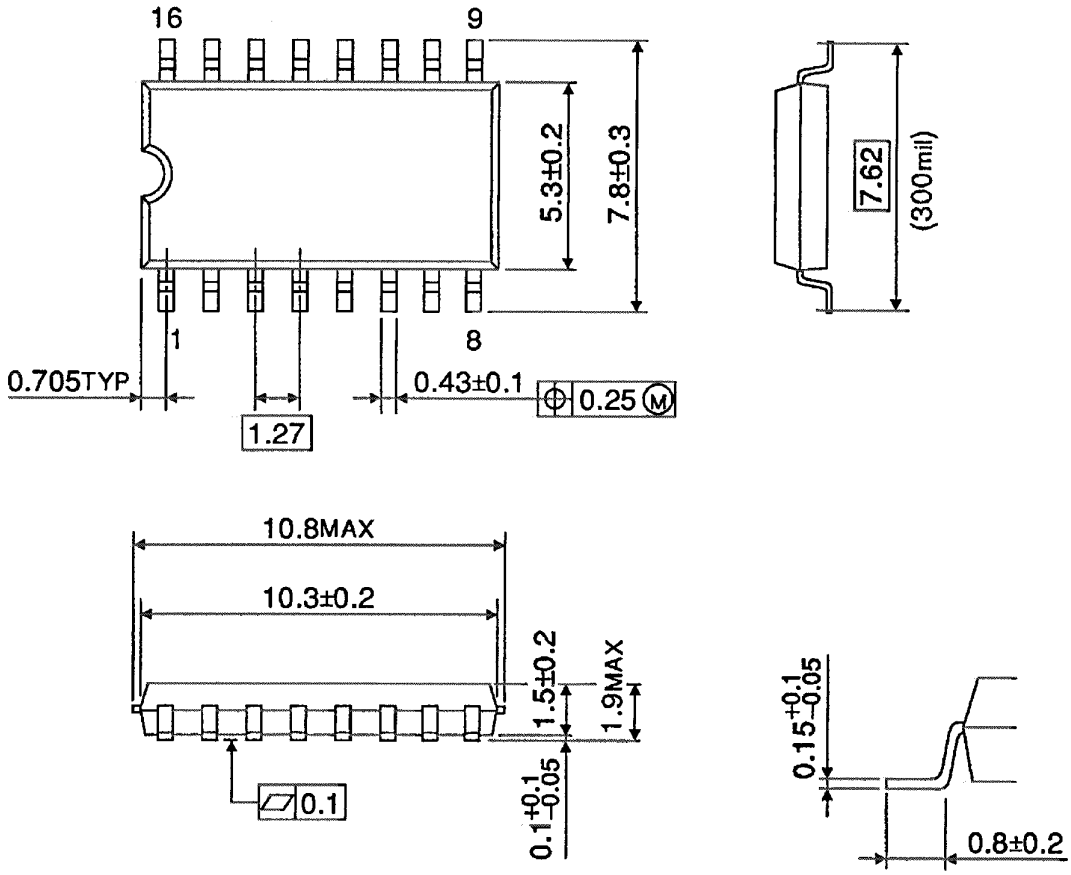
SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

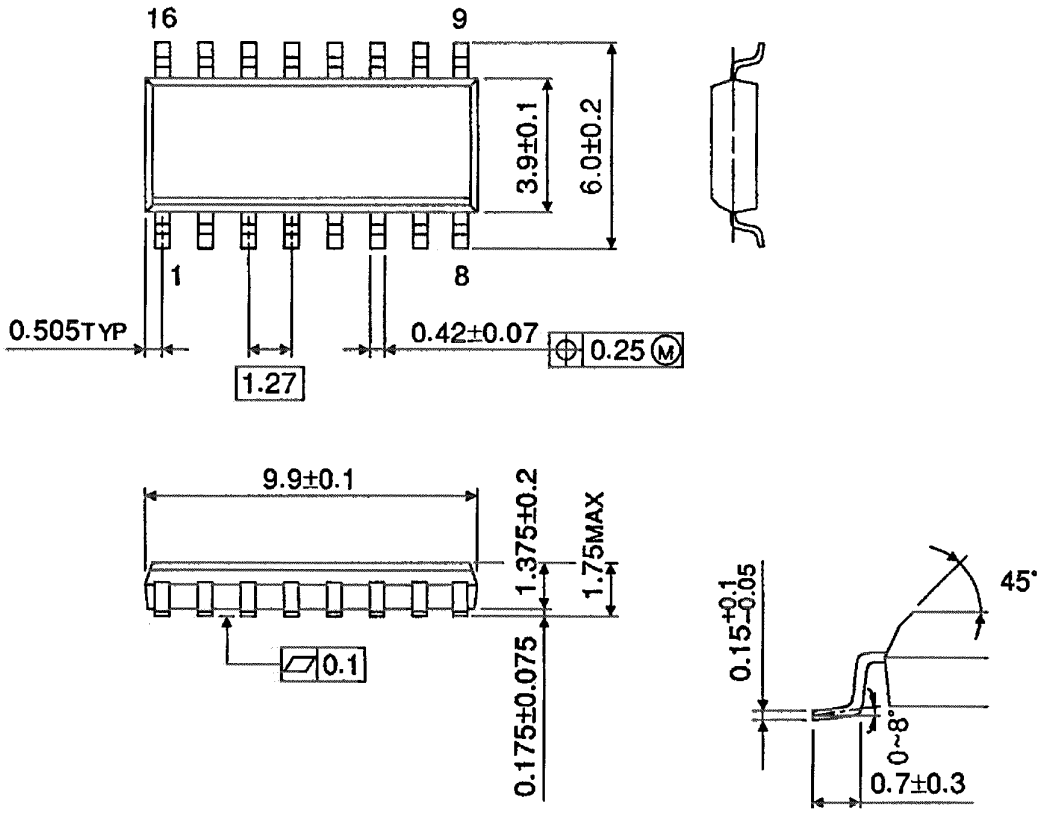
SOP16-P-300-1.27 Unit : mm



Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Note: Lead (Pb)-Free Packages

DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27

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