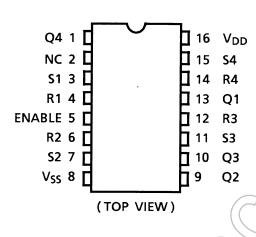
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4044BP, TC4044BF

TC4044B Quad 3-State R/S Latch (quad NAND R/S latch)

TC4044B the latches composed by four independent R/S flip-flop circuits. TC4044B fabricated with NAND gates is suitable for data processing of four bits configuration. Four output lines can have high impedance regardless of the contents of latches by means of common ENABLE input to make connection to the bus lines easy.

Pin Assignment



SOP16-P-300-1.27A Weight DIP16-P-300-2.54A : 1. SOP16-P-300-1.27A : 0.

DIP16-P-300-2.54A

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TC4044BP

TC4044BF

: 1.00 g (typ.) : 0.18 g (typ.)

Truth Table

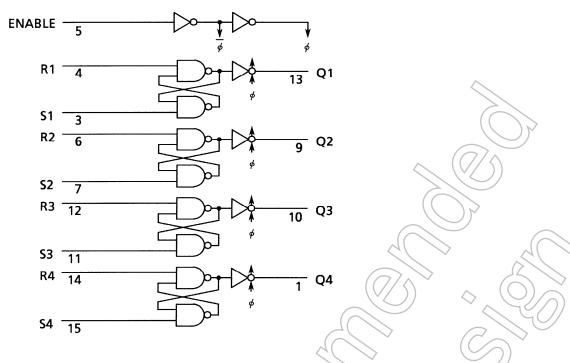
R	S	E.	
*	*	L	HZ
L	L	Н	L
L	Н	Ŧ	L
Н	L	H	И
н	н (H	No Change
*: Don	't care		

HZ: High impedance

Start of commercial production 1978-04

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Logic Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol 🗸	Rating	Unit
DC supply voltage	V _{DD}	V_{SS} – 0.5 to V_{SS} + 20	V
Input voltage	VIN	V_{SS} – 0.5 to V_{DD} + 0.5	V
Output voltage	VOUT	V _{SS} – 0.5 to V _{DD} + 0.5	V
DC input current	$\left(\left(I_{N} \right) \right)$	±10	mA
Power dissipation	PD	300 (DIP)/180 (SOIC)	mW
Operating temperature range	Topr	-40 to 85	°C
Storage temperature range	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V _{DD}	—	3	_	18	V
Input voltage	V _{IN}	_	0		V _{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics ($V_{SS} = 0 V$)

		Sym-	Test Condition		-40°C		25°C			85°C		
Charac	teristics	bol		V _{DD} (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit
High-level output voltage			I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	4.95	_	4.95	5.00	_	4.95	_	
		VOH		10	9.95	—	9.95	10.00 <	_	9.95	_	V
Ū			VIN - VSS, VDD	15	14.95	_	14.95	15.00	λ	14.95		
			I _{OUT} < 1 μΑ	5	—	0.05	—	0.00	0.05)	0.05	
Low-level voltage	output	V _{OL}	$V_{IN} = V_{SS}, V_{DD}$	10	—	0.05	—	0.00	0.05	2_	0.05	V
			VIN - VSS, VDD	15	_	0.05	\wedge	0.00	0.05	—	0.05	
			V _{OH} = 4.6 V	5	-0.61	—	-0.51	-1.0		-0.42	—	mA
			V _{OH} = 2.5 V	5	-2.50	—	-2.10	-4.0	> —	-1.70	—	
Output hig	h current	Iон	V _{OH} = 9.5 V	10	-1.50	—	-1.30	-2.2	—	-1.10	_	
			V _{OH} = 13.5 V	15	-4.00	- <	-3.40	9.0	—	-2.80	\searrow	
			$V_{IN} = V_{SS}, V_{DD}$			6				\geq		
			$V_{OL} = 0.4 V$	5	0.61	((//	0.51	1.2	-((0.42	_	mA
	/ current	I _{OL}	$V_{OL} = 0.5 V$	10	1.50	\sim	1.3	3.2	$\langle \mathcal{K} \rangle$	(1.10	/ —	
Output low	Output low current		V _{OL} = 1.5 V	15	4.00		3.4	12.0	2-/	2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$		20				$\langle \rangle$			
		VIH	$V_{OUT} = 0.5 V, 4.5 V$	5	3.5	>-	3.5	2.75		3.5	_	V
Input high	voltage		V _{OUT} = 1.0 V, 9.0 V	10	7.0	—	7.0	5.50) —	7.0	—	
input nigh	voltage		V _{OUT} = 1.5 V, 13.5 V	15	11,0	_//	11.0	8.25	_	11.0	—	
			$ I_{OUT} < 1 \mu A$									
			V _{OUT} = 0.5 V, 4.5 V	5	—	1.5	\searrow	2.25	1.5	—	1.5	
Input low y	voltage	VIL	V _{OUT} = 1.0 V, 9.0 V	_10	—	3.0		4.50	3.0	—	3.0	v
inpution	Input low voltage		V _{OUT} = 1.5 V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	ľ
			I _{OUT} <1 µA		~	\mathcal{N}	\geq					
Input	"H" level	Чн	VIH = 18 V	18	1	0.1		10 ⁻⁵	0.1		1.0	μA
current	"L" level	h	V _{IL} = 0 V	18	(\overline{q})	0.1		-10 ⁻⁵	-0.1		-1.0	μι
3-state output	"H" level	IDH	V _{OH} = 18 V	18		0.4	_	10 ⁻⁴	0.4	_	12	μA
leakage current	"L" level	I _{DL}	V _{OL} ≓0V	18		-0.4	_	-10 ⁻⁴	-0.4	—	-12	pur i
Quiescent supply		R.		5	> —	1	—	0.002	1	—	30	
		IDD	$V_{IN} = V_{SS}, V_{DD}$ (Note)	10	—	2	—	0.004	2	—	60	μA
~	$(\bigcirc$			15	—	4	—	0.008	4	—	120	

Note: All valid input combinations.

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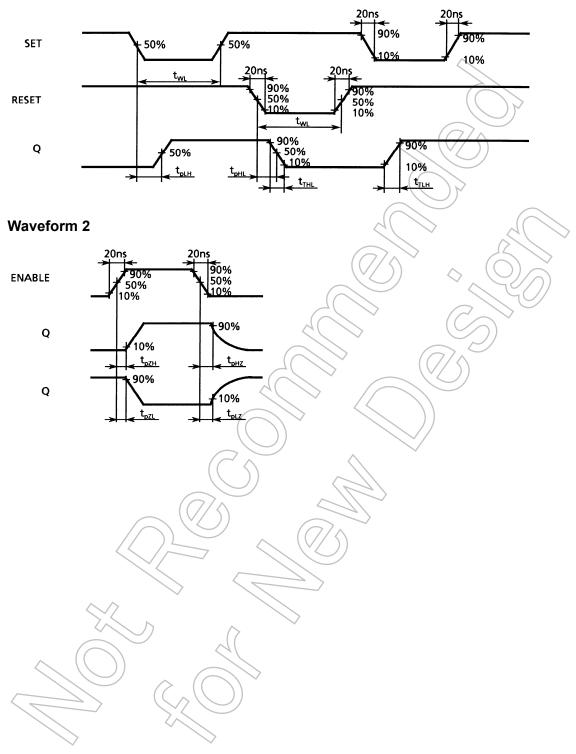
Dynamic Electrical Characteristics (Ta = 25° C, V_{SS} = 0 V, C_L = 50 pF)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
	Cymbol		V _{DD} (V)	IVIIII	۰ <i>۶</i> p.	IVIAX	Onic
Output transition time			5	_	70	200	
	t _{TLH}	—	10		35	100	ns
(low to high)			15	\searrow	30	80	
Output transition time			5	(=)	70	200	
	t _{THL}	—	10		35	100	ns
(high to low)			15	VA -	30	80	
Propagation delay time	+		5	Ì	90	300	
(SET, RESET-Q)	t _{pLH}	—	10	10 —	45	140	ns
(SET, RESET-Q)	^t pHL		15	15 —		100	
3-state propagation delay time	^t pHZ ^t pLZ	~(5		55	180	
(ENABLE-Q)		$R_L = 1 k\Omega$	10	- (35	100	ns
		(7/1)	15	-(30	70	
3-state propagation delay time	t. 70		5 🛇	~	55	180	
(ENABLE-Q)	^t pZH ^t pZL	$R_L = 1 k\Omega$	10	\rightarrow	30	100	ns
			15		25	70	
Min pulse width			5	Ð	25	160	
(SET, RESET)	t _{WL}		(10/<	-	20	80	ns
			15	/ _	20	40	
Input capacitance	C _{IN}	\searrow \checkmark \checkmark		—	5	7.5	pF

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Waveforms for Measurement of Dynamic Characteristics

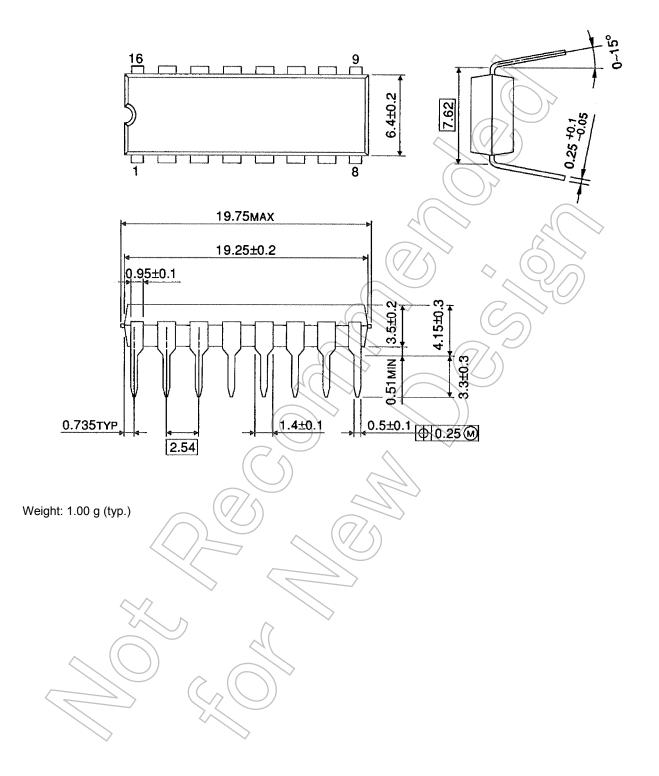
Waveform 1



Package Dimensions

DIP16-P-300-2.54A

Unit : mm

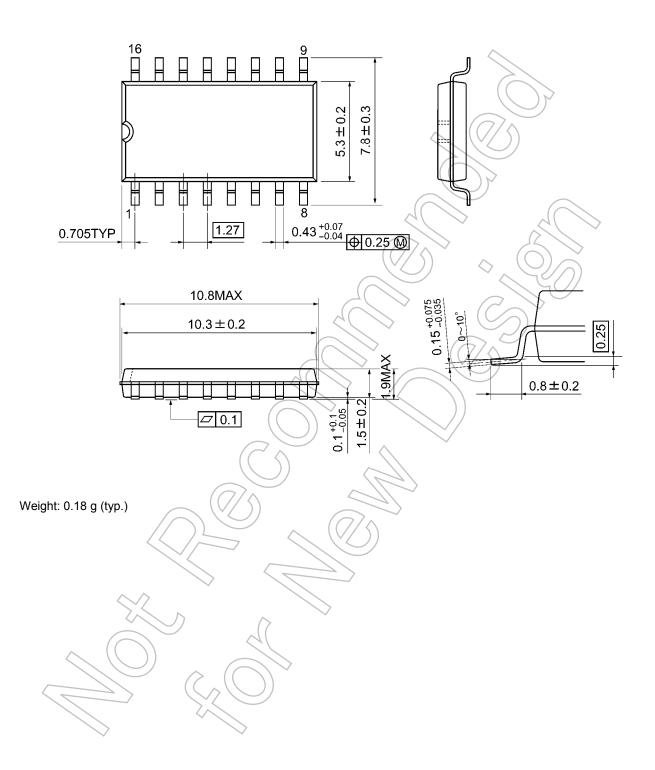




Package Dimensions

SOP16-P-300-1.27A

Unit: mm



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