

TC4076BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4076BP 4-BIT D-TYPE REGISTER

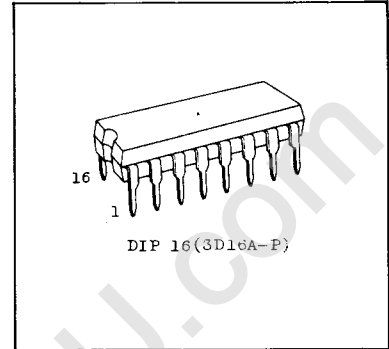
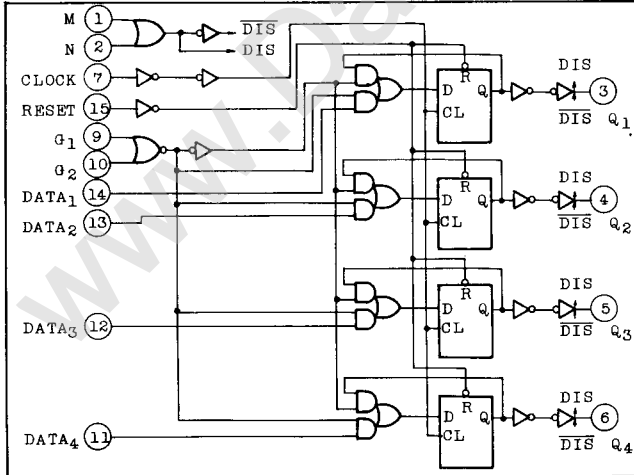
TC4076BP is the register which consists of four D type flip-flops having 3-stage outputs, and these four flip-flops are controlled by common CLOCK input and RESET input.

When both of INPUT DISABLE inputs G₁ and G₂ are at "L", data inputs D₁ through D₄ are stored in F/F's at the rising edge of CLOCK input, and with other combination of G₁ and G₂, the previous conditions of F/F's are retained even if the rising edge of CLOCK occurs. When both of OUTPUT DISABLE inputs M and N are at "L", the outputs of flip-flops appear at Q₁ through Q₄ outputs, and with any other combinations of M and N, the outputs have high impedance. RESET is active with "H" level.

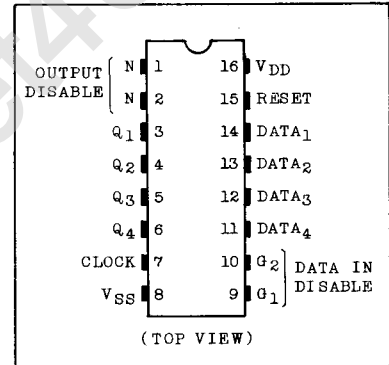
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +20	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300	mW
Operating Temperature Range	T _A	-40 ~ 85	°C
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10 sec	

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

RESET	CLOCK	DATA IN DISABLE		DATA	OUTPUT DISABLE		Q _{n+1}
		G ₁	G ₂		M	N	
*	*	*	*	*	H	*	HZ
*	*	*	*	*	*	H	HZ
H	*	*	*	*	L	L	L
L	L	*	*	*	L	L	Q _n
L	f	H	*	*	L	L	Q _n
L	f	*	H	*	L	L	Q _n
L	f	L	L	H	L	L	H
L	f	L	L	L	L	L	L
L	H	*	*	*	L	L	Q _n
L	L	*	*	*	L	L	Q _n

Q_{n+1} : NEXT STATE of Q_n
 HZ : HIGH IMPEDANCE
 * : Don't care

RECOMMENDED OPERATING CONDITIONS (VSS=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	VDD	3	-	18	V
Input Voltage	VIN	0	-	VDD	V

STATIC ELECTRICAL CHARACTERISTICS (VSS=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	VCC (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	VOH	IOUT < 1μA VIN=VSS,VDD	5	4.95	-	4.95	5.00	-	4.95	-	V	
			10	9.95	-	9.95	10.00	-	9.95	-		
			15	14.95	-	14.95	15.00	-	14.95	-		
Low-Level Output Voltage	VOL	IOUT < 1μA VIN=VSS,VDD	5	-	0.05	-	0.00	0.05	-	0.05	V	
			10	-	0.05	-	0.00	0.05	-	0.05		
			15	-	0.05	-	0.00	0.05	-	0.05		
Output High Current	IOH	VOH=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA	
		VOH=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-		
		VOH=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-		
		VOH=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-		
		VIN=VSS,VDD										
Output Low Current	IOL	VOL=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	mA	
		VOL=0.5V	10	1.5	-	1.3	3.8	-	1.1	-		
		VOL=1.5V	15	4.0	-	3.4	15.0	-	2.8	-		
		VIN=VSS,VDD										
Input High Voltage	VIH	VOUT=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V	
		VOUT=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-		
		VOUT=1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.0	-		
		IOUT < 1μA										
Input Low Voltage	VIL	VOUT=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V	
		VOUT=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0		
		VOUT=1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0		
		IOUT < 1μA										
Input Current	"H" Level	IIH	VIH=18V	18	-	0.1	-	10 ⁻⁵	0.1	-	1.0	μA
	"L" Level	IIL	VIL=0V	18	-	-0.1	-	-10 ⁻⁵	-0.1	-	-1.0	

TC4076BP

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYM-BOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I _{DH}	V _{OUT} =18V	18	-	0.4	-	10 ⁻⁴	0.4	-	12	μA
	"L" Level	I _{DL}	V _{OUT} =0V	18	-	-0.4	-	-10 ⁻⁴	-0.4	-	-12	
Quiescent Device Current		I _{DD}	V _{IN} =V _{SS} , V _{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

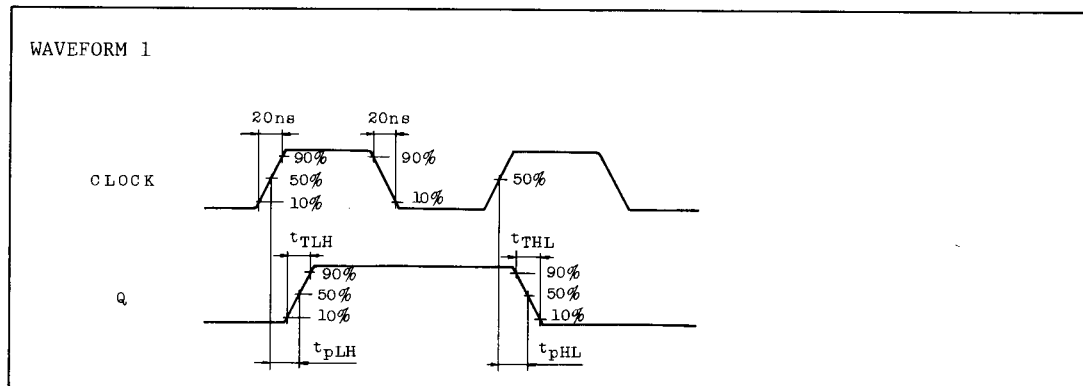
DYNAMIC ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t _{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t _{PLH} t _{pHL}		5	-	250	600	ns
			10	-	95	250	
			15	-	65	180	
Propagation Delay Time (RESET - Q)	t _{pHL}		5	-	230	460	ns
			10	-	90	200	
			15	-	60	150	
Three State Disable Time (OUTPUT DISABLE - Q)	t _{pHZ} t _{pLZ}	R _L =1kΩ	5	-	100	300	ns
			10	-	45	120	
			15	-	35	90	
Three State Disable Time (OUTPUT DISABLE - Q)	t _{pZH} t _{pZL}	R _L =1kΩ	5	-	110	300	ns
			10	-	40	150	
			15	-	30	120	
Max. Clock Frequency	f _{CL}		5	3	7	-	MHz
			10	6	21	-	
			15	8	24	-	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Min. Clock Pulse Width	t _w		5	-	70	200	ns
			10	-	25	100	
			15	-	20	80	
Min. Pulse Width (RESET)	t _{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t _{rCL}		5	20	-	-	μs
	t _{fCL}		10	2.5	-	-	
			15	1.0	-	-	
Min. Set-up Time (DATA - CLOCK)	t _{SU}		5	-	75	150	ns
			10	-	30	60	
			15	-	20	40	
Min. Set-up Time (DATA INPUT DISABLE - CLOCK)	t _{SU}		5	-	100	200	ns
			10	-	40	80	
			15	-	25	50	
Min. Hold Time (DATA - CLOCK)	t _H		5	-	-	135	ns
			10	-	-	60	
			15	-	-	50	
Input Capacitance	C _{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



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