

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H076P/F

TC40H076AP/AF

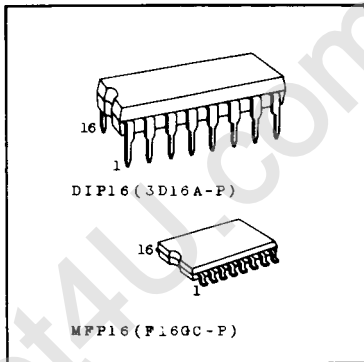
TC40H076 DUAL J-K FLIP-FLOP (PULSE TRIGGER TYPE)

TC40H076A DUAL J-K FLIP-FLOP (EDGE TRIGGER TYPE)

The TC40H076 is a dual J-K flip-flop with a synchronous clear preset function.

J-K mode: When both of CLEAR and PRESET are set to "H" level, and provided with CLOCK input, the output varies at the CLOCK 1 pulse for the TC40H076 and at the falling edge of CLOCK for the TC40H076A, depending on the conditions of J and K.

R-S mode: When CLEAR is set to "L" level and PRESET to "H" level, Q goes to "H" level and \bar{Q} to "L" level regardless of the other inputs.



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300(DIP)/180(MFP)	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C • 10 sec	

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	2.0	-	8.0	V
Input Voltage	V _{IN}	0	-	V _{DD}	V
Operating Temperature	T _{opr}	-40	-	85	°C

TRUTH TABLE (TC40H076)

INPUTS			OUTPUTS			
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
L	H	*	*	*	H	L
H	L	*	*	*	L	H
L	L	*	*	*	H	H
H	H		L	L	NO CHANGE	
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	TOGGLE	

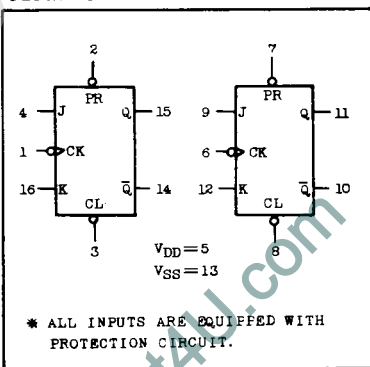
* Don't Care

One high-Level Pulse

Transition from Low to high level.

Transition from high to Low level.

BLOCK DIAGRAM



TRUTH TABLE (TC40H076A)

INPUTS			OUTPUTS			
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
L	H	*	*	*	H	L
H	L	*	*	*	L	H
L	L	*	*	*	H	H
H	H		L	L	NO CHANGE	
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	TOGGLE	
H	H		x	x	NO CHANGE	

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RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0.0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	-	2.0	-	8.0	V
Input Voltage	VIN	-	0.0	-	VDD	V
Operating Temperature	t _{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS ($V_{SS}=0.0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I _{OH}	V _{OH} =4.6V $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V $V_{IN}=V_{SS}, V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level V _{IH}	$ I_{OUT} < 1\mu A$ V _{OH} =4.5V V _{IL} =0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V _{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level I _{IH}	V _{IH} =8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level I _{IL}	V _{IL} =0.0V	8	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	5.0	-	10 ⁻²	5.0	-	25.0	μA

*All valid input combinations

SWITCHING CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0.0V$, $C_L=15pF$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t _{or}	Circuit 1	5	-	24	40	ns
Output Fall Time	t _{of}	Circuit 1	5	-	18	40	
Propagation Delay Time	(Low-High)	t _{pLH}	5	-	27	50	ns
	(High-Low)	t _{pHL}		CLOCK-Q, \bar{Q}	-	37	
Propagation Delay Time	(Low-High)	t _{pLH}	5	-	40	60	ns
	(High-Low)	t _{pHL}		CLOCK, \overline{PR} -Q, \bar{Q}	-	56	
Max. Clock Frequency	f _{MAX} ∅		5	10	20	-	MHz
Min. Data Setup Time	t _{set up}	Circuit 3 TC40H076A	5	-	-	25	ns
Min. Data Setup Time	t _{set up}	Circuit 2 TC40H076	5	-	-	0	ns
Min. Data Hold Time	t _{hold}	Circuit 3 TC40H076A	5	-	-	0	ns
Min. Data Hold Time	t _{hold}	Circuit 2 TC40H076	5	-	-	0	ns
Min. Clear and Preset Pulse Width	t _w	Circuit 1 CLEAR, PRESET	5	-	23	40	ns

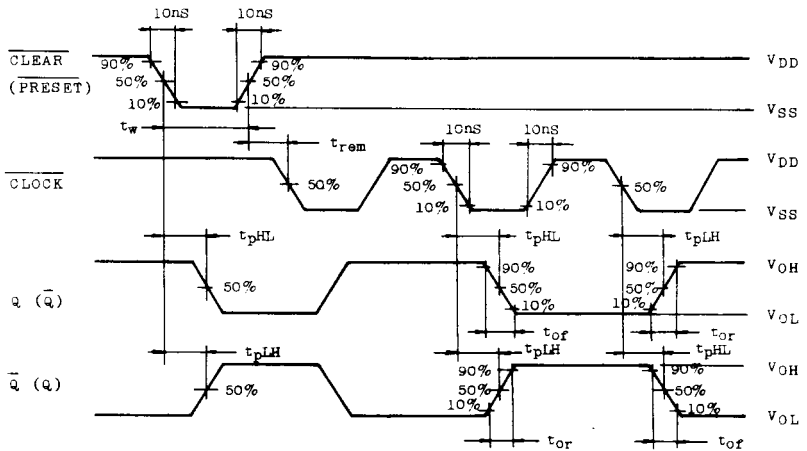
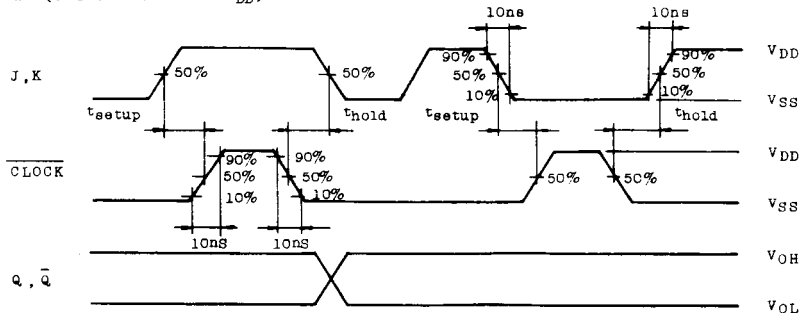
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CHARACTERISTIC	SYMBOL	TEST CONITION	V _{DD}	MIN.	TYP.	MAX.	UNIT
			(V)				
Max. Clock Rise Time	$t_{r\phi}$		5	0.5	-	-	μ S
Max. Clock Fall Time	$t_{f\phi}$		5	-	-	-	μ S
Min. Clear and Preset Removal Time	t_{rem}	CIRCUIT 1	5	-	15	30	ns
Input Capacitance	C_{IN}			-	5	-	pF

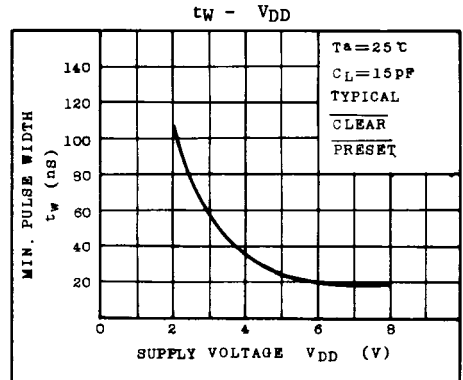
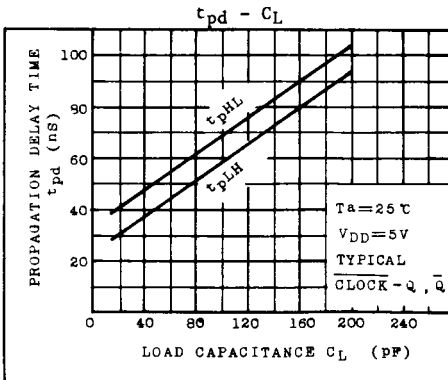
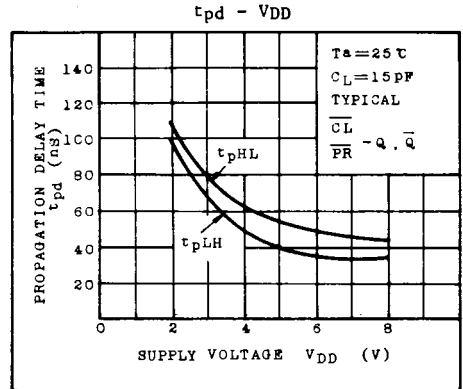
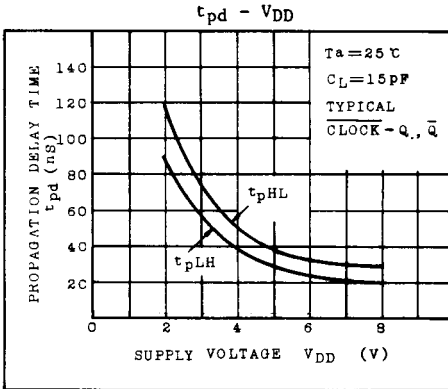
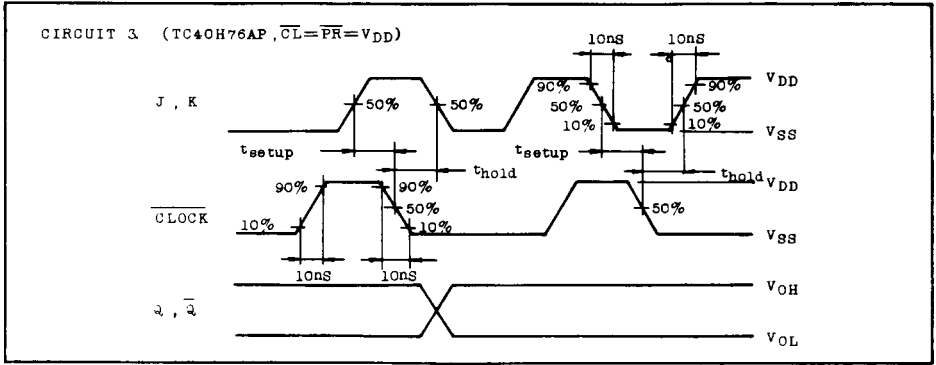
SWITCHING TIME TEST WAVEFORM

CIRCUIT 1. ($J=K=V_{DD}$, $\overline{CL}=V_{DD}$ or $\overline{PR}=V_{DD}$)CIRCUIT 2. (TC40H076, $\overline{CL}=\overline{PR}=V_{DD}$)

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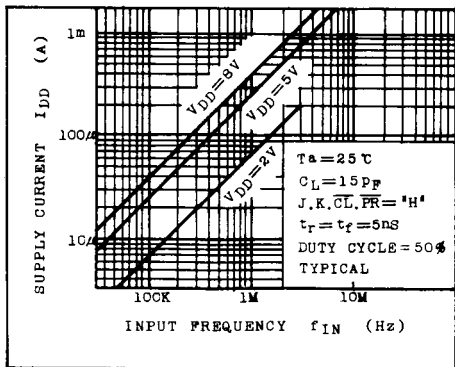
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SWITCHING TIME TEST WAVEFORM

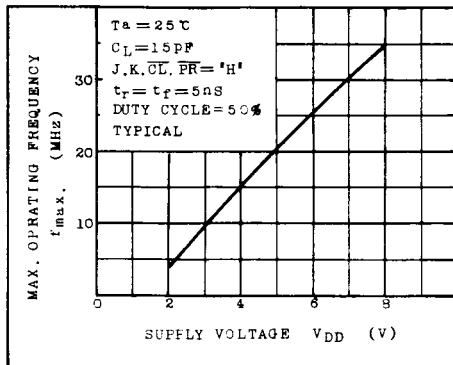


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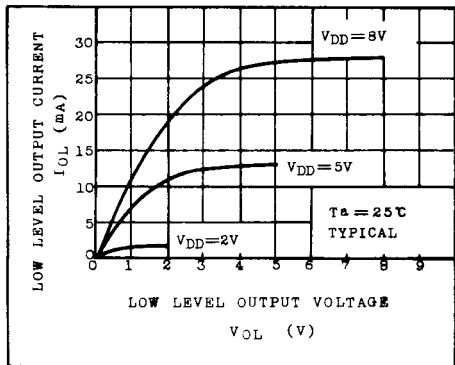
$I_{DD} - f_{IN}$



$f_{MAX\phi} - V_{DD}$



$I_{OL} - V_{OL}$



$I_{OH} - (V_{DD} - V_{OH})$

