TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

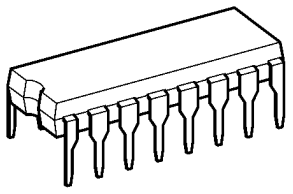
TC4521BP

TC4521BP 24-Stage Frequency Divider

TC4521BP is frequency divider consisting of 24 stages of flip-flop. The input section is equipped with an inverter to enable to use either RC oscillator circuit or crystal oscillator circuit and to accept pulse from external clock source.

Each flip-flop is inverted by the falling edge of the output of previous stage flip-flop and this can count up to the maximum of $2^{24} = 16{,}777{,}216$.

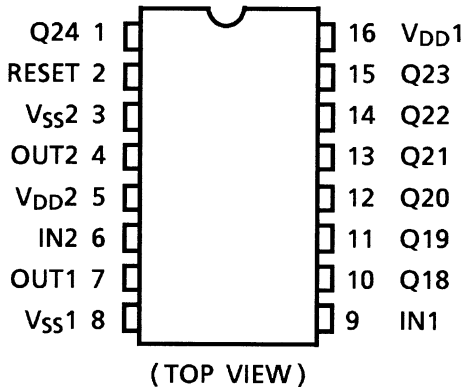
Since six outputs, 2^{18}, 2^{19}, 2^{20}, 2^{21}, 2^{22}, and 2^{23} are available besides of 2^{24}, adjustment of frequency divided output can be achieved.



DIP16-P-300-2.54A

Weight: 1.00 g (typ.)

Pin Assignment

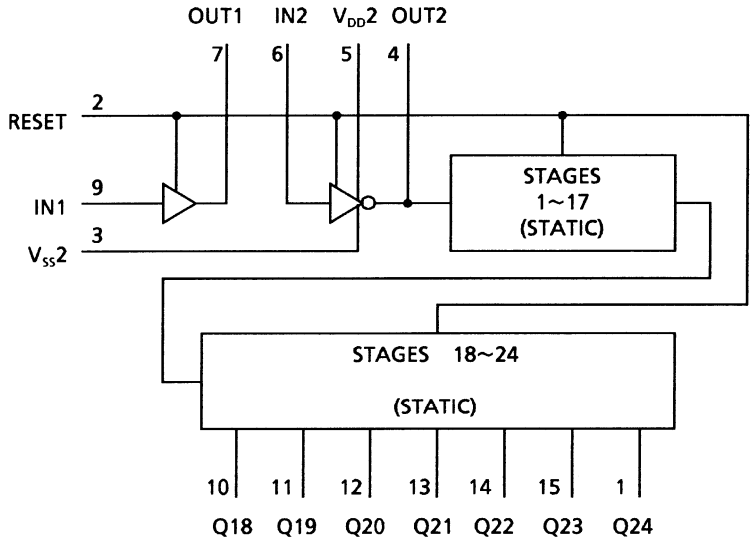


Count Capacity

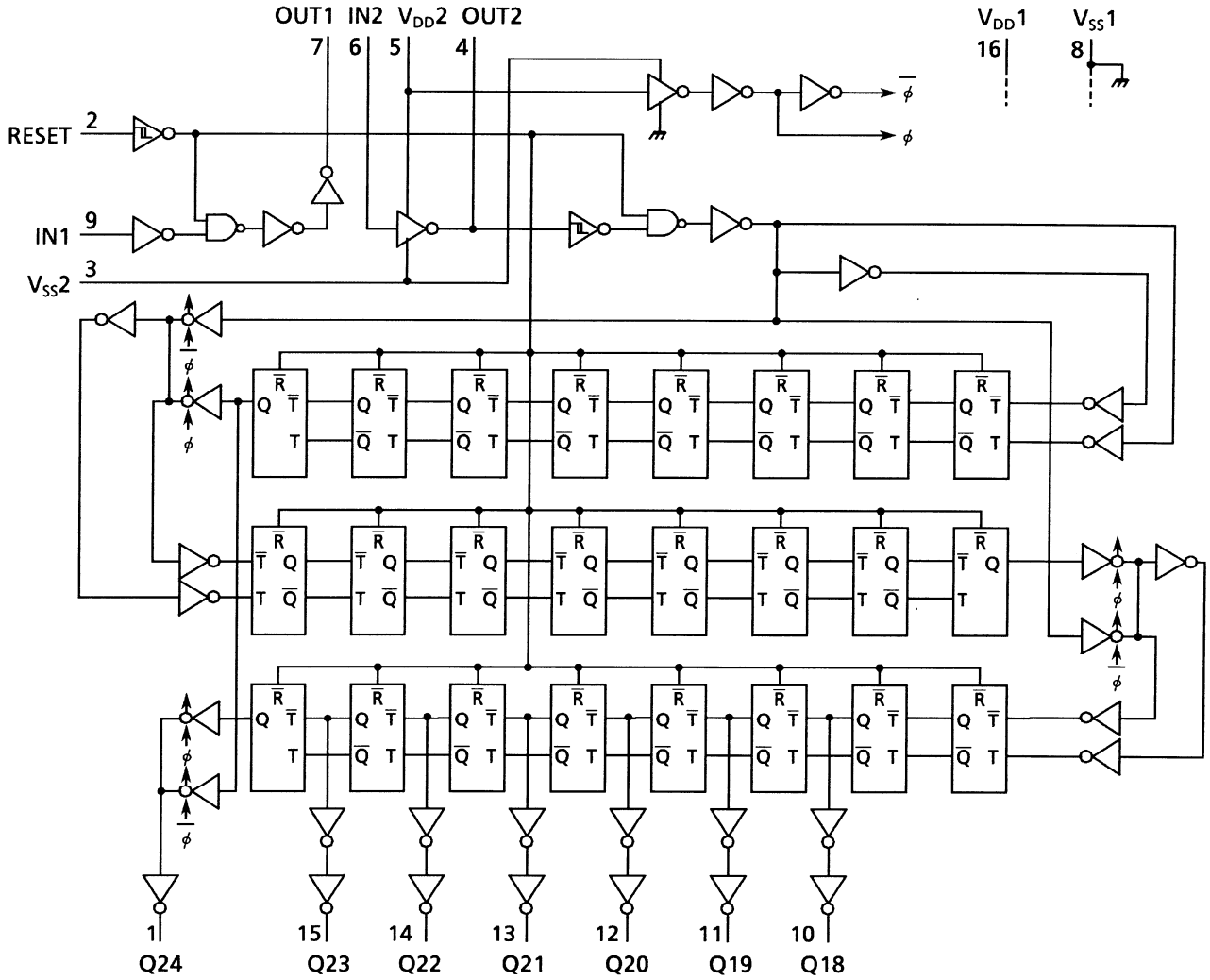
Output	Count Capacity
Q18	$2^{18} = 262{,}144$
Q19	$2^{19} = 524{,}288$
Q20	$2^{20} = 1{,}048{,}576$
Q21	$2^{21} = 2{,}097{,}152$
Q22	$2^{22} = 4{,}194{,}304$
Q23	$2^{23} = 8{,}388{,}608$
Q24	$2^{24} = 16{,}777{,}216$

Start of commercial production
1978-04

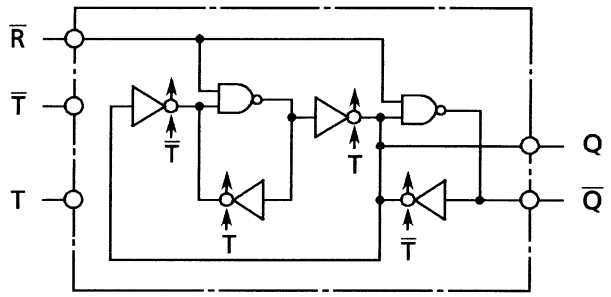
Block Diagram



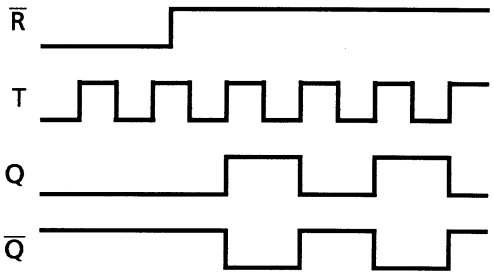
Logic Diagram



Internal Flip Flop Logic Diagram



Flip Flop Timing Chart



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	$V_{DD}1$	$V_{SS}1 - 0.5$ to $V_{SS}1 + 20$	V
	$V_{DD}2$	$V_{SS}1 - 0.5$ to $V_{DD}1 + 0.5$	
Input voltage	V_{IN}	$V_{SS}1 - 0.5$ to $V_{DD}1 + 0.5$	V
Output voltage	V_{OUT}	$V_{SS}1 - 0.5$ to $V_{DD}1 + 0.5$	V
DC input current	I_{IN}	±10	mA
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges ($V_{SS}1 = V_{SS}2 = 0$ V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	$V_{DD}1$, $V_{DD}2$	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	$V_{DD}1$	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{DD} or V_{SS}.

Static Electrical Characteristics ($V_{SS}1 = V_{SS}2 = 0$ V, $V_{DD}1 = V_{DD}2$)

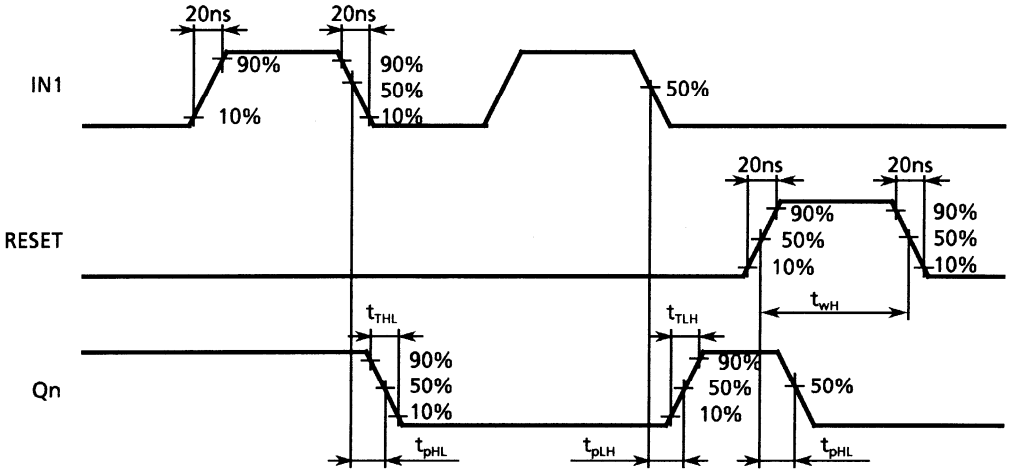
Characteristics		Sym-bol	Test Condition		−40°C		25°C			85°C		Unit
				V_{DD} (V)	Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage		V_{OH}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
				10	9.95	—	9.95	10.00	—	9.95	—	
				15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage		V_{OL}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
				10	—	0.05	—	0.00	0.05	—	0.05	
				15	—	0.05	—	0.00	0.05	—	0.05	
Output high current		I_{OH}	$V_{OH} = 4.6$ V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
			$V_{OH} = 2.5$ V	5	−2.5	—	−2.1	−4.0	—	−1.7	—	
			$V_{OH} = 9.5$ V	10	−1.5	—	−1.3	−2.2	—	−1.1	—	
			$V_{OH} = 13.5$ V	15	−4.0	—	−3.4	−9.0	—	−2.8	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Output low current		I_{OL}	$V_{OL} = 0.4$ V	5	0.61	—	0.51	1.2	—	0.42	—	mA
			$V_{OL} = 0.5$ V	10	1.5	—	1.3	3.2	—	1.1	—	
			$V_{OL} = 1.5$ V	15	4.0	—	3.4	12.0	—	2.8	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage		V_{IH}	$V_{OUT} = 0.5$ V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
			$V_{OUT} = 1.0$ V, 9.0 V	10	7.0	—	7.0	5.5	—	7.0	—	
			$V_{OUT} = 1.5$ V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
			$\|I_{OUT}\| < 1$ μA									
Input low voltage		V_{IL}	$V_{OUT} = 0.5$ V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
			$V_{OUT} = 1.0$ V, 9.0 V	10	—	3.0	—	4.5	3.0	—	3.0	
			$V_{OUT} = 1.5$ V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
			$\|I_{OUT}\| < 1$ μA									
Input current	"H" level	I_{IH}	$V_{IH} = 18$ V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" level	I_{IL}	$V_{IL} = 0$ V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent supply current		I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	5	—	0.005	5	—	150	μA
				10	—	10	—	0.010	10	—	300	
				15	—	20	—	0.015	20	—	600	

Note: All valid input combinations.

Dynamic Electrical Characteristics
(Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0$ V, $V_{DD}1 = V_{DD}2$, $C_L = 50$ pF)

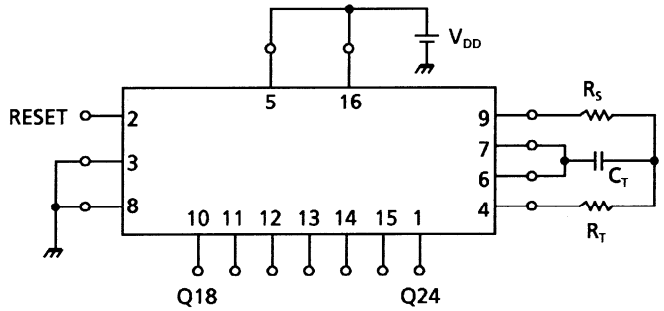
Characteristics	Symbol	Test Condition	V_{DD} (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t_{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output transition time (high to low)	t_{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time (IN2-Q18)	t_{pLH} t_{pHL}	—	5	—	1.1	9.0	μs
			10	—	0.5	3.5	
			15	—	0.3	2.7	
Propagation delay time (IN2-Q24)	t_{pLH} t_{pHL}	—	5	—	1.4	12	μs
			10	—	0.6	4.5	
			15	—	0.4	3.5	
Propagation delay time (RESET-Qn)	t_{pHL}	—	5	—	220	2600	ns
			10	—	100	1000	
			15	—	70	750	
Max clock frequency	f_{CL}	—	5	3	9.5	—	MHz
			10	6	17.5	—	
			15	8	23.5	—	
Max clock input rise time Max clock input fall time	t_{rCL} t_{fCL}	—	5	No limit			μs
			10				
			15				
Min clock pulse width	t_W	—	5	—	55	385	ns
			10	—	25	150	
			15	—	16	120	
Min pulse width (RESET)	t_{WH}	—	5	—	60	385	ns
			10	—	26	150	
			15	—	20	120	
Input capacitance	C_{IN}	—		—	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics



Application Circuit

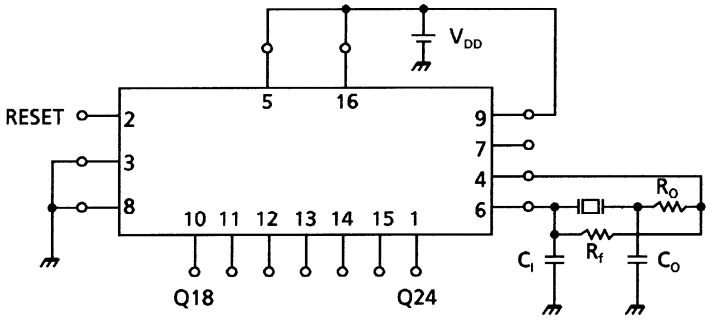
When CR Oscillation is Used as Time Reference



$$R_S \geqq 2R_T$$

$$f_{OSC} \simeq \frac{1}{2.2R_T\ C_T}$$

When Crystal Oscillation is Used as the Time Reference



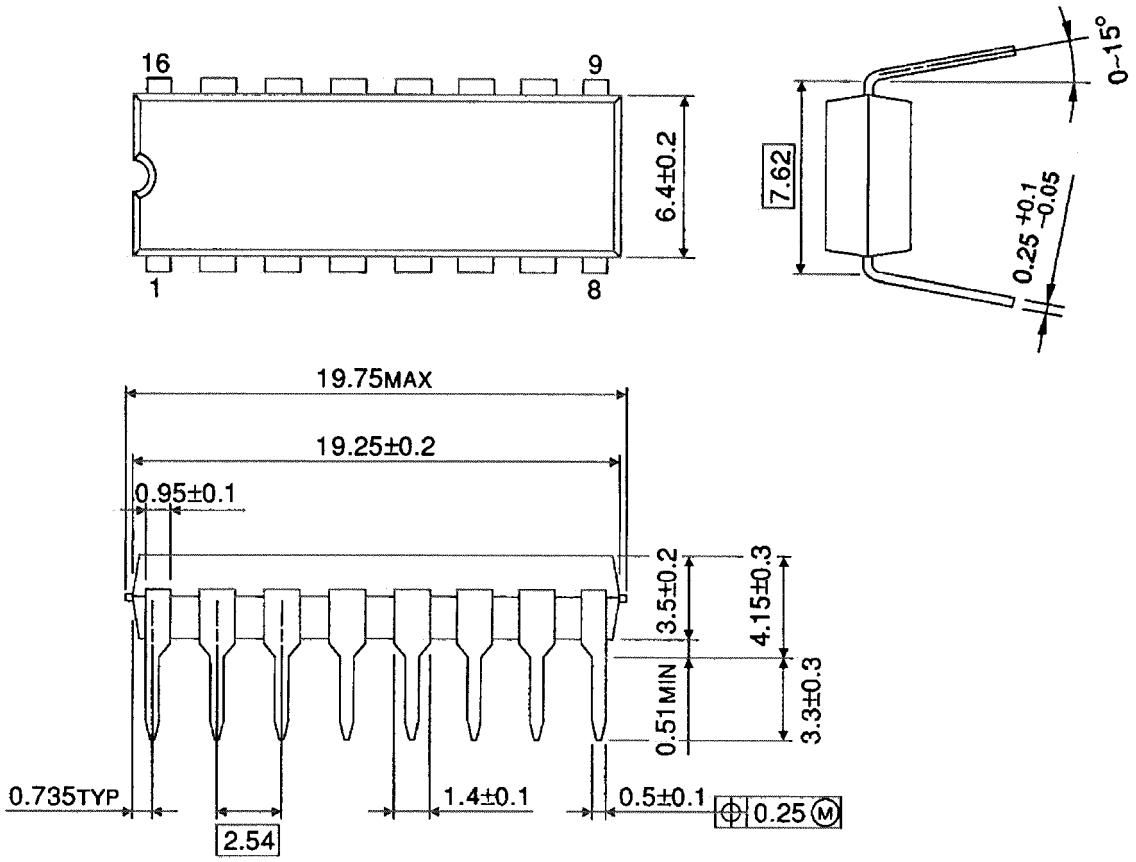
Typical Data

X'tal (Hz)	C_I, C_O (pF)	R_O (Ω)
32.768 k	23	500 k
100 k	60	100 k
1 M	45 to 50	100
4.194304 M	12 to 15	0

R_f = 10 MΩ

Package Dimensions

DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

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