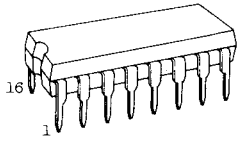
TC5036AP, TC5048AP

TC5036AP TC5048AP 17-STAGE HIGH SPEED FREQUENCY DIVIDER

TC5036AP and TC5048AP are 17-stage ripple carry binary counters equipped with inverters for crystal oscillators.
If ϕ input is opened (ϕ="L"), the inverted output of 9th stage appears on FC terminal. If ϕ input is set to "H", 9 stages from 9th stage through 17th stage can be also independently used having FC terminal as the clock input.
Outputs can be derived arbitrarily from stages 4, 12, 13, 14, 15, 16 and 17 of TC5036AP and stages 4, 5, 6, 7, 14, 16 and 17 of TC5048AP.
Both devicies are improved to have 50% duty Q4 output as same as others by changing the divider stage of TC5036P and TC5048P to static type counter.



DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

CHRACTERISTIC		SYMBOL	RATING	UNIT
DC Supply Voltage		V_{DD1}	$V_{SS1}-0.5 \sim V_{SS1}+10$	V
		V_{DD2}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	
Input Voltage	XT	V_{IN}	$V_{SS1}-0.5 \sim V_{DD2}+0.5$	V
	ϕ, FC	V_{IN}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	
Output Voltage		V_{OUT}	$V_{SS1}-0.5 \sim V_{DD1}+0.5$	V
DC Input Current		I_{IN}	±10	mA
Power Dissipation		P_D	300	mW
Storage Temperature Range		T_{stg}	-65 ~ 150	°C
Lead Temp./Time		T_{sol}	260°C · 10 sec	

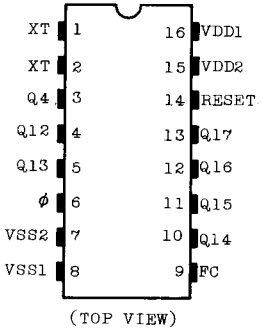
TRUTH TABLE

INPUTS				FUNCTION (See Timing Chart)
RESET	XT	ϕ	FC	
H	⎍	OPEN	H	$f_{Q4}=f_{XT}/2^4$
		H	*	Q5 ~ Q17="L" LEVEL
L	⎍	OPEN	$\overline{Q9}$	$f_{Qn}=f_{XT}/2^n$ n; 5 ~ 17
L	⎍	H	⎍	$f_{Qn}=f_{XT}/2^n$ n; 5 ~ 7 $f_{Qm}=f_{FC}/2^{(m-8)}$ m; 12 ~ 17

* Don't Care

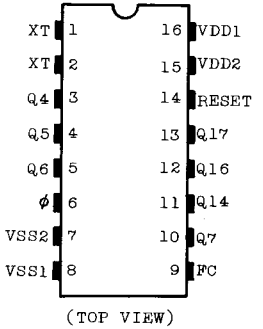
PIN ASSIGNMENT

TC5036AP



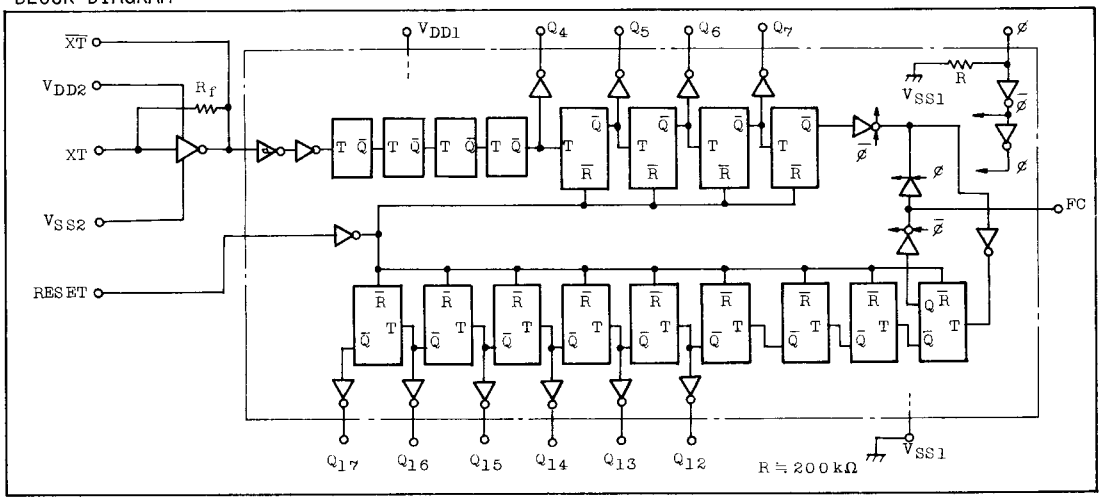
(TOP VIEW)

TC5048AP

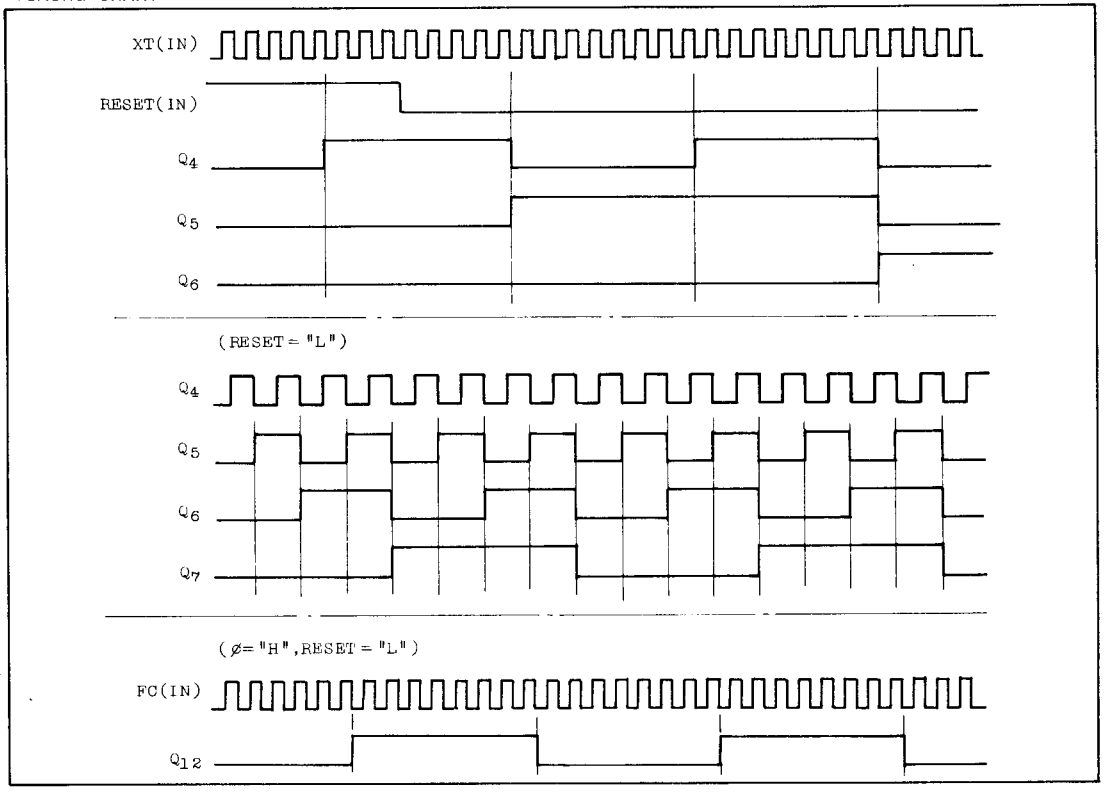


(TOP VIEW)

BLOCK DIAGRAM



TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS1}=V_{SS2}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}		3	-	8	V
	V_{DD2}		3	-	V_{DD1}	
Input Voltage	V_{IN}	Except XT	0	-	V_{DD1}	
Operating Temp.	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS1}=V_{SS2}=0V, V_{DD1}=V_{DD2})

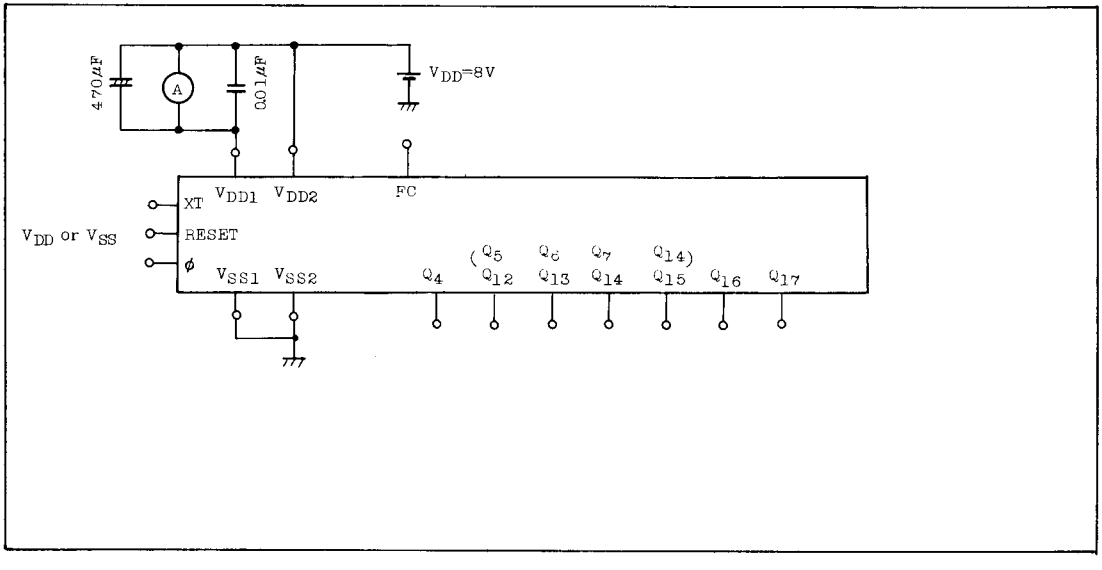
CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}, V_{SS}	5	4.95	-	4.95	5.00	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}, V_{SS}	5	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	Q Output	I_{OH}	V_{OH}=4.6V, V_{IN}=V_{DD}, V_{SS}	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
	FC, $\overline{XT}$		V_{OH}=4.6V, V_{IN}=V_{DD}, V_{SS}	5	0.025	-	-0.02	-0.06	-	-0.015	-	
Low Level Output Current	Q OUTPUT	I_{OL}	V_{OL}=0.4V, V_{IN}=V_{DD}, V_{SS}	5	0.61	-	0.51	1.5	-	0.42	-	
	FC, $\overline{XT}$		V_{OL}=0.4V, V_{IN}=V_{DD}, V_{SS}	5	0.10	-	0.08	0.25	-	0.06	-	
High Level Input Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	5	3.5	-	3.5	2.75	-	3.5	-	V
Low Level Input Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	5	-	1.5	-	2.25	1.5	-	1.5	
High Level Input Current (except XT, φ)		I_{IH}	V_{IH}=8V	8	-	0.2	-	10^{-5}	0.2	-	1.0	μA
Low Level Input Current (except XT, φ)		I_{IL}	V_{IL}=0V	8	-	-0.2	-	-10^{-5}	-0.2	-	-1.0	
Quiescent Device Current		I_{DD1}	V_{IN}=V_{DD}, V_{SS} *	8	-	5	-	0.005	5	-	150	

* All valid input combinations.

SWITCHING CHARACTERISTICS ($V_{DD1}=V_{DD2}$, $V_{SS1}=V_{SS2}=0V$, Ta=25°C, C_L=50pF)

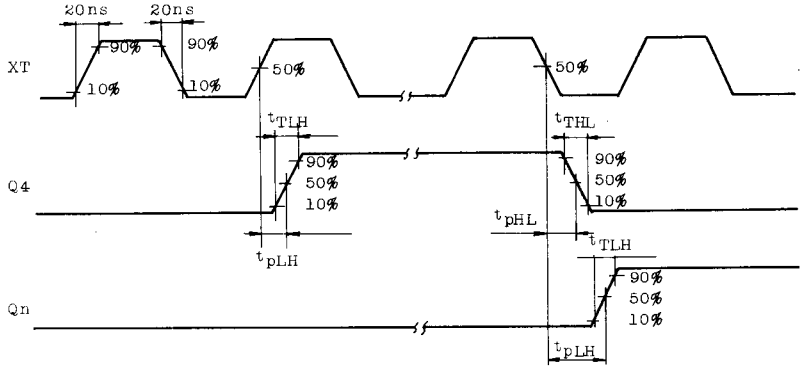
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time (Q OUTPUT)	t_{TLH}		5	-	70	200	ns
Output Fall Time (Q OUTPUT)	t_{THL}						
Input Amp Vias Resistance	R_f		8	0.6	1.6	3.0	MΩ
Propagation Delay Time (XT-Q4)	t_{pLH}, t_{pHL}		5	-	200	400	ns
Propagation Delay Time (XT-Q17)	t_{pLH}, t_{pHL}		5	-	0.78	1.6	μs
Propagation Delay Time (FC-Q12)	t_{pLH}, t_{pHL}		5	-	240	480	ns
Propagation Delay Time (FC-Q17)	t_{pLH}, t_{pHL}		5	-	420	900	ns
Propagation Delay Time (RESET-Q)	t_{pHL}(RESET)		5	-	100	200	ns
Min. Pulse Width	t_w(RESET)		5	-	35	70	ns
Max. Clock Frequency	f_{CL}(XT)		5	10	20	-	MHz
Max. Clock Frequency	f_{CL}(FC)		5	8	16	-	
Max. Clock Rise Time	t_{rCL}	(XT)	5	No Limit			μs
Max. Clock Fall Time	t_{fCL}						
Max. Clock Rise Time	t_{rCL}	(FC)	5	20	-	-	
Max. Clock Fall Time	t_{fCL}						
Input Capacitance	C_{IN}	except FC		-	5	7.5	pF

I_{DD1} TEST CIRCUIT

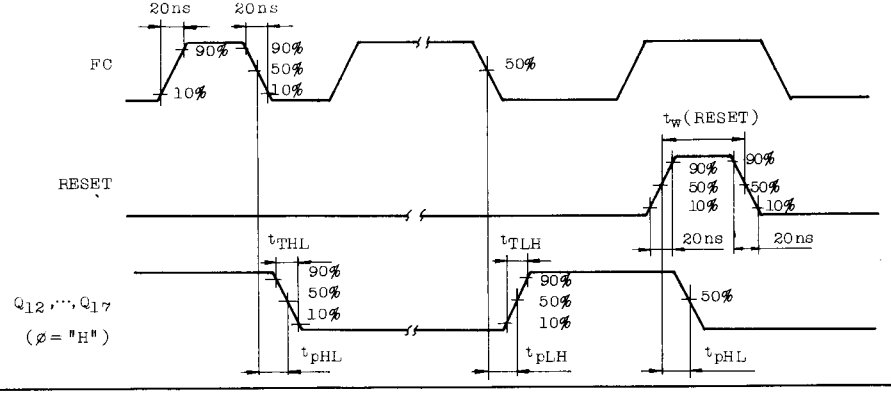


SWITCHING TIME TEST WAVEFORMS

1. f_{CL}(XT), t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}



2. f_{CL}(FC), t_w(RESET), t_{pHL}(RESET)



TYPICAL APPLICATION