

TC5093AP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5093AP 8 BIT ANALOG TO DIGITAL CONVERTER

GENERAL DESCRIPTION

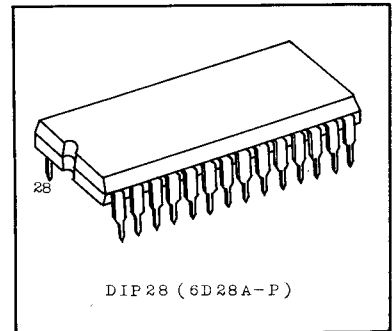
The TC5093AP is a monolithic CMOS 8 bit successive approximation A/D converter with 8 channel multiplex inputs. After an analog input channel is selected with channel select input (CH0 ~2) and channel latch input (CHL), when STC is set high EOC goes low at the leading edge of STC and the conversion starts.

After the conversion is completed, EOC returns high and the new data replace the previous data at DB0 ~DB7.

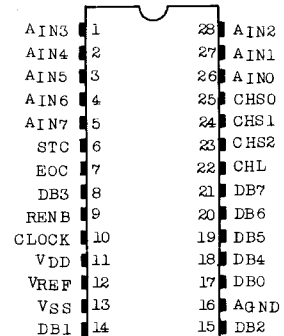
The TC5093AP has features of high speed, high accuracy and very low power consumption which make the device well suited to a broad application field such as process and machine control and automotive equipment.

FEATURES

- High accuracy $\pm \frac{1}{2}$ LSB TYP
- High speed conversion 100 μ sec TYP @ $f_{cp}=640$ kHz
- Single power supply 5V \pm 10%
- Low power consumption 9mW MAX @ $T_a=25^\circ$ C
- 8 channel analog multiplex input
- Easy interface to all microprocessors
- Zero or full scale adjustment free
- Latched 3-state output



PIN ASSIGNMENT

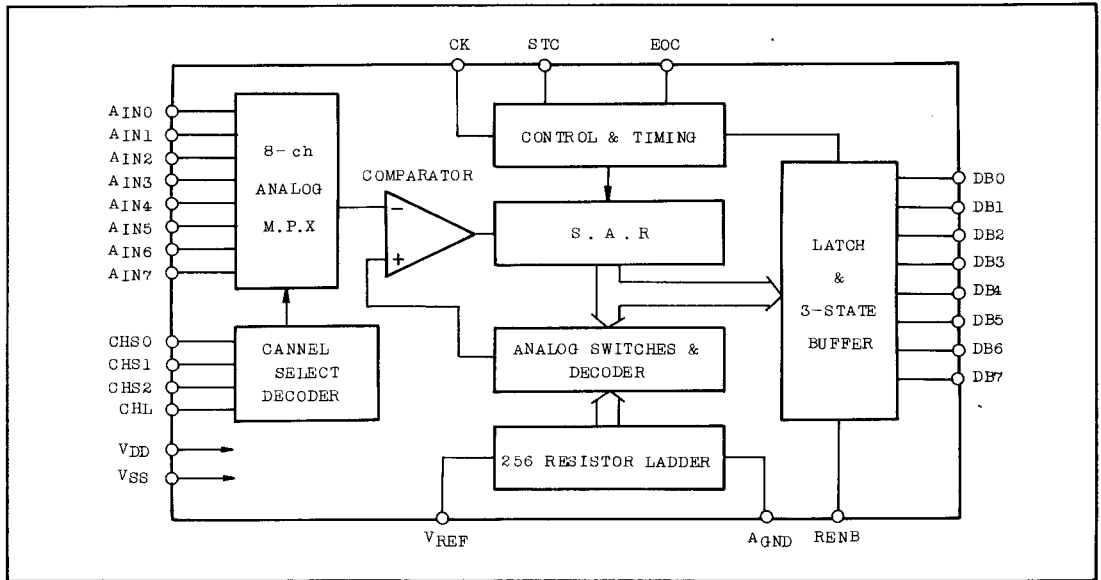


(TOP VIEW)

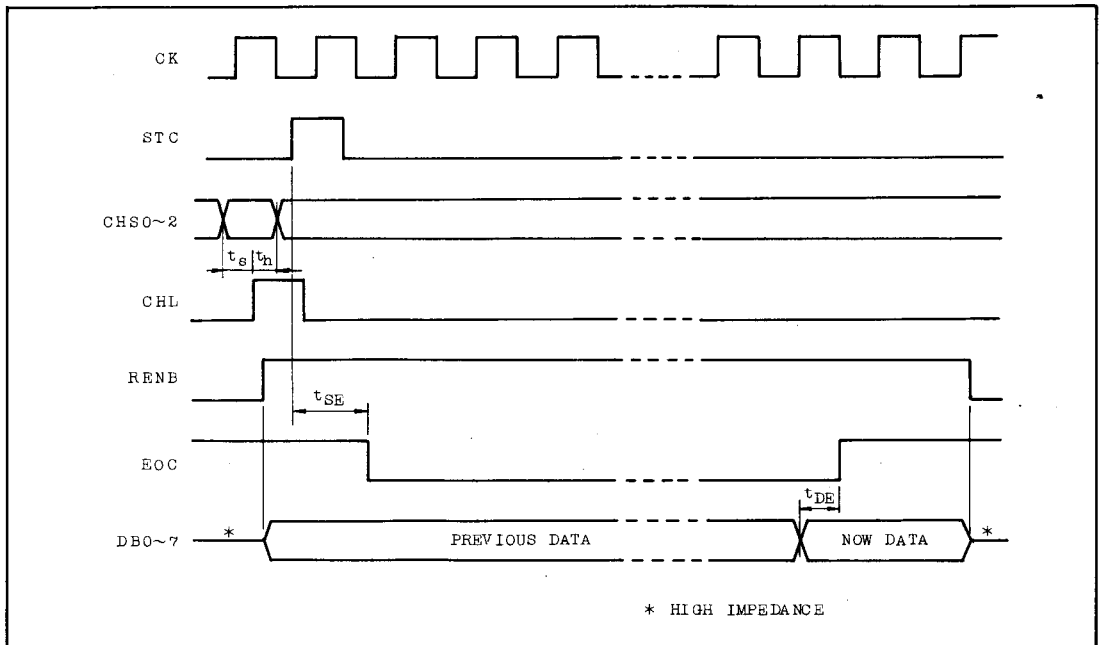
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	VDD	$V_{SS}-0.5 \sim V_{SS} + 7$	V
DC Input Voltage	VIN	$V_{SS}-0.5 \sim V_{DD} + 0.5$	V
DC Output Voltage	VOU	$V_{SS}-0.5 \sim V_{DD} + 0.5$	V
Reference Voltage	VREF	$V_{SS}-0.5 \sim V_{DD} + 0.5$	V
Analog Ground Voltage	AGND	$V_{SS}-0.5 \sim V_{DD} + 0.5$	V
DC Input Current	IIN	± 10	mA
Power Dissipation	PD	300	mW
Storage Temperature	TSTG	-65 ~ 150	°C
Lead Temperature 10 sec.	TL	300	°C

BLOCK DIAGRAM



TIMING CHART



TC5093AP

PIN & FUNCTION

PIN NO.	SYMBOL	PIN NAME & FUNCTION	PIN NO.	SYMBOL	PIN NAME & FUNCTION																																				
1	A _{IN3}	[ANALOG INPUT] The analog input voltage applied to the selected channel is converted. Full range of input signal is to be from A _{GND} to V _{REF} .	15	DB2	3-STATE PARALLEL DATA OUTPUT																																				
2	A _{IN4}		16	A _{GND}	[ANALOG GROUND] A _{GND} defines the zero level of A _{IN} .																																				
3	A _{IN5}		17	DB0	3-STATE PARALLEL DATA OUTPUT DB0 : LSB DB7 : MSB																																				
4	A _{IN6}		18	DB4																																					
5	A _{IN7}		19	DB5																																					
6	STC	[START CONVERSION] Conversion starts at the falling edge of STC.	20	DB6																																					
7	EOC	[END OF CONVERSION] EOC becomes low level at the rising edge of STC. And when the conversion is completed EOC returns to high level.	21	DB7	[CHANNEL LATCH INPUT] The channel select signals CHS0 ~2 are latched at the rising edge of CHL.																																				
8	DB3	3-STATE PARALLEL DATA OUTPUT	22	CHL																																					
9	RENB	[READ ENABLE] Output enable signal "H" = DB0 ~7 enable "L" = DB0 ~7 high impedance	23	CHS2	[CHANNEL SELECT INPUT] One of A _{IN0} ~A _{IN7} is selected according to the status of CH0 ~CH2.																																				
10	CLOCK	[CLOCK INPUT] Basic system clock	24	CHS2																																					
11	V _{DD}	[SYSTEM POWER SUPPLY] V _{DD} =5V ±10%	25	CHS0	<table border="1"> <thead> <tr> <th>CHS2</th> <th>CHS1</th> <th>CHS0</th> <th>ON CHANNEL</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>A_{IN0}</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>A_{IN1}</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>A_{IN2}</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>A_{IN3}</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>A_{IN4}</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>A_{IN5}</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>A_{IN6}</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>A_{IN7}</td> </tr> </tbody> </table>	CHS2	CHS1	CHS0	ON CHANNEL	L	L	L	A _{IN0}	L	L	H	A _{IN1}	L	H	L	A _{IN2}	L	H	H	A _{IN3}	H	L	L	A _{IN4}	H	L	H	A _{IN5}	H	H	L	A _{IN6}	H	H	H	A _{IN7}
CHS2	CHS1	CHS0			ON CHANNEL																																				
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H	H	H	A _{IN7}																																						
12	V _{REF}	[REFERENCE VOLTAGE] V _{REF} defines the full scale of A _{IN} .	26	A _{IN0}	[ANALOG INPUT]																																				
13	V _{SS}	[SYSTEM GROUND] V _{SS} =0V	27	A _{IN1}																																					
14	DB1	3-STATE PARALLEL DATA OUTPUT	28	A _{IN2}																																					

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}		4.5	5.0	5.5	V
Input Voltage	V _{IN}		0	-	V _{DD}	V
Reference Voltage	V _{REF}	V _{DD} =5V, AGND=0V	3.5	V _{DD}	V _{DD}	V
Analog Ground Voltage	AGND	V _{DD} =5V, V _{REF} =5V	0.0	0.0	3.0	V
Voltage Between V _{REF} and AGND		V _{DD} =5V ± 10%	2.0	V _{DD}	V _{DD}	V
Clock Frequency	f _{cp}	V _{DD} =5V ± 10% Duty Cycle=50%	10	640	1280	kHz
Operating Temperature	T _{opr}		-40	-	+85	°C

DC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

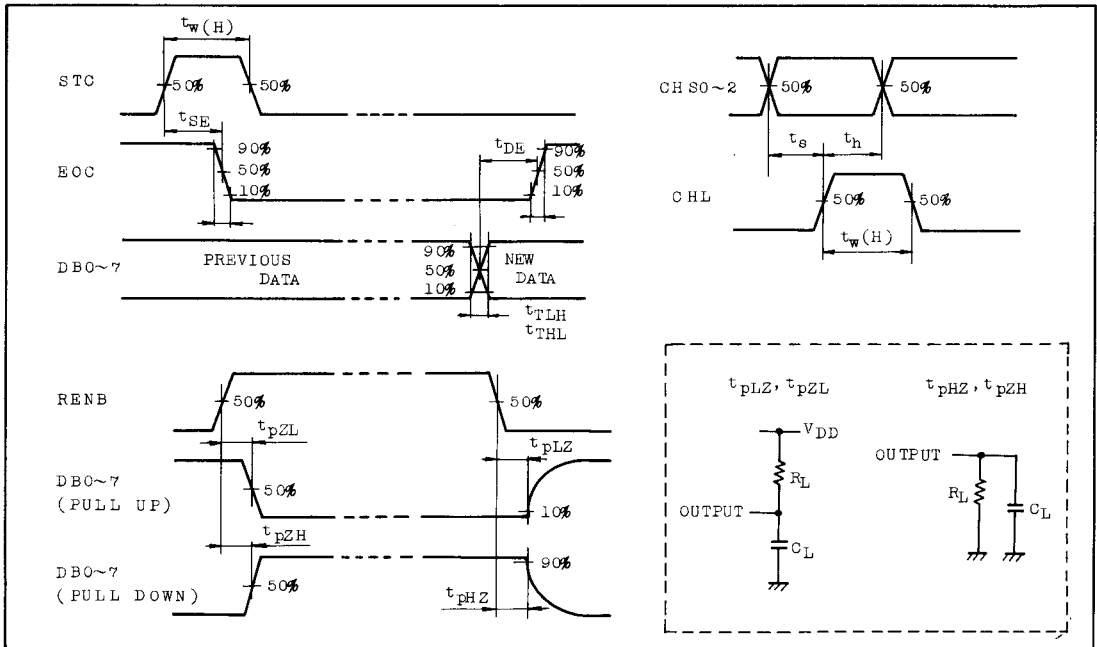
PARAMETER	SYMBOL	TEST CONDITION	-40°C		25°C			85°C		UNIT	
			V _{DD}	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.		MAX.
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5.0	4.95	-	4.95	5.00	-	4.95	-	V
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5.0	-	0.05	-	0.00	0.05	-	0.05	V
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5.0	-1.2	-	-	-	-	-0.7	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{SS} , V _{DD}	5.0	2.4	-	2.0	-	-	1.6	-	mA
High Level Input Voltage	V _{IH}	I _{OUT} < 1μA V _{OUT} =0.5V, 4.5V	5.0	3.5	-	3.5	-	-	3.5	-	V
Low Level Input Voltage	V _{IL}	I _{OUT} < 1μA V _{OUT} =0.5V, 4.5V	5.0	-	1.5	-	-	1.5	-	1.5	V
3-State Output Disable Current	I _{DH} I _{DL}	V _{OH} =5.5V or V _{OL} =0.0V	5.5	-	±0.5	-	-	±0.5	-	±1	μA
Digital Input Current	I _{IH} I _{IL}	V _{IH} =5.5V or V _{IL} =0.0V	5.5	-	±0.3	-	-	±0.3	-	±1	μA
On Channel Input Current	I _{ON}	V _{IH} =5.5V or V _{IL} =0.0V f _{cp} = kHz	5.5	-	±2	-	-	±2	-	±5	μA
OFF Channel Input Current	I _{OFF}	V _{IH} =5.5V or V _{IL} =0.0V	5.5	-	±0.2	-	-	±0.2	-	±1	μA
Operating Current	I _{DD}	f _{cp} =1 MHz	5.0	-	2.0	-	-	1.8	-	2.0	mA
Reference Resistance	R _{REF}		-	4.0	1.7	4.3	7.5	17	4.3	19	kΩ

TC5093AP

SWITCHING CHARACTERISTICS ($V_{DD}=5.0V$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	$C_L=50pF$	-	50	100	nS
Propagation Delay Time (STC - EOC)	t_{SE}	$C_L=50pF$	10	1/2 CLOCK + 200	1/2 CLOCK + 600	
Data-EOC Time	t_{DE}	$C_L=50pF$	1 CLOCK - 300	1 CLOCK - 70	1 CLOCK	
3-State Output Enable Time	t_{pZH} t_{pZL}	$C_L=50pF$ $R_L=1k$	-	85	200	
3-State Output Disable Time	t_{pHZ}		-	85	200	
	t_{pLZ}		-	65	200	
Minimum Pulse Width (STC, CHL)	$t_w(H)$	$C_L=50pF$	-	40	100	
Minimum Set-up Time (CHSO ~2)	t_s	$C_L=50pF$	-	2	50	
Minimum Hold Time (CHSO ~2)	t_h	$C_L=50pF$	-	0	50	
Input Capacitance	C_{IN1}	Digital Input	-	5	-	
Input Capacitance	C_{IN2}	Analog In(ON)	-	-	-	
Input Capacitance	C_{IN3}	Analog In(OFF)	-	-	-	
Output Capacitance	C_{OUT}	3-State Out	-	10	-	

SWITCHING CHARACTERISTICS TEST WAVEFORM



SYSTEM CHARACTERISTICS (T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E _{ZR}	V _{DD} =5.0V V _{REF} =5.000V t _{CP} =1 MHz	-	± $\frac{1}{4}$	±1	LSB
Full Scale Error	E _{FS}		-	± $\frac{1}{2}$	±1	
Nonlinearity Error	E _{LI}		-	± $\frac{1}{2}$	±1	
Conversion Time	T _C	f _{CP} =640 kHz	-	100		μs
		f _{CP} =1280 kHz	-	50		