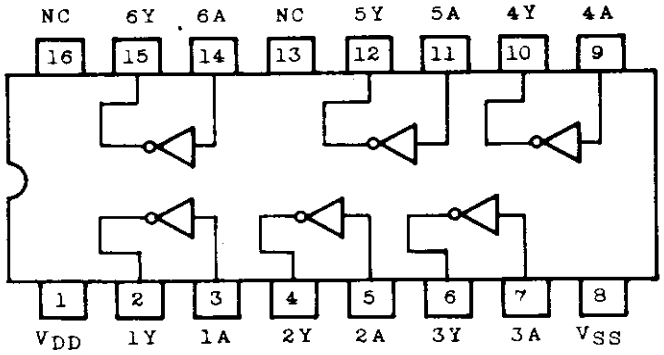
TC50H000P/F
TC50H001P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

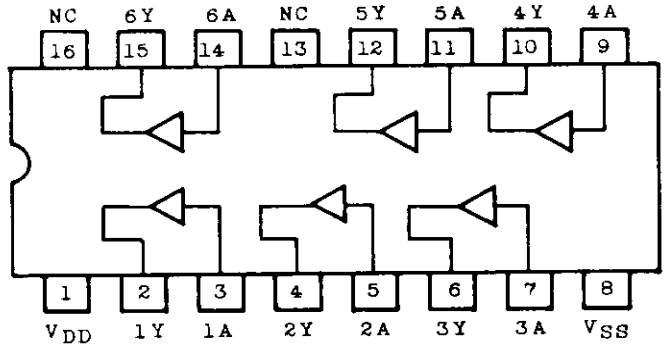
TC50H000 HEX BUFFER/CONVERTER INVERTING TYPE

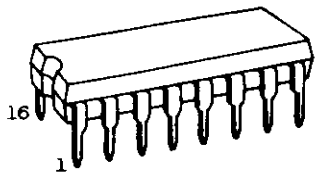
TC50H001 HEX BUFFER/CONVERTER NONINVERTING TYPE

TC50H000

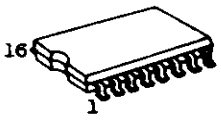


TC50H001





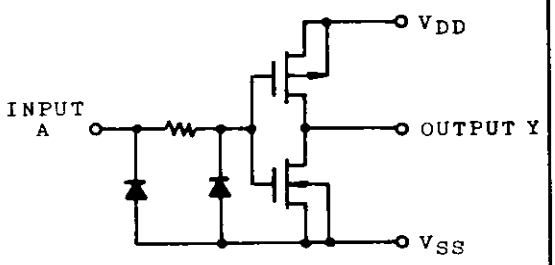
DIP16(3D16A-P)



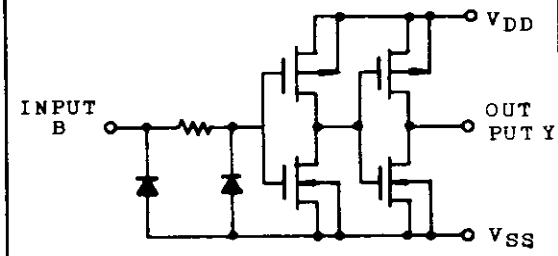
MFP16(F16GC-P)

PIN CONNECTION

TC50H000 1/6



TC50H001 1/6



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{SS}+18$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	2.0	-	8.0	V
Input Voltage	V_{IN}	—	0	-	18	V
Operating Temperature	T_{opr}	—	-40	-	85	°C

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ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-1.04	-	-0.88		-	-0.72	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	2.8	-	2.2		-	1.6	-	mA
Input Voltage	High Level	V_{IH}	$\|I_{OUT}\|<1\mu A$ V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
	Low Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current	"H"Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L"Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current		I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	5.0	-	10^{-3}	5.0	-	25	μA

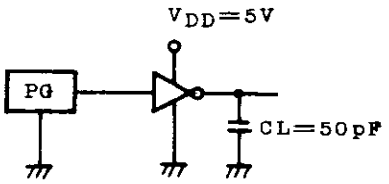
* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF)

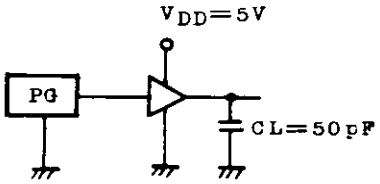
CHARACTERISTIC		SYMBOL	TEST CONDITION	TC50H000			TC50H001			UNIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Rise Time		t_{or}	Fig.1, 2	-	20	35	-	24	35	ns
Output Fall Time		t_{of}		-	13	30	-	13	30	ns
Propagation Delay Time	Low-High	t_{pLH}	Fig.1, 2	-	14	21	-	18	27	ns
	High-Low	t_{pHL}		-	12	18	-	15	23	ns
Input Capacitance		C_{IN}		-	5		-	5		pF

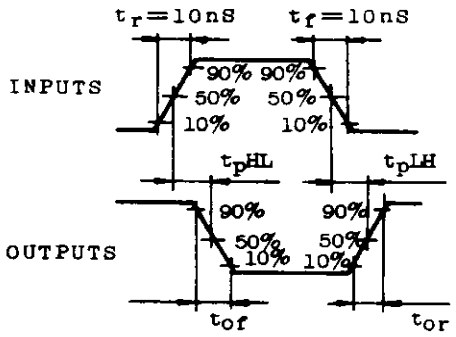
SWITCHING TIME TEST CIRCUIT AND WAVEFORM (f_{IN}=1MHz, Duty Cycle=50%)

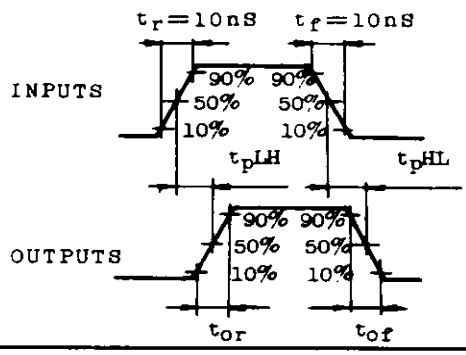
CIRCUIT 1
TC50H000



CIRCUIT 2
TC50H001

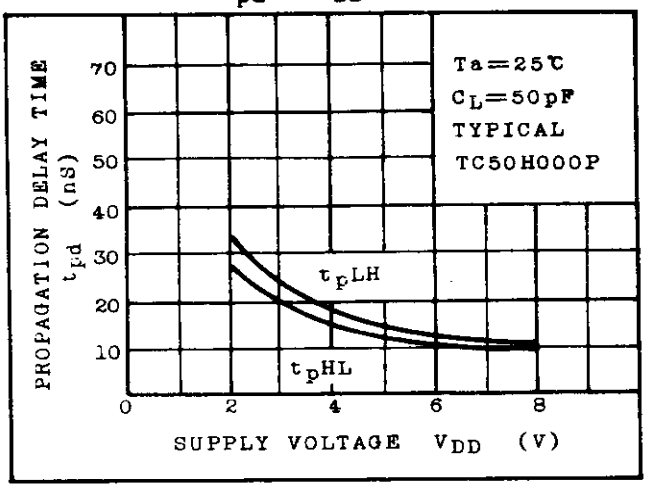




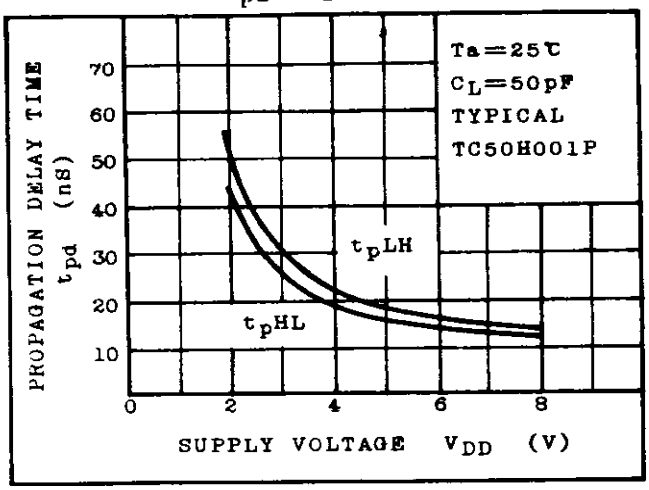


TC50H000P/F
TC50H001P/F

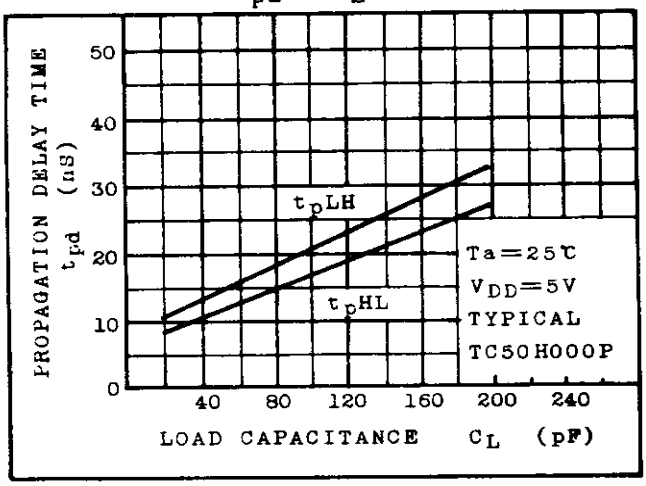
t_{pd} - V_{DD}



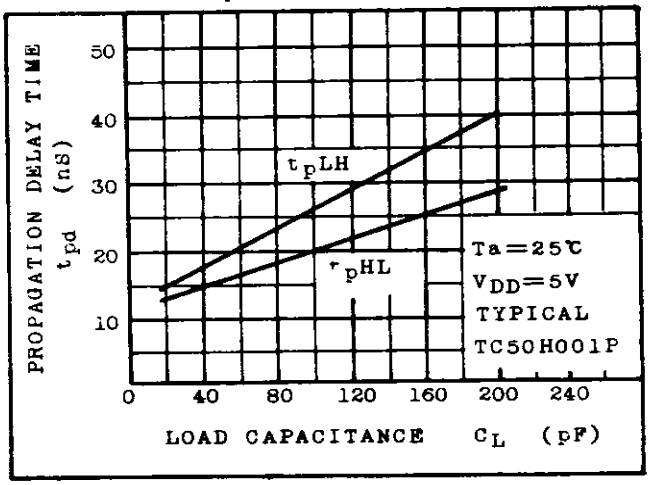
t_{pd}- V_{DD}



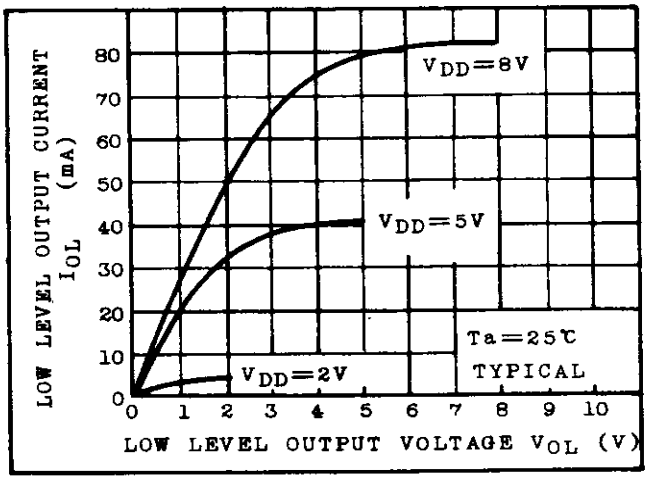
t_{pd} - C_L



t_{pd} - C_L



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})