TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

TC511001P/J/Z-85, TC511001P/J/Z-10
TC511001P/J/Z-12

DESCRIPTION

The TC511001P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001P/J/Z is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. "Test Mode" function is implemented from Revision C.

FEATURES

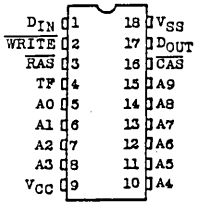
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511001P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

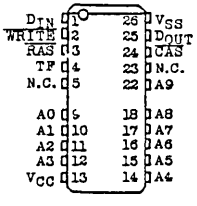
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  385mW MAX. Operating (TC511001P/J/Z-85)
  330mW MAX. Operating (TC511001P/J/Z-10)
  275mW MAX. Operating (TC511001P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511001P
  Plastic SOJ: TC511001J
  Plastic ZIP: TC511001Z

PIN CONNECTION (TOP VIEW)

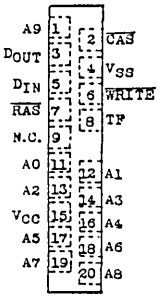
Plastic DIP



Plastic SOJ



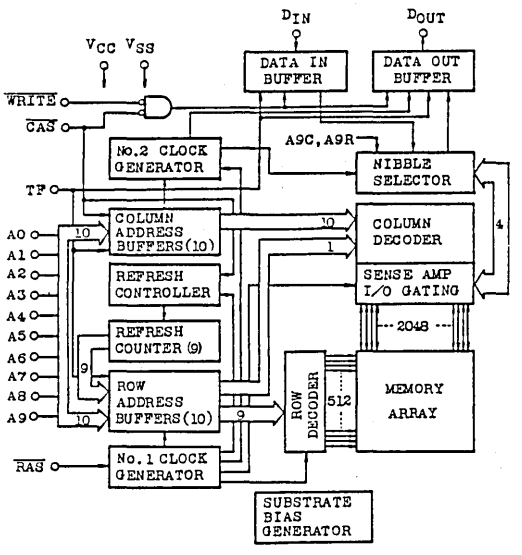
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Mode Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Temperature	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	3
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	50 40 30	mA mA mA	3,4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFERSH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	- - -	70 60 50	mA mA mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ 0.8V, All Other Pins Not Under Test = 0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)		-10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{NRMW}	Nibble Mode Read-Write Cycle Time	65	-	65	-	80	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time reference to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	-	35	-	40	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEH}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

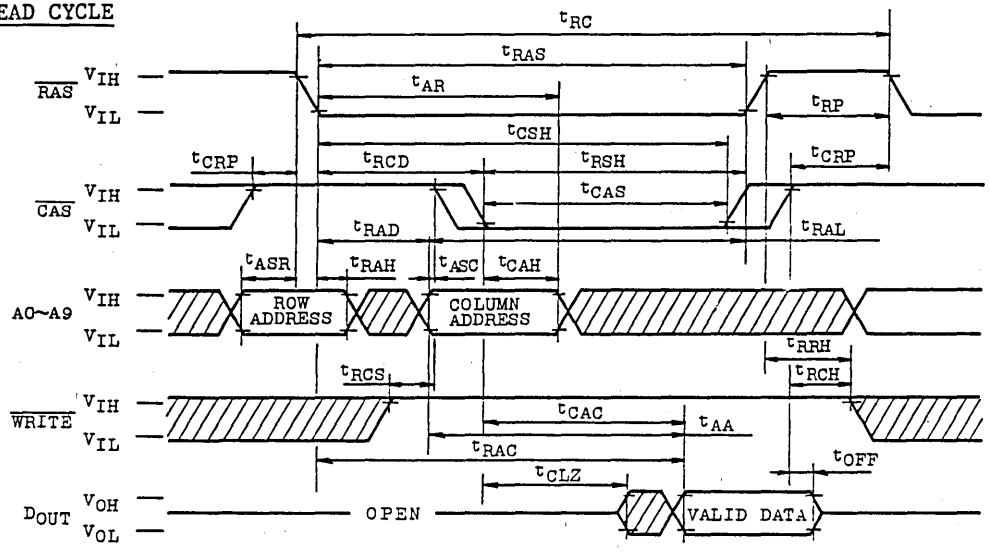
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

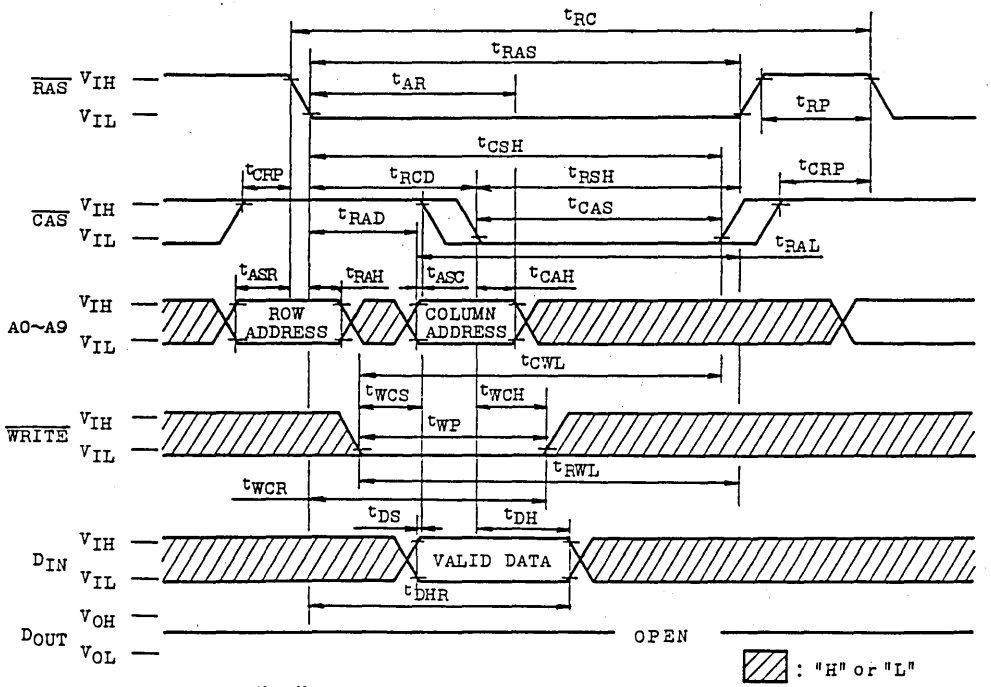
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

READ CYCLE

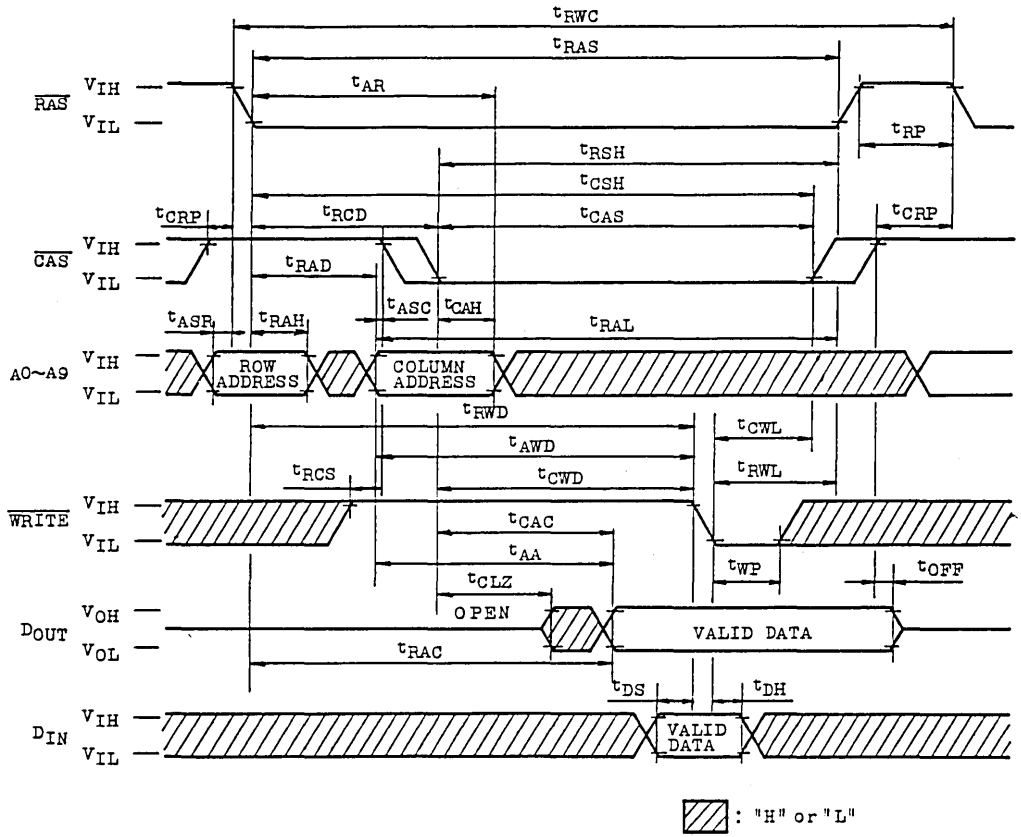


WRITE CYCLE (EARLY WRITE)



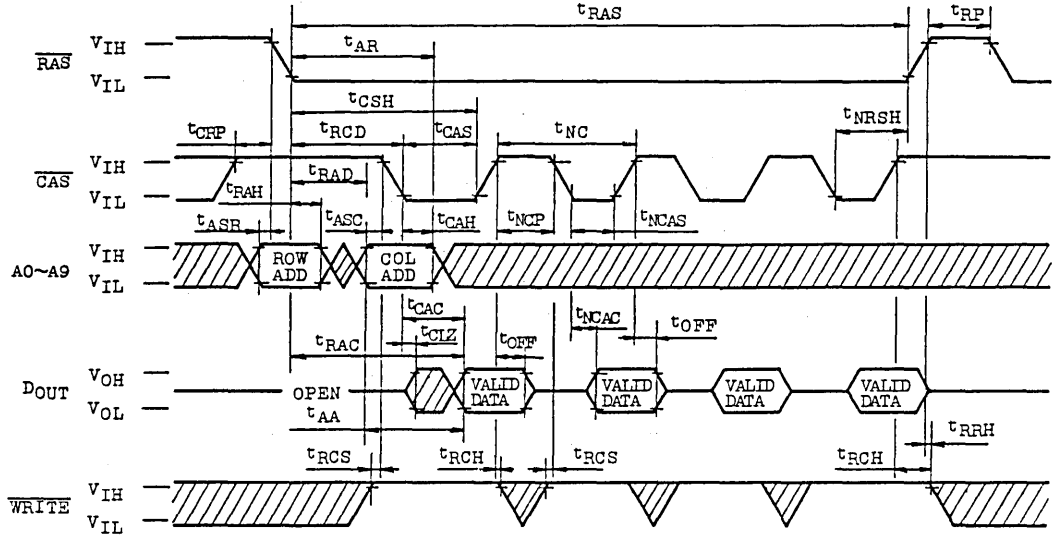
NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

READ-WRITE CYCLE

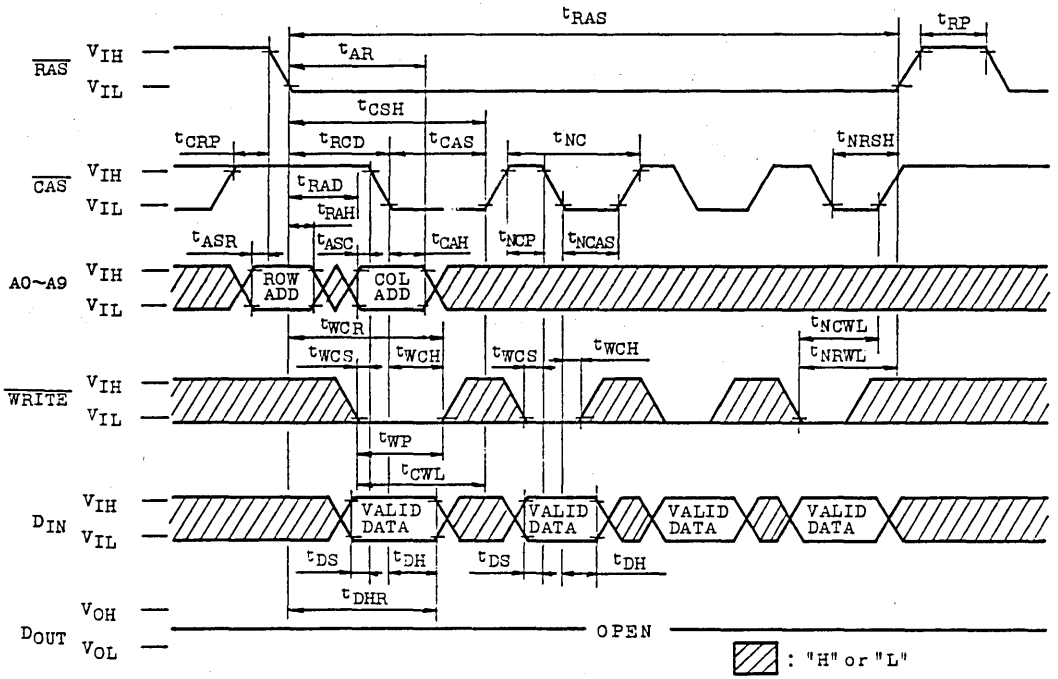


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

NIBBLE MODE READ CYCLE

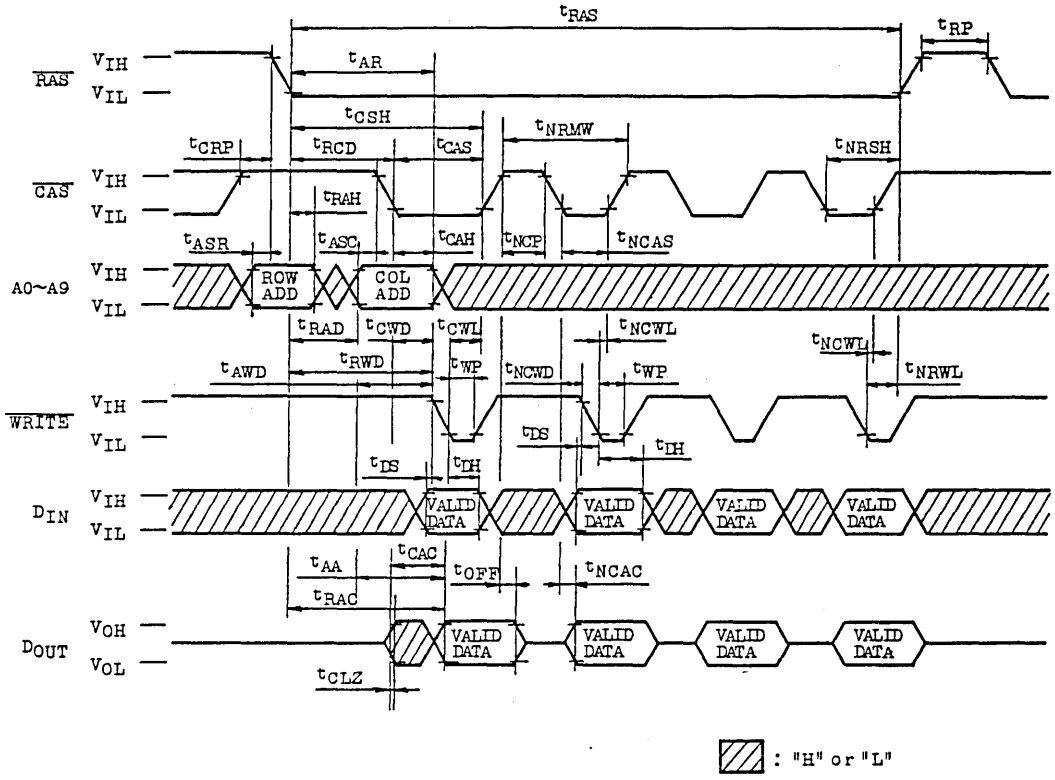


NIBBLE MODE WRITE CYCLE (EARLY WRITE)



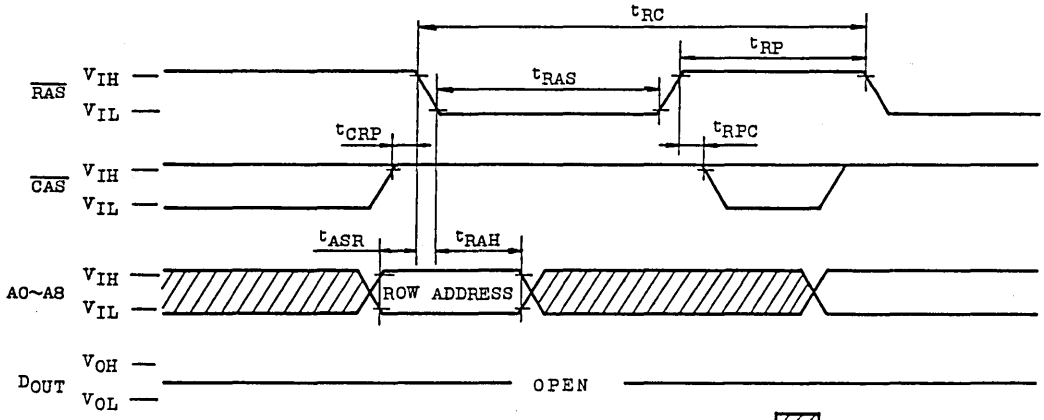
NOTE: "TF" pin should be connected to V_{IL} level or open.

NIBBLE MODE READ-WRITE CYCLE



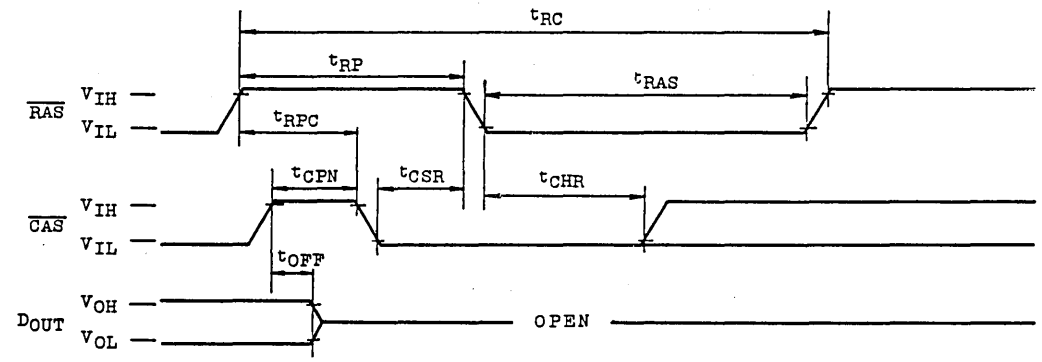
NOTE: "TF" pin should be connected to V_{IL} level or open.

$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H" or "L"

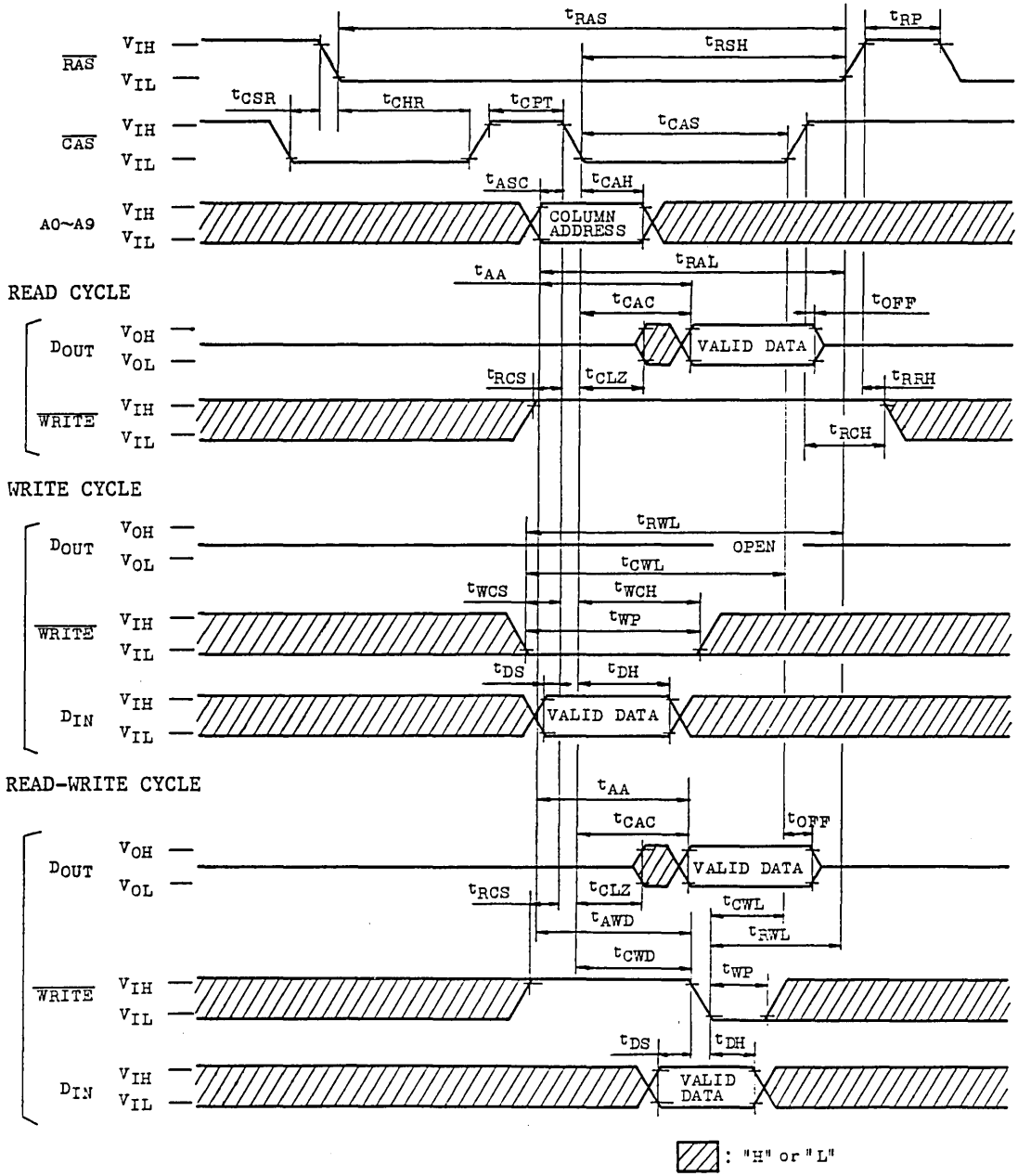
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

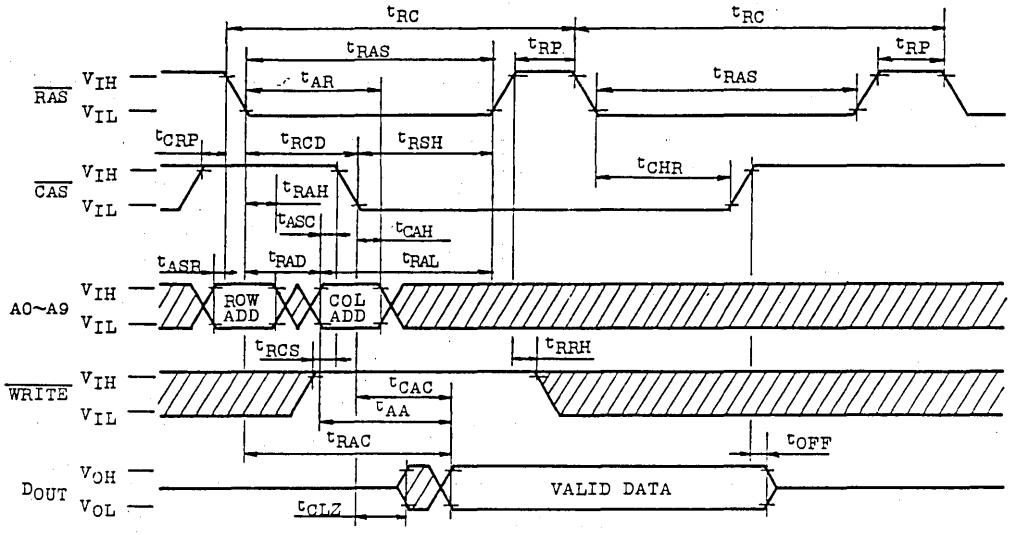
"TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

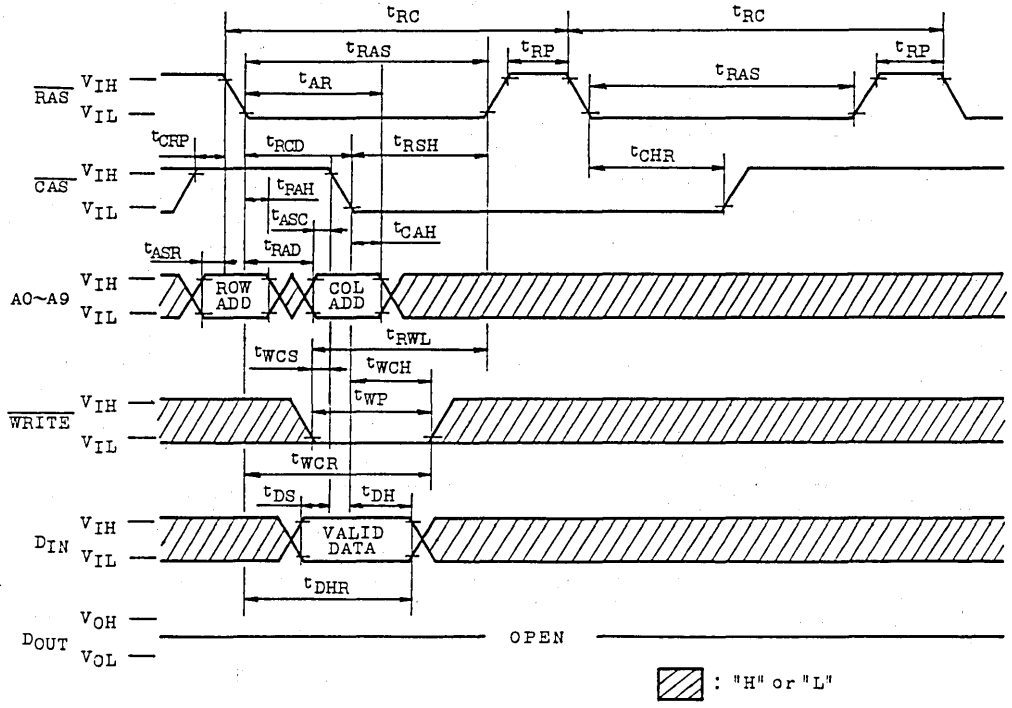


NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001P/J/Z are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In(D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low(active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made is negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

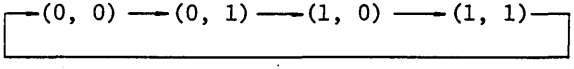
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active(low). Data read from the selected cell will be avialable at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001P/J/Z is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

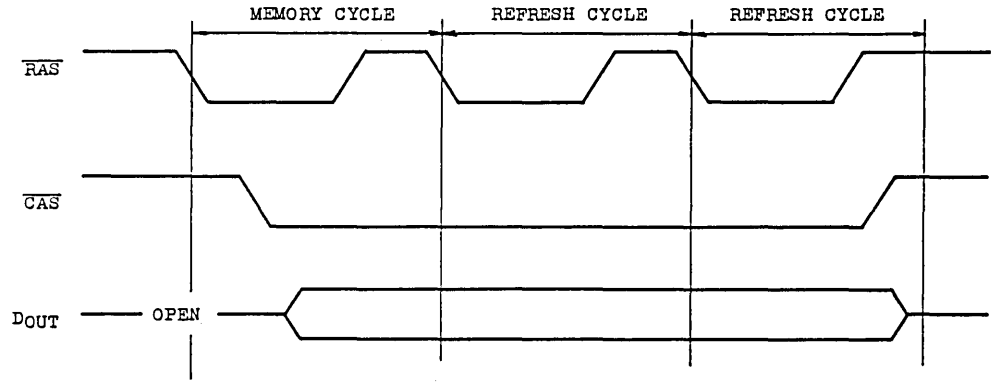
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ∿ A8) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001P/J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in perparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001P/J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001P/J/Z can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one cartain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST.
Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

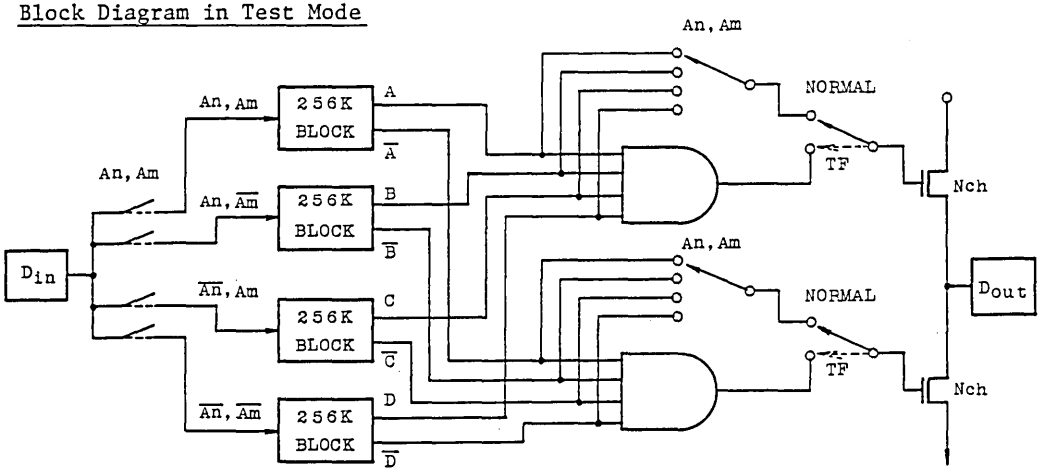
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super Voltage; Test Mode

TF Pin = Low Level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES and tTEH as shown in figure 2) It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

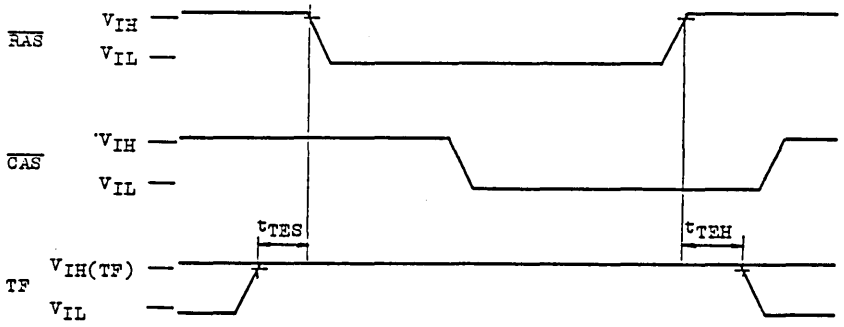
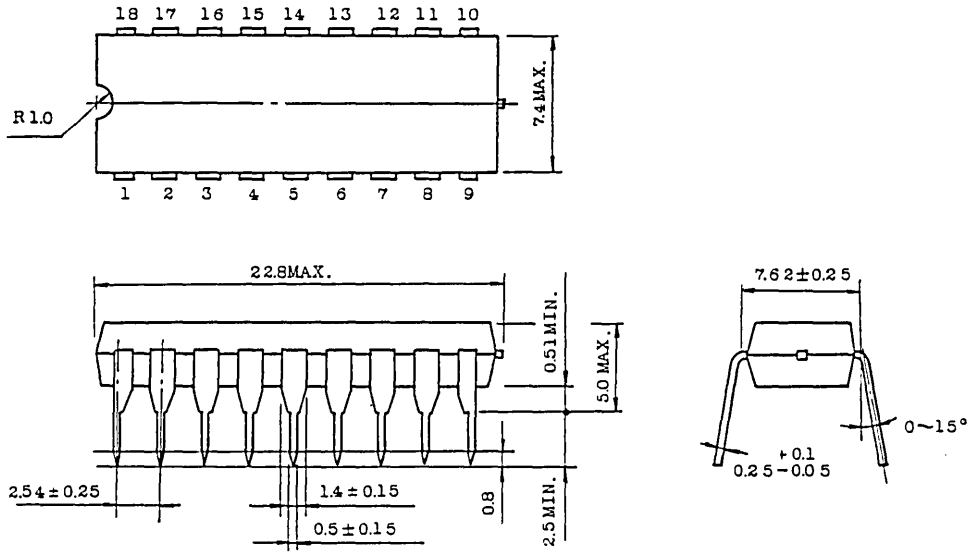


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

• Plastic DIP

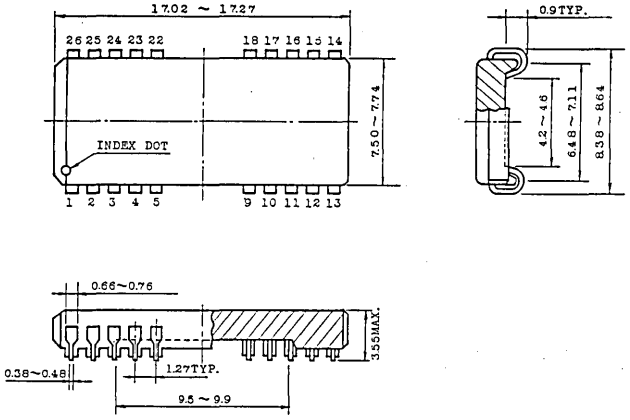
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

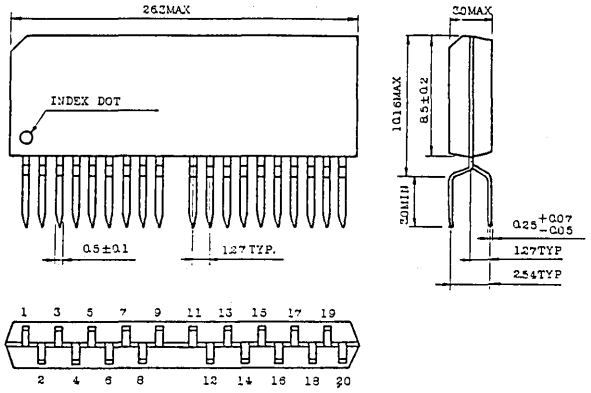
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.