PRELIMINARY

1,048,576 WORD X 16 BIT HYPER PAGE (EDO) DYNAMIC RAM

Description

The TC5118165BJ/BFT is the hyper page (EDO) dynamic RAM organized 1,048,576 words by 16 bits. The TC5118165BJ/BFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118165BJ/BFT to be packaged in a standard 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 990mW MAX. Operating
  - (TC5118165BJ/BFT-60)
  - 825mW MAX. Operating
  - (TC5118165BJ/BFT-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC5118165BJ: SOJ42-P-400
  TC5118165BFT: TSOP50-P-400

Note: For packaging details see Mechanical Dimensions section.

Key Parameters

ITEM		TC5118165BJ/BFT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Department of Commerce prior to export. Any export or re-export, directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.
2. LIFE SUPPORT POLICY

   Toshiba products described in this document are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

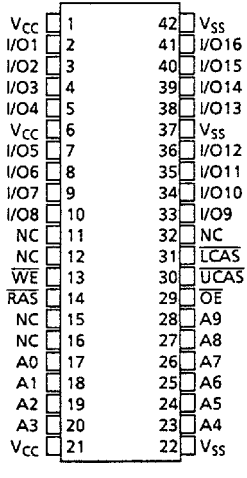
   A critical component in any component of a life support system whose failure to perform may cause a malfunction of the life support system, or may affect its safety or effectiveness.
3. The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this data book is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.

Pin Name

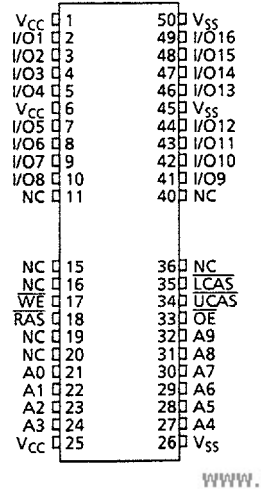
A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/ Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/ Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 ~ I/O16	Data Input/Output
V_{CC}	Power (+5.0V)
V_{SS}	Ground
NC	No Connection

Pin Connection (Top View)

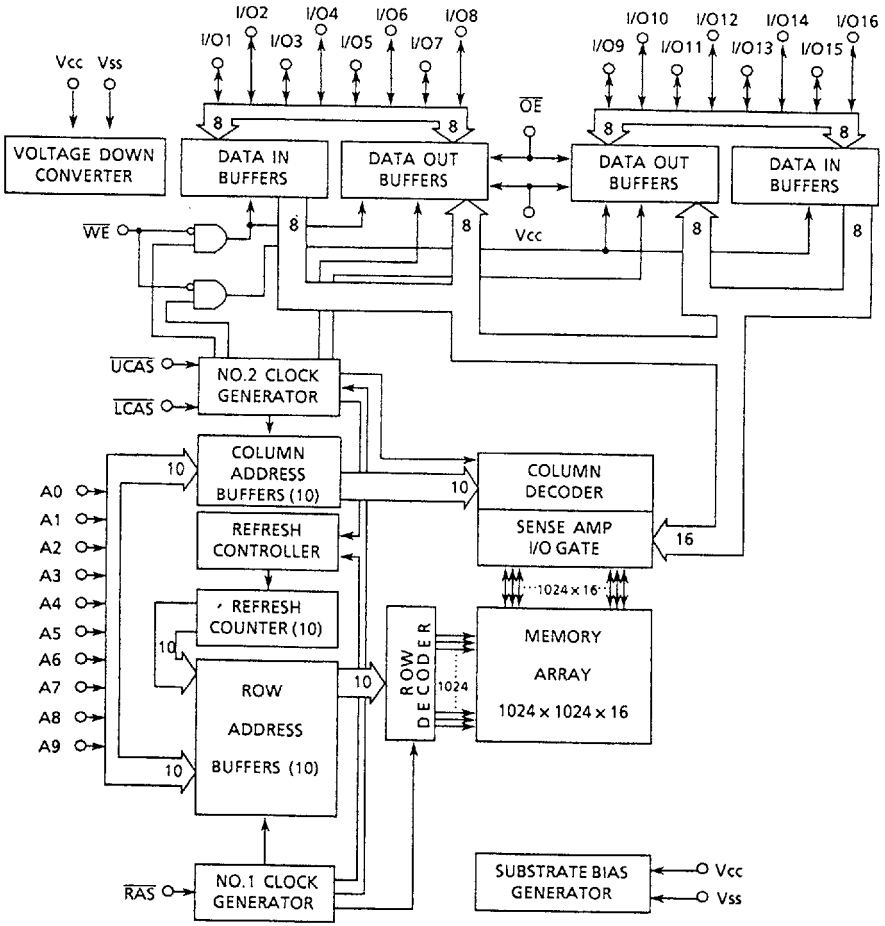
Plastic SOJ



Plastic TSOP



Block Diagram



Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V	1
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V	1
Power Supply Voltage	V_{CC}	-0.5 ~ 7.0	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.3	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	$V_{CC}+0.5^{*}$	V	2
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20ns (pulse width is measured at V_{CC}).
**-2.0V at pulse width ≤ 20ns (pulse width is measured at V_{SS}).

DC Electrical Characteristics (V_{CC} = 5V±10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{ULAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	150	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{ULAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$=$\overline{ULAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 5
		TC5118165BJ/BFT-70	-	150	mA	
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$, $\overline{ULAS}$, Address Cycling: t_{HPC}=t_{HPC} MIN.)	TC5118165BJ/BFT-60	-	110	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	100	mA	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{ULAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{ULAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	150	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤0.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (0V≤V_{OUT}≤V_{CC})		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 5V±10%, Ta = 0 ~ 70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	157	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	17	-	20	ns	9, 14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	60	100,000	70	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	10	-	12	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Hyper Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	12	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	43	14	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	12	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	12	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	12	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	12	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	12	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	12	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	12	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	36	-	39	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	79	-	89	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	49	-	54	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	54	-	59	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	20	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	10	-	12	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	60	-	70	-	ns	
t_{HPC}	Hyper Page Mode Cycle Time	25	-	30	-	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	68	-	75	-	ns	
t_{COH}	Output Data Hold Time	5	-	5	-	ns	
t_{REZ}	Output Buffer Turn-off Delay from $\overline{RAS}$	0	15	0	15	ns	10, 16
t_{WEZ}	Output Buffer Turn-off Delay from $\overline{WE}$	0	15	0	15	ns	10
t_{WED}	$\overline{WE}$ to Data Delay	15	-	15	-	ns	
t_{OE}	$\overline{OE}$ Pulse Width	15	-	20	-	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	10	-	12	-	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	-	5	-	ns	

Capacitance (V_{CC} = 5V±10%, f = 1MHz, Ta = 0 ~ 70°C)

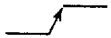
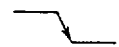
SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 ~ A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	
C_O	Input Capacitance (I/O1 ~ I/O16)	-	7	

Note: Please refer to Timing Diagrams Number 2.

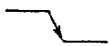
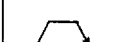
Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}$=V_{IL}. In case of I_{CC4}, it can be changed once or less during a hyper page mode cycle (t_{HPC}).
6. An initial pause of 500μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=2ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. This parameter is measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.), t_{OEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.), define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going (t_{OFF}). If $\overline{CAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going (t_{REZ}).

Data Out Hi-Z Control Logic

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"H"		"L"	"H"	t_{OFF}
	"H"	"L"	"H"	t_{REZ}
"L"	"L"		"H"	t_{OEZ}
"L"	"H"	"L"		t_{WEZ}

Data Out Lo-Z Control Logic

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"L"		"L"	"H"	t_{CLZ}
"L"	"L"		"H"	t_{OLZ}
"L"	"L"		"H"	t_{OLZ}