

4,194,304 WORD x 1 BIT DYNAMIC RAM

\* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514100J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514100J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

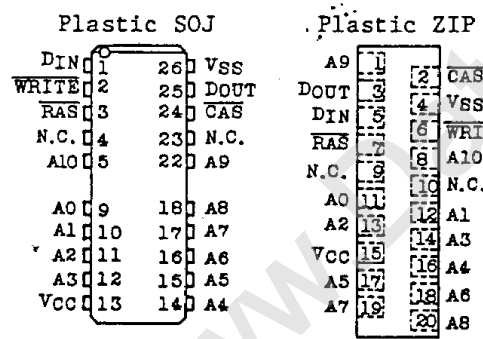
FEATURES

- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

|                  |                            | TC514100J/Z-80/-10 |       |
|------------------|----------------------------|--------------------|-------|
| t <sub>RAC</sub> | RAS Access Time            | 80ns               | 100ns |
| t <sub>AA</sub>  | Column Address Access Time | 40ns               | 50ns  |
| t <sub>CAC</sub> | CAS Access Time            | 20ns               | 25ns  |
| t <sub>RC</sub>  | Cycle Time                 | 150ns              | 180ns |
| t <sub>PC</sub>  | Fast Page Mode Cycle Time  | 50ns               | 60ns  |

- Low Power  
550mW Operating (TC514100J/Z-80)  
468mW Operating (TC514100J/Z-10)  
5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514100J  
Plastic ZIP: TC514100Z

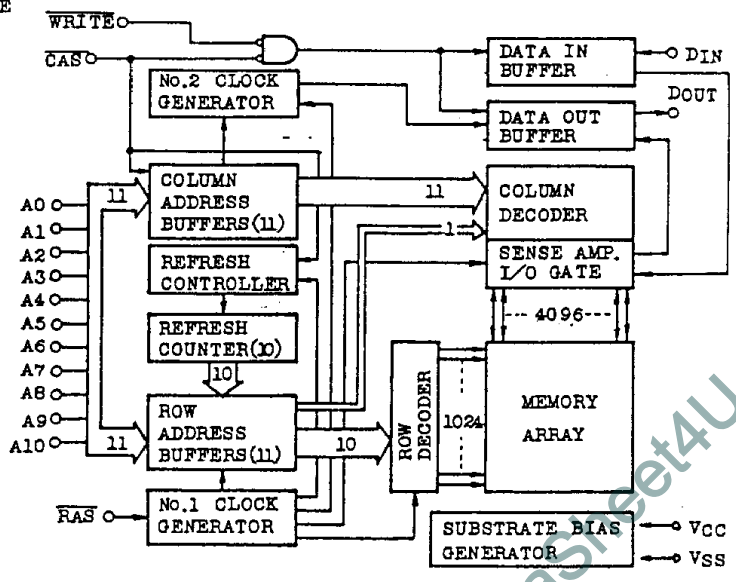
PIN CONNECTION (TOP VIEW)



PIN NAMES

|          |                       |
|----------|-----------------------|
| A0 ~ A10 | Address Inputs        |
| RAS      | Row Address Strobe    |
| DIN      | Data In               |
| DOUT     | Data Out              |
| CAS      | Column Address Strobe |
| WRITE    | Read/Write Input      |
| VCC      | Power (+5V)           |
| VSS      | Ground                |
| N.C.     | No Connection         |

BLOCK DIAGRAM



# TC514100J/Z-80

# TC514100J/Z-10

## ABSOLUTE MAXIMUM RATINGS

| ITEM                         | SYMBOL              | RATING    | UNITS    | NOTE |
|------------------------------|---------------------|-----------|----------|------|
| Input Voltage                | V <sub>IN</sub>     | -1 ~ 7    | V        | 1    |
| Output Voltage               | V <sub>OUT</sub>    | -1 ~ 7    | V        | 1    |
| Power Supply Voltage         | V <sub>CC</sub>     | -1 ~ 7    | V        | 1    |
| Operating Temperature        | T <sub>OPR</sub>    | 0 ~ 70    | °C       | 1    |
| Storage Temperature          | T <sub>STG</sub>    | -55 ~ 150 | °C       | 1    |
| Soldering Temperature · Time | T <sub>SOLDER</sub> | 260 · 10  | °C · sec | 1    |
| Power Dissipation            | P <sub>D</sub>      | 600       | mW       | 1    |
| Short Circuit Output Current | I <sub>OUT</sub>    | 50        | mA       | 1    |

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

| SYMBOL          | PARAMETER          | MIN. | TYP. | MAX. | UNIT | NOTE |
|-----------------|--------------------|------|------|------|------|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5  | 5.0  | 5.5  | V    | 2    |
| V <sub>IH</sub> | Input High Voltage | 2.4  | -    | 6.5  | V    | 2    |
| V <sub>IL</sub> | Input Low Voltage  | -1.0 | -    | 0.8  | V    | 2    |

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C)

| SYMBOL            | PARAMETER   | MIN.           | MAX. | UNITS | NOTES |       |
|-------------------|---|----------------|------|-------|-------|-------|
| I <sub>CC1</sub>  | OPERATING CURRENT<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC}=t_{RC\ MIN.}$ )   | TC514100J/Z-80 | -    | 100   | mA    | 3,4,5 |
|                   |   | TC514100J/Z-10 | -    | 85    |       |       |
| I <sub>CC2</sub>  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS}=\overline{CAS}=V_{IH}$ )   | -              | 2    | mA    |       |       |
| I <sub>CC3</sub>  | $\overline{RAS}$ ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$ Only Mode<br>( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC\ MIN.}$ )                                | TC514100J/Z-80 | -    | 100   | mA    | 3,5   |
|                   |   | TC514100J/Z-10 | -    | 85    |       |       |
| I <sub>CC4</sub>  | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode<br>( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{PC}=t_{PC\ MIN.}$ )   | TC514100J/Z-80 | -    | 60    | mA    | 3,4,5 |
|                   |   | TC514100J/Z-10 | -    | 50    |       |       |
| I <sub>CC5</sub>  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )  | -              | 1    | mA    |       |       |
| I <sub>CC6</sub>  | $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$ Before<br>$\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC\ MIN.}$ ) | TC514100J/Z-80 | -    | 100   | mA    | 3     |
|                   |   | TC514100J/Z-10 | -    | 85    |       |       |
| I <sub>I(L)</sub> | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , All Other<br>Pins Not Under Test=0V)   | -10            | 10   | μA    |       |       |
| I <sub>O(L)</sub> | OUTPUT LEAKAGE CURRENT<br>(D <sub>OUT</sub> is disabled, $0V \leq V_{OUT} \leq 5.5V$ )  | -10            | 10   | μA    |       |       |
| V <sub>OH</sub>   | OUTPUT LEVEL<br>Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)   | 2.4            | -    | V     |       |       |
| V <sub>OL</sub>   | OUTPUT LEVEL<br>Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)  | -              | 0.4  | V     |       |       |

# TC514100J/Z-80 TC514100J/Z-10

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub>=5V±10%, T<sub>a</sub>=0~70°C) (Notes 6, 7, 8)

| SYMBOL            | PARAMETER  | TC514100J/Z-80 |         | TC514100J/Z-10 |         | UNIT | NOTES   |
|-------------------|--|----------------|---------|----------------|---------|------|---------|
|                   |  | MIN.           | MAX.    | MIN.           | MAX.    |      |         |
| t <sub>RC</sub>   | Random Read or Write Cycle Time  | 150            | -       | 180            | -       | ns   |         |
| t <sub>RMW</sub>  | Read-Modify-Write Cycle Time   | 175            | -       | 210            | -       | ns   |         |
| t <sub>PC</sub>   | Fast Page Mode Cycle Time  | 50             | -       | 60             | -       | ns   |         |
| t <sub>PRMW</sub> | Fast Page Mode Read-Modify-Write Cycle Time                            | 75             | -       | 90             | -       | ns   |         |
| t <sub>RAC</sub>  | Access Time from $\overline{\text{RAS}}$                               | -              | 80      | -              | 100     | ns   | 9,14,15 |
| t <sub>CAC</sub>  | Access Time from $\overline{\text{CAS}}$                               | -              | 20      | -              | 25      | ns   | 9,14    |
| t <sub>AA</sub>   | Access Time from Column Address  | -              | 40      | -              | 50      | ns   | 9,15    |
| t <sub>CPA</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                     | -              | 45      | -              | 55      | ns   | 9       |
| t <sub>CLZ</sub>  | $\overline{\text{CAS}}$ to Output in Low-Z                             | 0              | -       | 0              | -       | ns   | 9       |
| t <sub>OFF</sub>  | Output Buffer Turn-off Delay   | 0              | 20      | 0              | 20      | ns   | 10      |
| t <sub>T</sub>    | Transition Time (Rise and Fall)  | 3              | 50      | 3              | 50      | ns   | 8       |
| t <sub>RP</sub>   | $\overline{\text{RAS}}$ Precharge Time                                 | 60             | -       | 70             | -       | ns   |         |
| t <sub>RAS</sub>  | $\overline{\text{RAS}}$ Pulse Width                                    | 80             | 10,000  | 100            | 10,000  | ns   |         |
| t <sub>RASP</sub> | $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)                   | 80             | 200,000 | 100            | 200,000 | ns   |         |
| t <sub>RSH</sub>  | $\overline{\text{RAS}}$ Hold Time                                      | 20             | -       | 25             | -       | ns   |         |
| t <sub>CSH</sub>  | $\overline{\text{CAS}}$ Hold Time                                      | 80             | -       | 100            | -       | ns   |         |
| t <sub>RHCP</sub> | $\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time | 45             | -       | 55             | -       | ns   |         |
| t <sub>CAS</sub>  | $\overline{\text{CAS}}$ Pulse Width                                    | 20             | 10,000  | 25             | 10,000  | ns   |         |
| t <sub>RCD</sub>  | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time          | 20             | 60      | 25             | 75      | ns   | 14      |
| t <sub>RAD</sub>  | $\overline{\text{RAS}}$ to Column Address Delay Time                   | 15             | 40      | 20             | 50      | ns   | 15      |
| t <sub>CRP</sub>  | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time      | 5              | -       | 10             | -       | ns   |         |
| t <sub>CP</sub>   | $\overline{\text{CAS}}$ Precharge Time                                 | 10             | -       | 10             | -       | ns   |         |
| t <sub>ASR</sub>  | Row Address Set-Up Time  | 0              | -       | 0              | -       | ns   |         |
| t <sub>RAH</sub>  | Row Address Hold Time  | 10             | -       | 15             | -       | ns   |         |
| t <sub>ASC</sub>  | Column Address Set-Up Time   | 0              | -       | 0              | -       | ns   |         |
| t <sub>CAH</sub>  | Column Address Hold Time   | 15             | -       | 20             | -       | ns   |         |
| t <sub>AR</sub>   | Column Address Hold Time referenced to $\overline{\text{RAS}}$         | 60             | -       | 75             | -       | ns   |         |
| t <sub>RAL</sub>  | Column Address to $\overline{\text{RAS}}$ Lead Time                    | 40             | -       | 50             | -       | ns   |         |
| t <sub>RCS</sub>  | Read Command Set-Up Time   | 0              | -       | 0              | -       | ns   |         |
| t <sub>RCH</sub>  | Read Command Hold Time   | 0              | -       | 0              | -       | ns   | 11      |
| t <sub>RRH</sub>  | Read Command Hold Time referenced to $\overline{\text{RAS}}$           | 0              | -       | 0              | -       | ns   | 11      |
| t <sub>WCH</sub>  | Write Command Hold Time  | 15             | -       | 20             | -       | ns   |         |

**TC514100J/Z-80**  
**TC514100J/Z-10**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

| SYMBOL            | PARAMETER   | TC514100J/Z<br>-80 |      | TC514100J/Z<br>-10 |      | UNITS | NOTES |
|-------------------|---|--------------------|------|--------------------|------|-------|-------|
|                   |   | MIN.               | MAX. | MIN.               | MAX. |       |       |
| t <sub>WCR</sub>  | Write Command Hold Time referenced to $\overline{\text{RAS}}$   | 60                 | -    | 75                 | -    | ns    |       |
| t <sub>WP</sub>   | Write Command Pulse Width   | 15                 | -    | 20                 | -    | ns    |       |
| t <sub>RWL</sub>  | Write Command to $\overline{\text{RAS}}$ Lead Time  | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>CWL</sub>  | Write Command to $\overline{\text{CAS}}$ Lead Time  | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>DS</sub>   | Data Set-Up Time  | 0                  | -    | 0                  | -    | ns    | 12    |
| t <sub>DH</sub>   | Data Hold Time  | 15                 | -    | 20                 | -    | ns    | 12    |
| t <sub>DHR</sub>  | Data Hold Time referenced to $\overline{\text{RAS}}$  | 60                 | -    | 75                 | -    | ns    |       |
| t <sub>REF</sub>  | Refresh Period  | -                  | 16   | -                  | 16   | ms    |       |
| t <sub>WCS</sub>  | Write Command Set-Up Time   | 0                  | -    | 0                  | -    | ns    | 13    |
| t <sub>CWD</sub>  | $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time   | 20                 | -    | 25                 | -    | ns    | 13    |
| t <sub>RWD</sub>  | $\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay Time   | 80                 | -    | 100                | -    | ns    | 13    |
| t <sub>AWD</sub>  | Column Address to $\overline{\text{WRITE}}$ Delay Time  | 40                 | -    | 50                 | -    | ns    | 13    |
| t <sub>CPWD</sub> | $\overline{\text{CAS}}$ Precharge to $\overline{\text{WRITE}}$ Delay Time (Fast Page Mode)  | 45                 | -    | 55                 | -    | ns    | 13    |
| t <sub>CSR</sub>  | $\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)                                 | 5                  | -    | 5                  | -    | ns    |       |
| t <sub>CHR</sub>  | $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)                                   | 15                 | -    | 20                 | -    | ns    |       |
| t <sub>RPC</sub>  | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time   | 0                  | -    | 0                  | -    | ns    |       |
| t <sub>CPT</sub>  | $\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test Cycle)                 | 40                 | -    | 50                 | -    | ns    |       |
| t <sub>WTS</sub>  | Write Command Set-Up Time (Test Mode In)  | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WTH</sub>  | Write Command Hold Time (Test Mode In)  | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WRP</sub>  | $\overline{\text{WRITE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle) | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WRH</sub>  | $\overline{\text{WRITE}}$ to $\overline{\text{RAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)      | 10                 | -    | 10                 | -    | ns    |       |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 6, 7, 8)

| SYMBOL     | PARAMETER  | TC514100J/Z<br>-80 |         | TC514100J/Z<br>-10 |         | UNIT | NOTES   |
|------------|--|--------------------|---------|--------------------|---------|------|---------|
|            |  | MIN.               | MAX.    | MIN.               | MAX.    |      |         |
| $t_{RC}$   | Random Read or Write Cycle Time                          | 155                | -       | 185                | -       | ns   |         |
| $t_{PC}$   | Fast Page Mode Cycle Time                                | 55                 | -       | 65                 | -       | ns   |         |
| $t_{RAC}$  | Access Time from $\overline{RAS}$                        | -                  | 85      | -                  | 105     | ns   | 9,14,15 |
| $t_{CAC}$  | Access Time from $\overline{CAS}$                        | -                  | 25      | -                  | 30      | ns   | 9,14    |
| $t_{AA}$   | Access Time from Column Address                          | -                  | 45      | -                  | 55      | ns   | 9,15    |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge              | -                  | 50      | -                  | 60      | ns   | 9       |
| $t_{RAS}$  | $\overline{RAS}$ Pulse Width                             | 85                 | 10,000  | 105                | 10,000  | ns   |         |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode)            | 85                 | 200,000 | 105                | 200,000 | ns   |         |
| $t_{RSH}$  | $\overline{RAS}$ Hold Time                               | 25                 | -       | 30                 | -       | ns   |         |
| $t_{CSH}$  | $\overline{CAS}$ Hold Time                               | 85                 | -       | 105                | -       | ns   |         |
| $t_{RHCP}$ | $\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time | 50                 | -       | 60                 | -       | ns   |         |
| $t_{CAS}$  | $\overline{CAS}$ Pulse Width                             | 25                 | 10,000  | 30                 | 10,000  | ns   |         |
| $t_{RAL}$  | Column Address to $\overline{RAS}$ Lead Time             | 45                 | -       | 55                 | -       | ns   |         |

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1MHz$ ,  $T_a=0\sim 70^\circ C$ )

| SYMBOL   | PARAMETER  | MIN. | MAX. | UNIT |
|----------|--|------|------|------|
| $C_{I1}$ | Input Capacitance ( $A_0\sim A_{10}$ , $D_{IN}$ )                              | -    | 5    | pF   |
| $C_{I2}$ | Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WRITE}$ ) | -    | 7    | pF   |
| $C_O$    | Output Capacitance ( $D_{OUT}$ )   | -    | 7    | pF   |

# TC514100J/Z-80

# TC514100J/Z-10

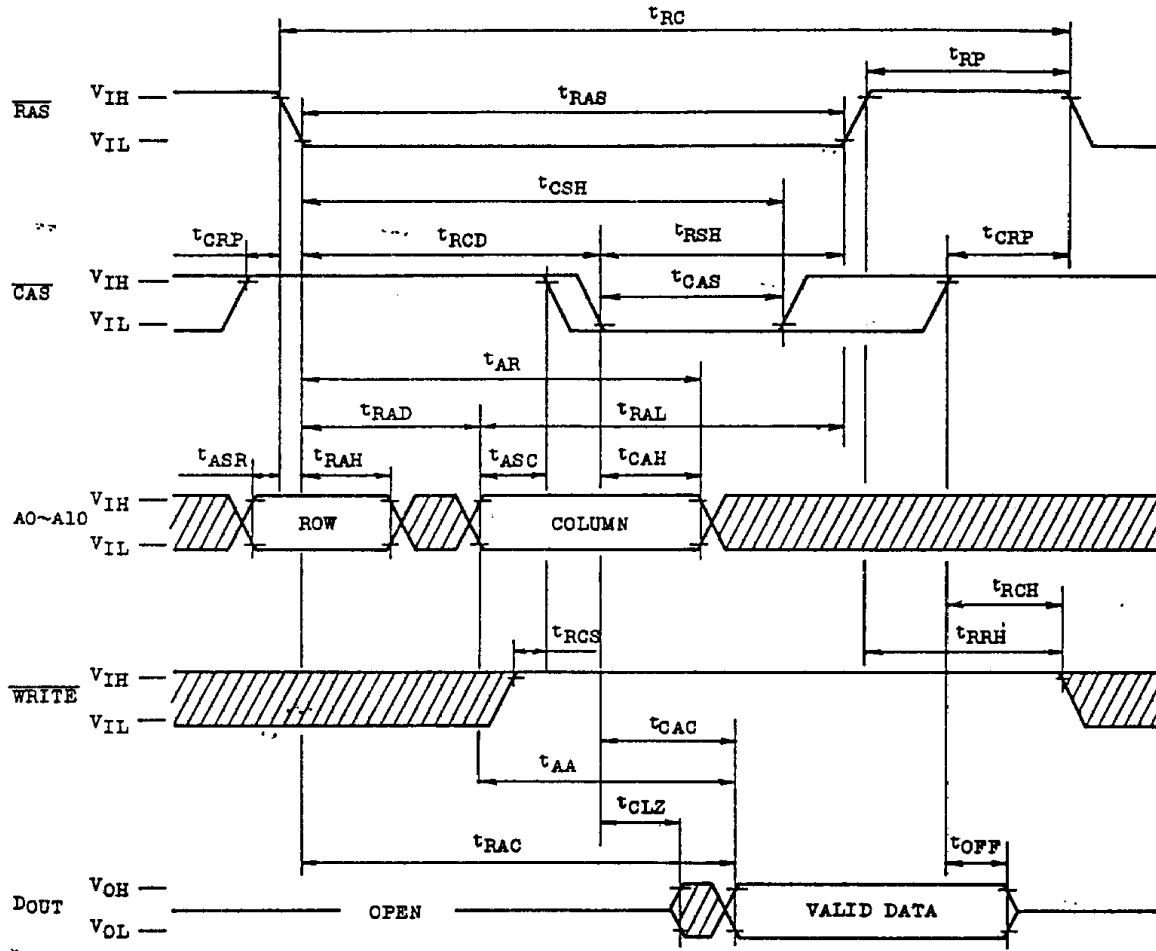
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## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while  $\overline{RAS}=V_{IL}$  and  $\overline{CAS}=V_{IH}$ .
6. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles instead of 8  $\overline{RAS}$  only refresh cycles are required.
7. AC measurements assume  $t_T=5$ ns.
8.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-modify-write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet at electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

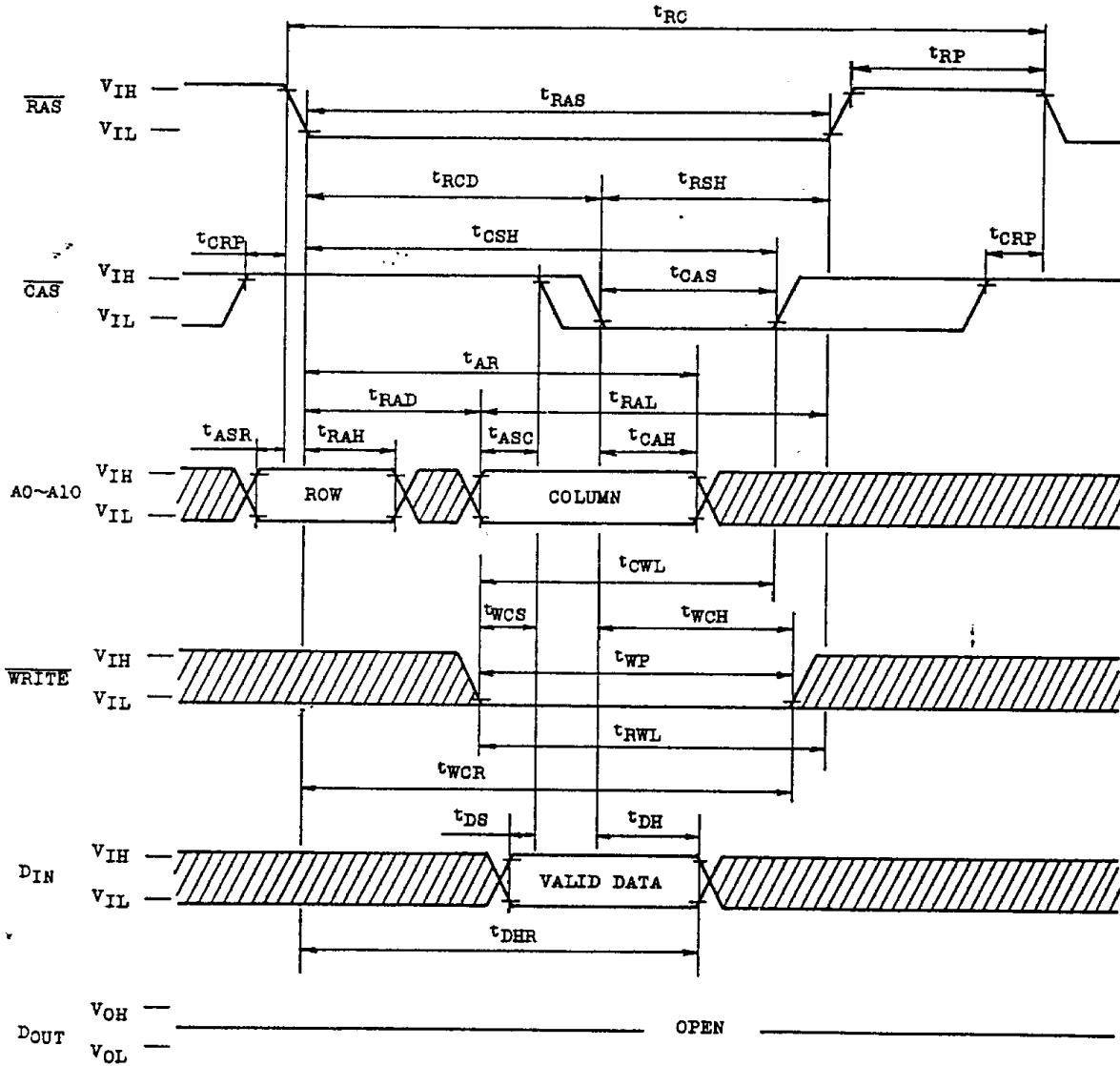
TIMING WAVEFORMS

READ CYCLE



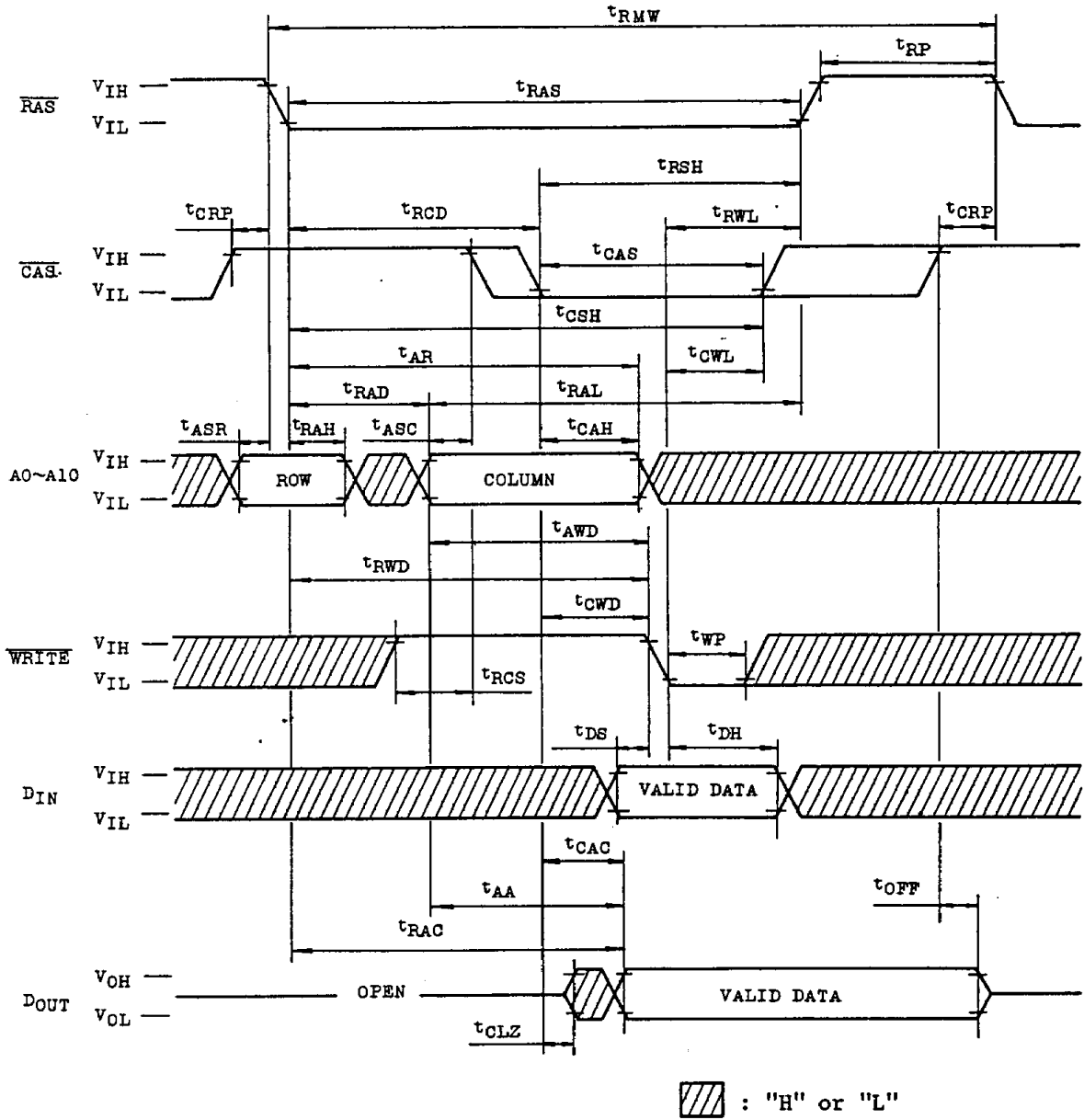
TC514100J/Z-80  
 TC514100J/Z-10

WRITE CYCLE (EARLY WRITE)



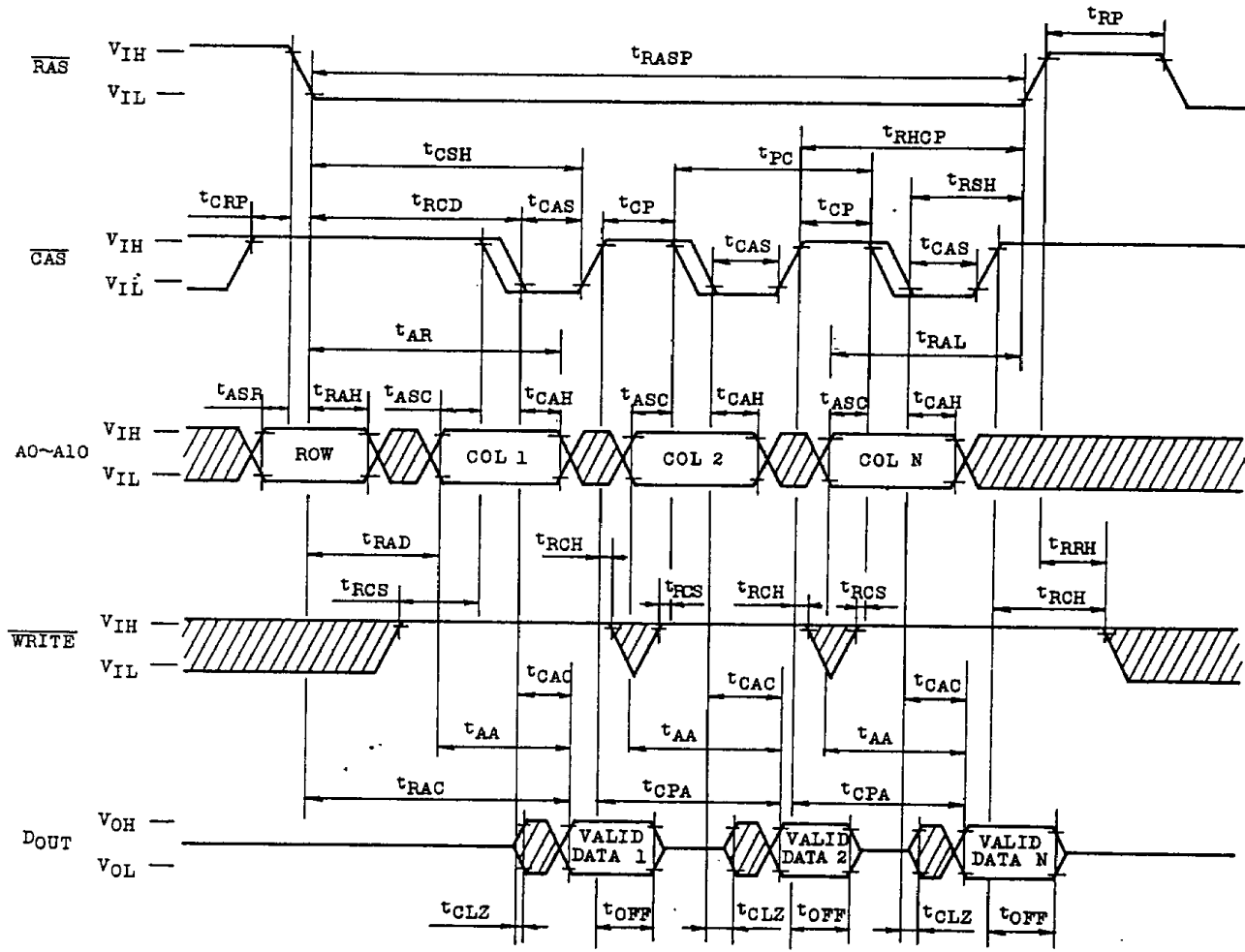


READ-MODIFY-WRITE CYCLE



TC514100J/Z-80  
TC514100J/Z-10

FAST PAGE MODE READ CYCLE

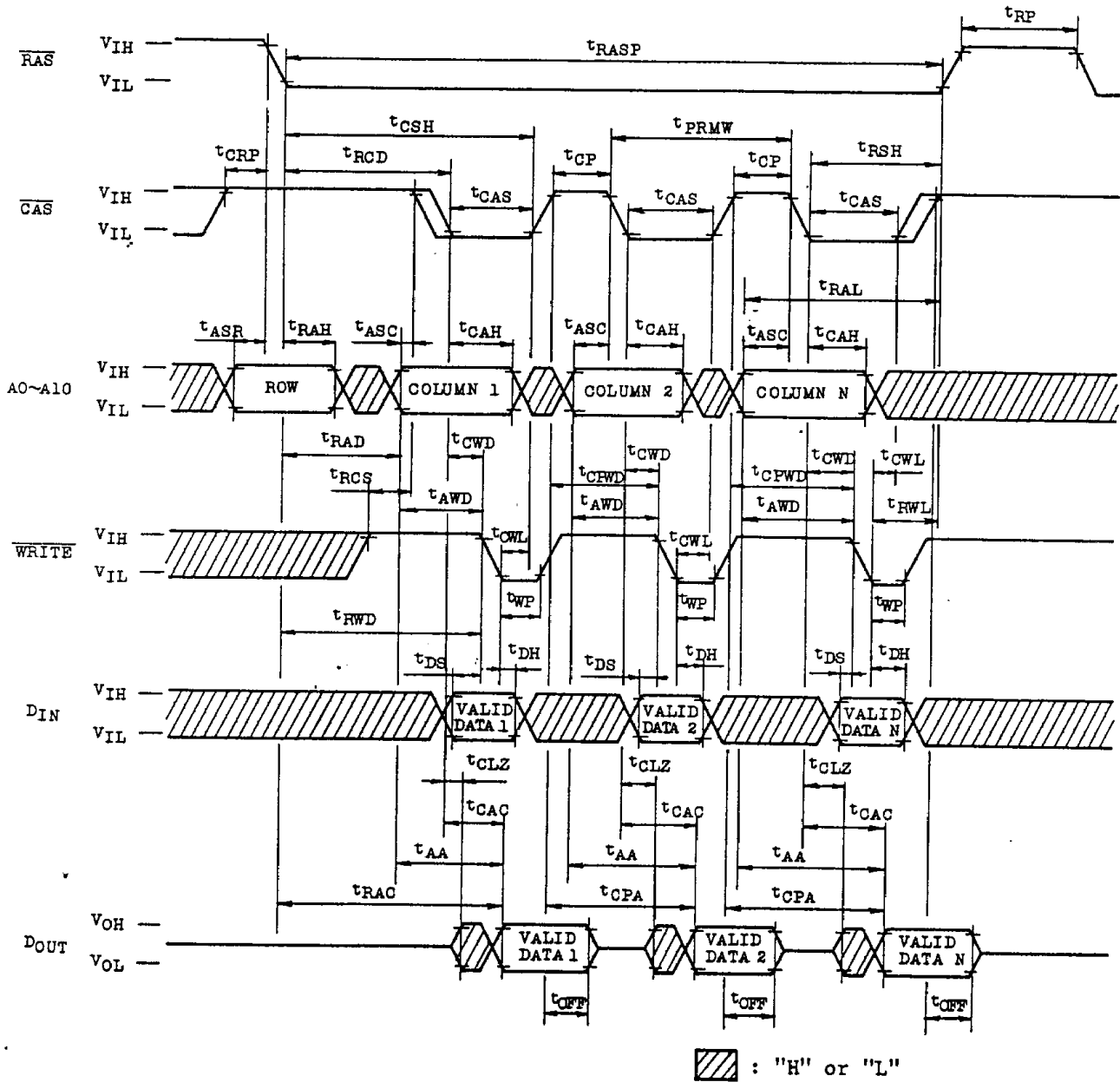


▨ : "H" or "L"

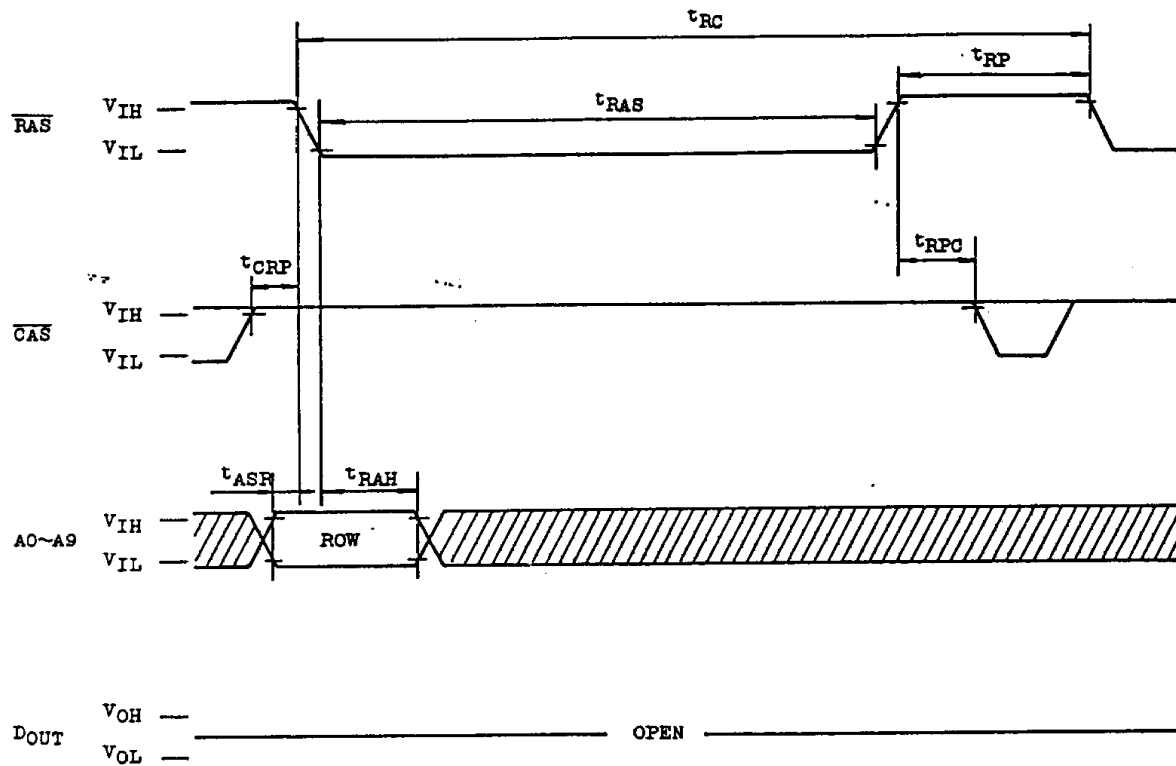


TC514100J/Z-80  
TC514100J/Z-10

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS ONLY REFRESH CYCLE

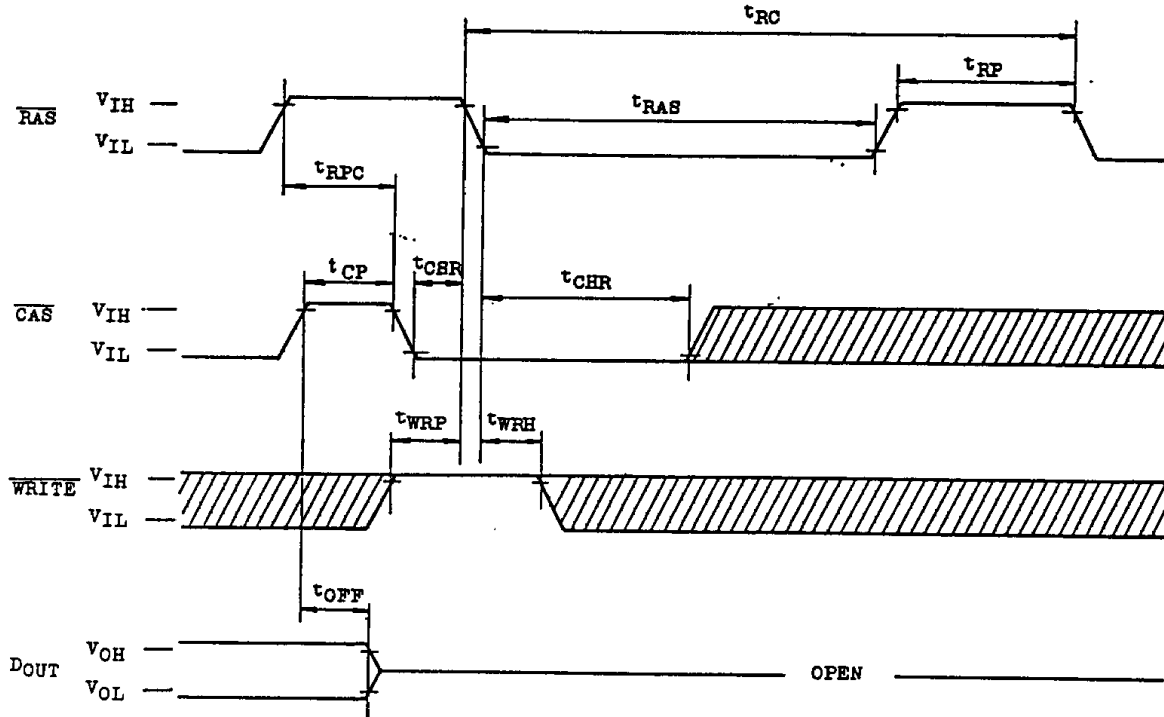


 : "H" or "L"

NOTE: WRITE="H" or "L", A10="H" or "L"

TC514100J/Z-80  
 TC514100J/Z-10

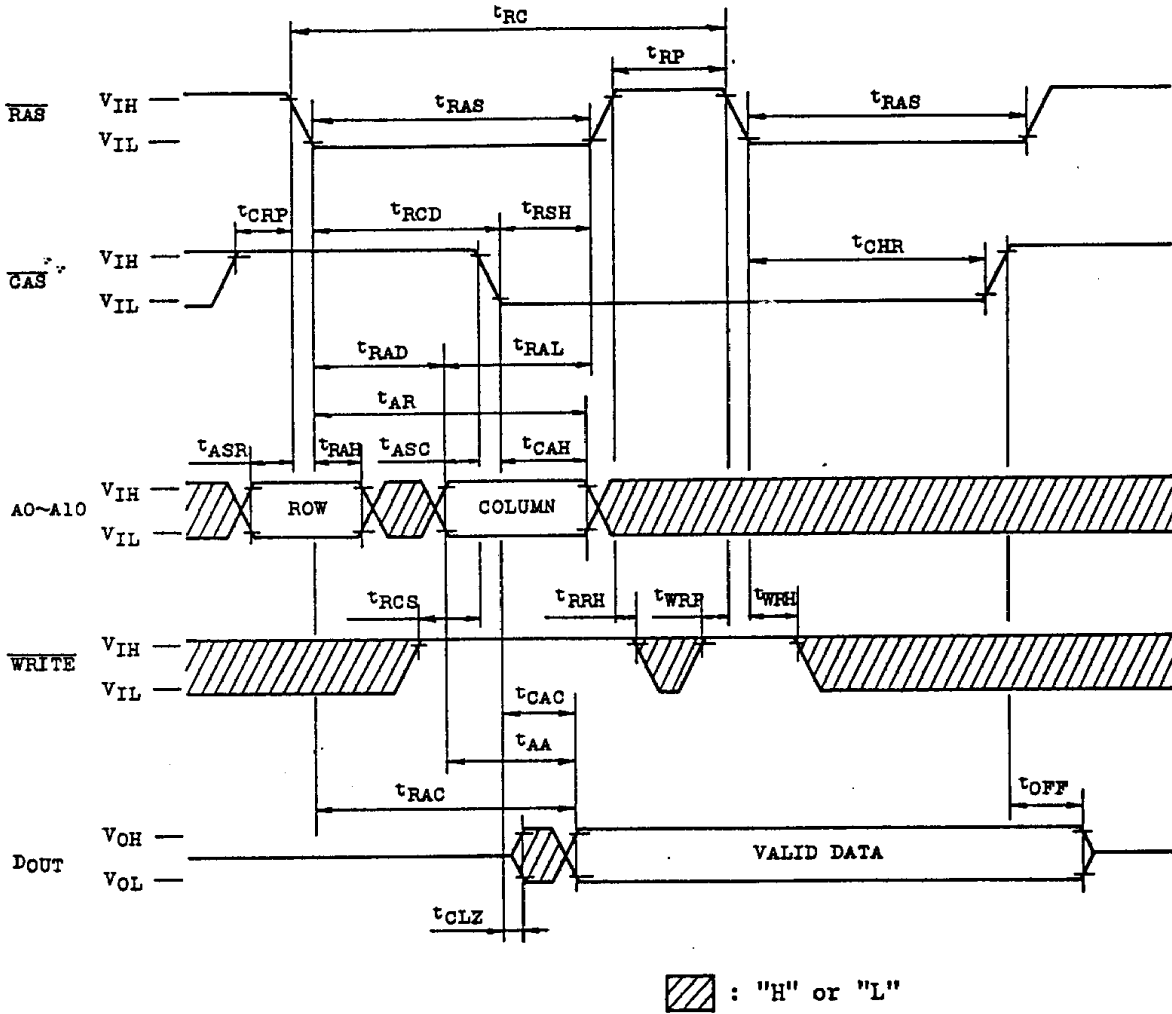
CAS BEFORE RAS REFRESH CYCLE



NOTE: A0 ~ A10="H" or "L"

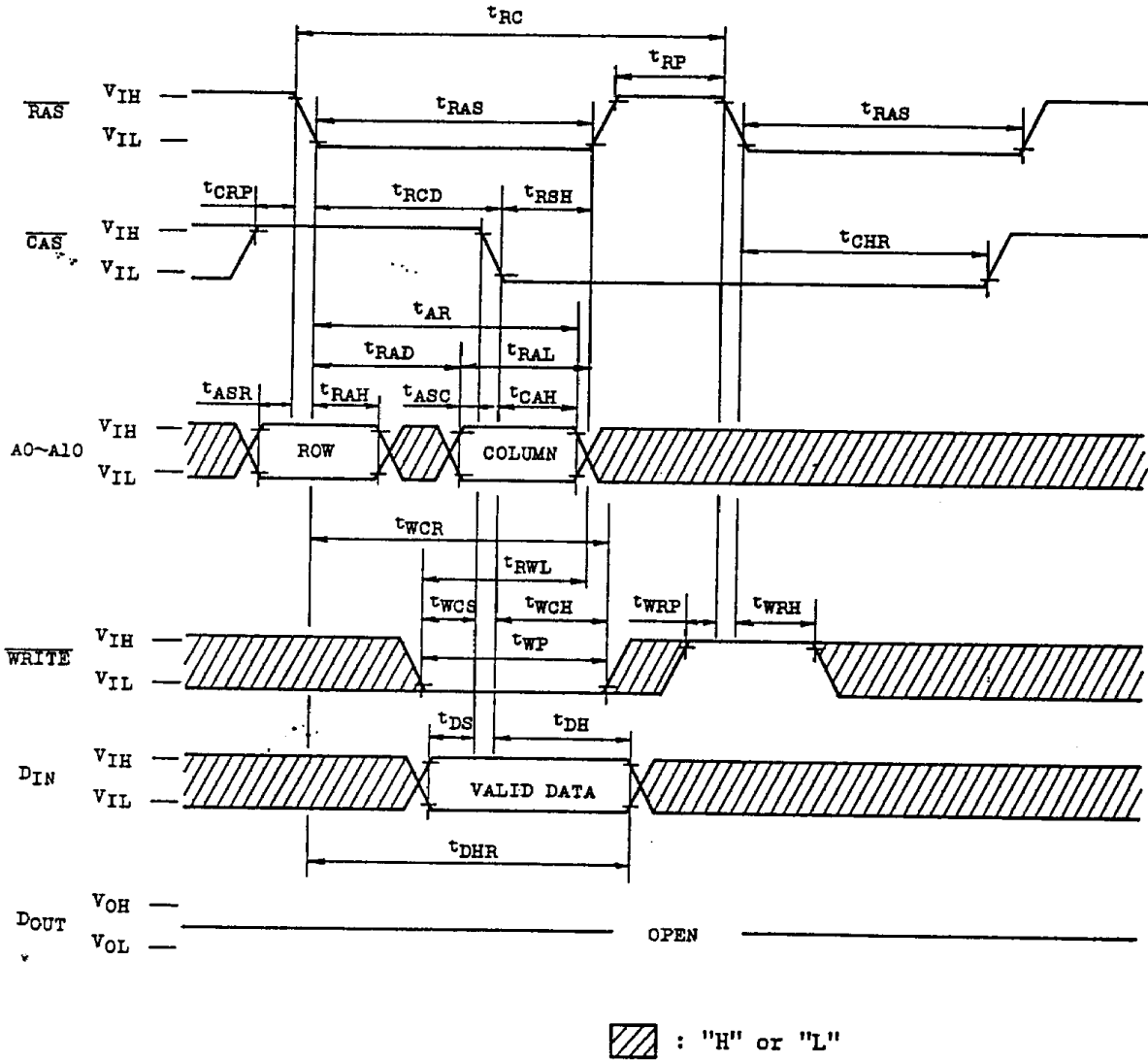
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



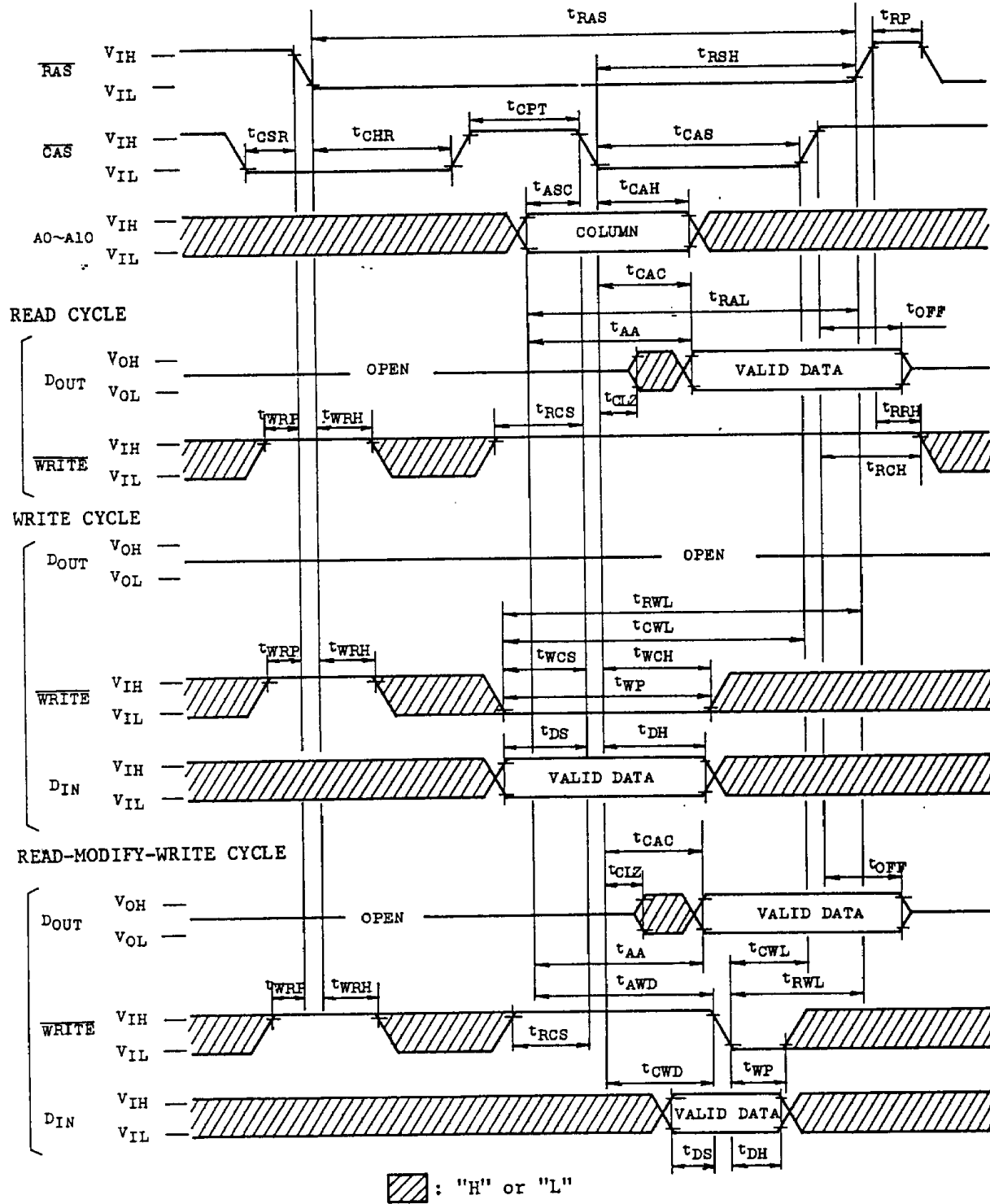
TC514100J/Z-80  
 TC514100J/Z-10

HIDDEN REFRESH CYCLE (WRITE)



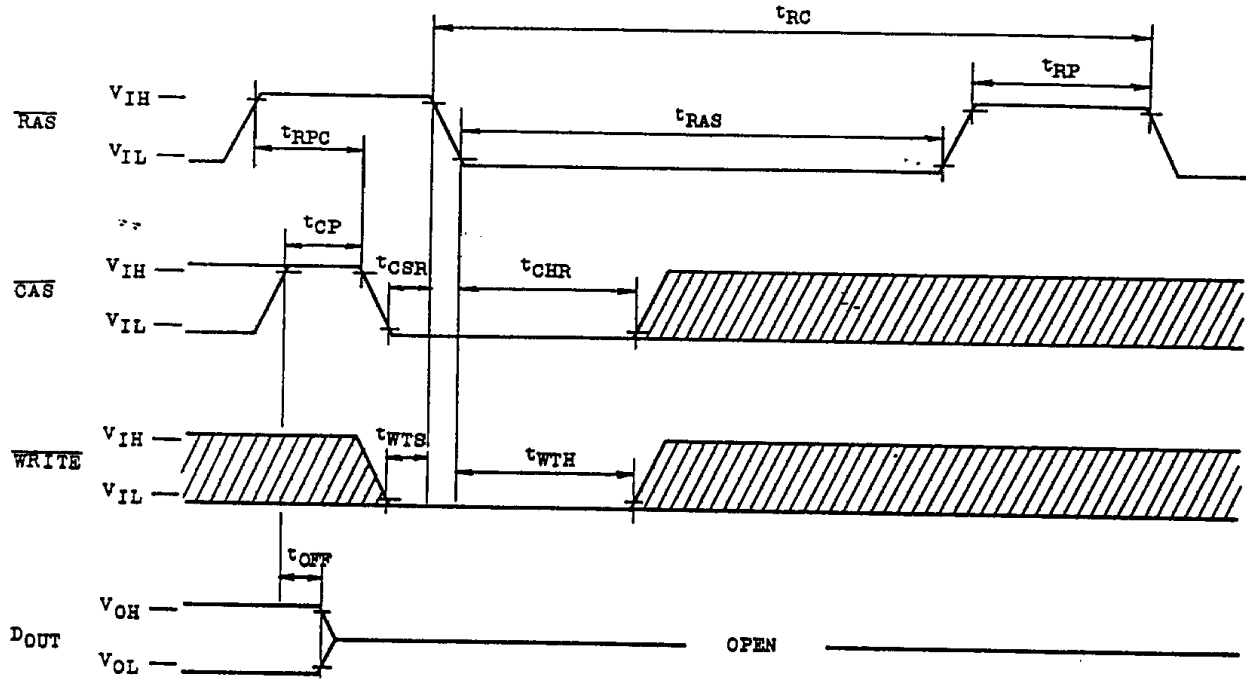


CAS BEFORE RAS REFRESH COUNTER TEST CYCLE




TC514100J/Z-80  
 TC514100J/Z-10

WRITE,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE



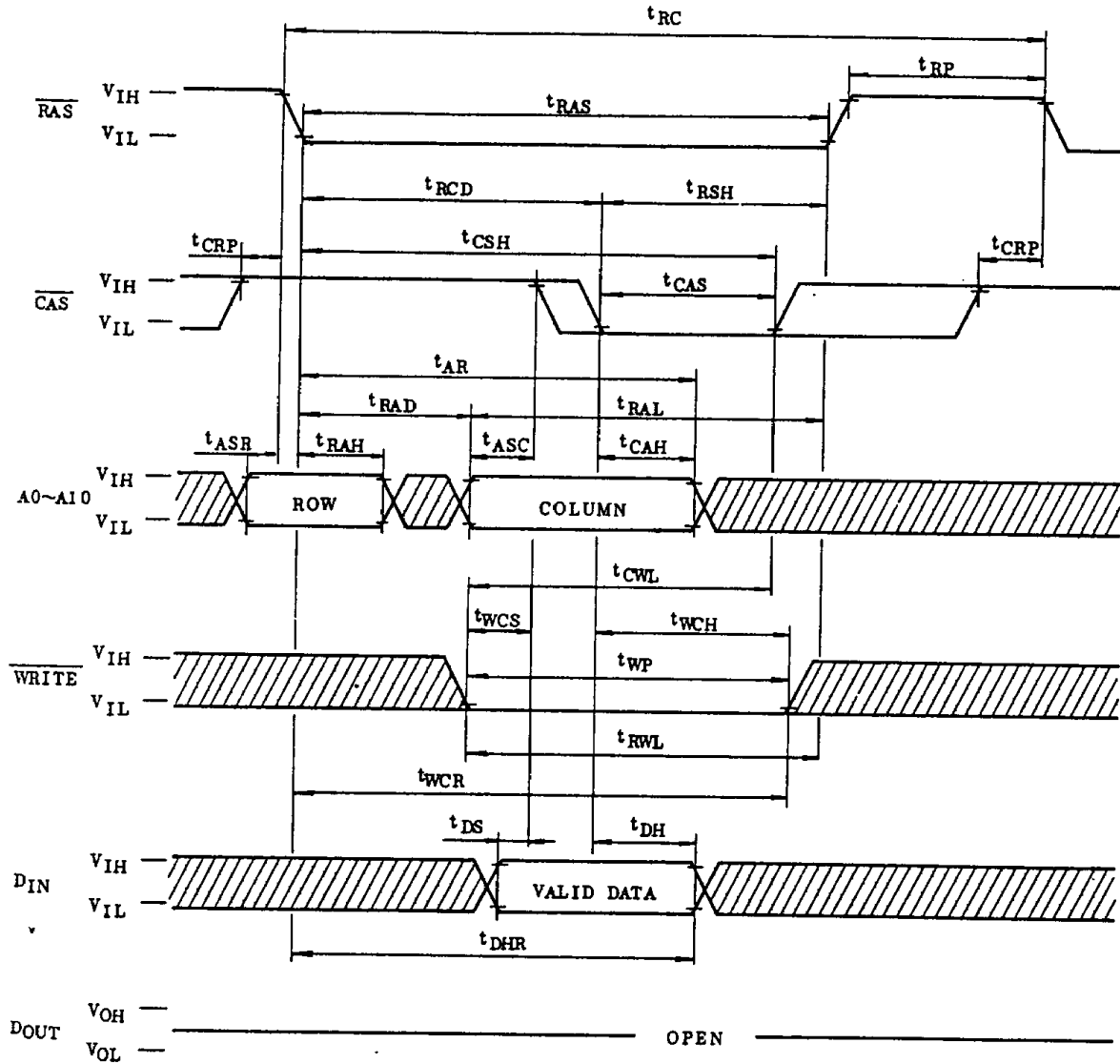
NOTE:  $D_{IN}$ ,  $A_0 \sim A_{10}$ : "H" or "L"


 : "H" or "L"



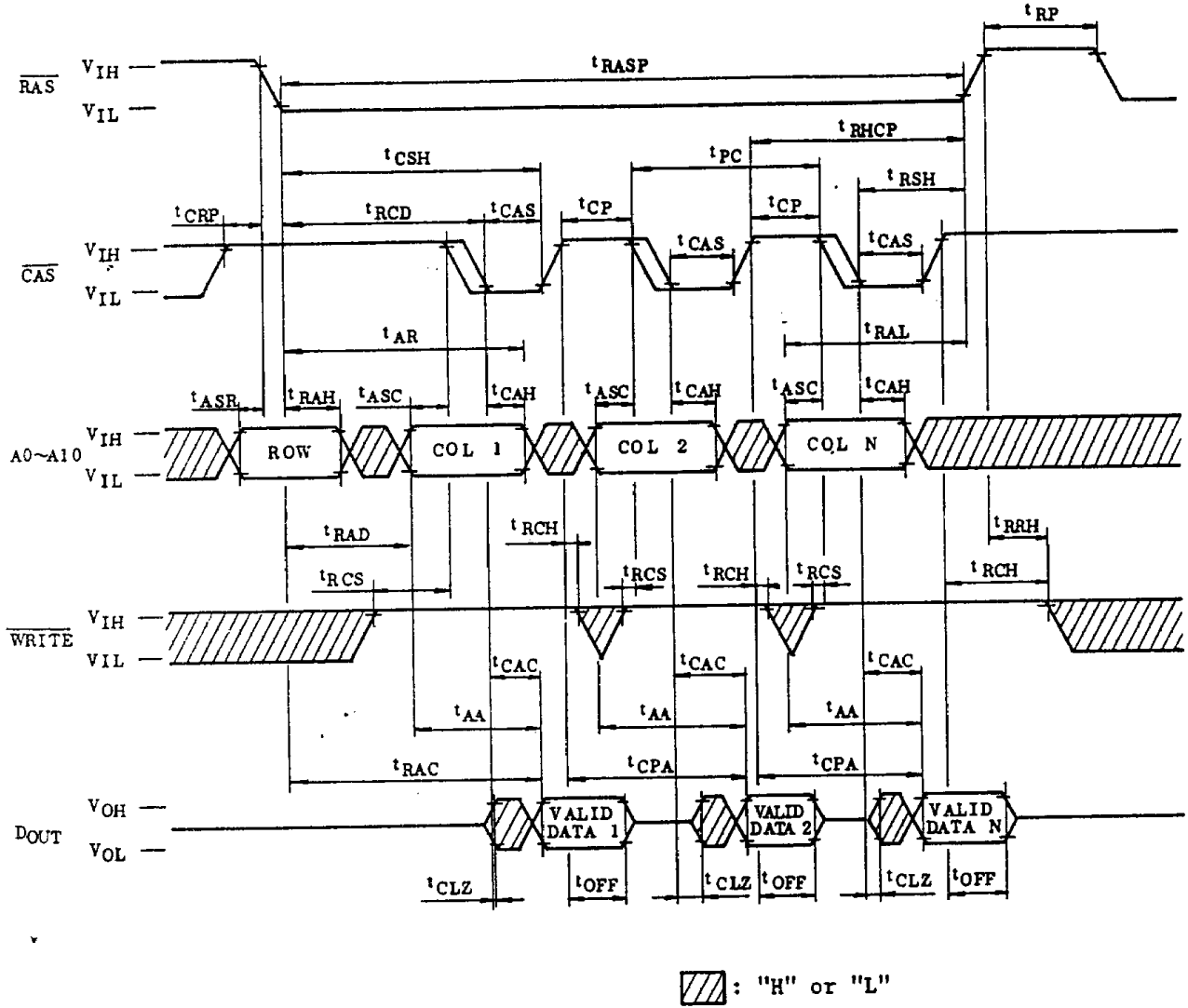
TC514100J/Z-80  
 TC514100J/Z-10

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



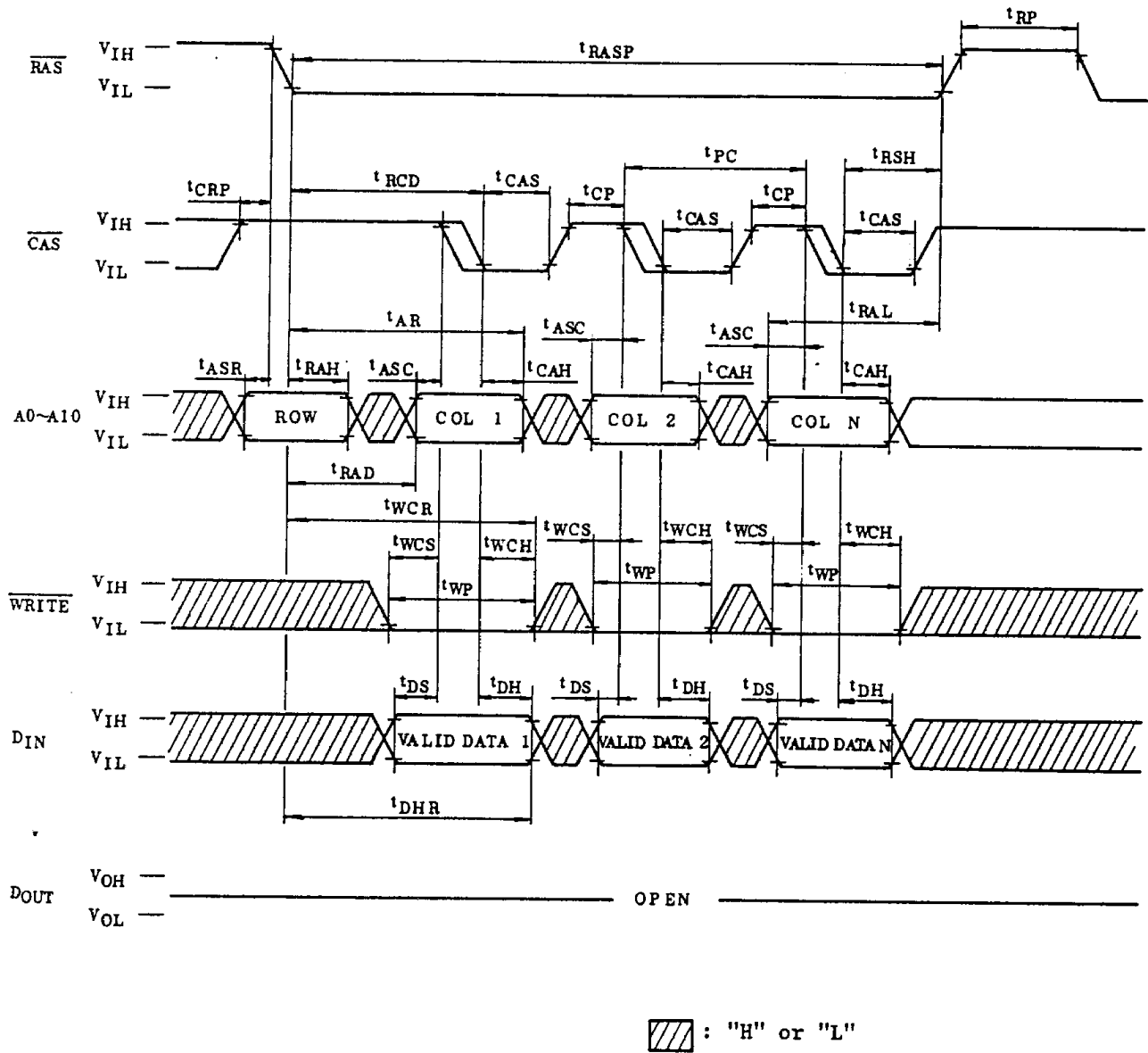
 : "H" or "L"

FAST PAGE MODE READ CYCLE IN THE TEST MODE



TC514100J/Z-80  
TC514100J/Z-10

FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



## TEST MODE

The TC514100J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A<sub>10R</sub>, A<sub>10C</sub> and A<sub>0C</sub> are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514100J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

" $\overline{\text{WRITE}}$ ,  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" puts the device into "Test Mode". And " $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" or " $\overline{\text{RAS}}$  Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{WRITE}}$ ,  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern)..

