

1,048,576 WORD x 4 BIT DYNAMIC RAM

\* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514400J/Z is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The TC514400J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

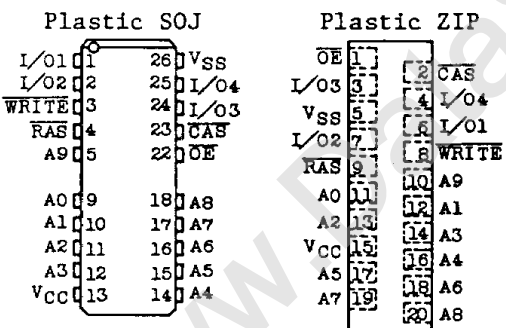
- 1,048,576 word by 4 bit organization
- Fast access time and cycle time

|                  |                            | TC514400J/Z-80/-10 |       |
|------------------|----------------------------|--------------------|-------|
| t <sub>RAC</sub> | RAS Access Time            | 80ns               | 100ns |
| t <sub>AA</sub>  | Column Address Access Time | 40ns               | 50ns  |
| t <sub>CAC</sub> | CAS Access Time            | 20ns               | 25ns  |
| t <sub>RC</sub>  | Cycle Time                 | 150ns              | 180ns |
| t <sub>PC</sub>  | Fast Page Mode Cycle Time  | 50ns               | 60ns  |

- Single power supply of 5V±10% with a built-in V<sub>BB</sub> generator

- Low Power  
578mW MAX. Operating (TC514400J/Z-80)  
495mW MAX. Operating (TC514400J/Z-10)  
5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514400J  
Plastic ZIP: TC514400Z

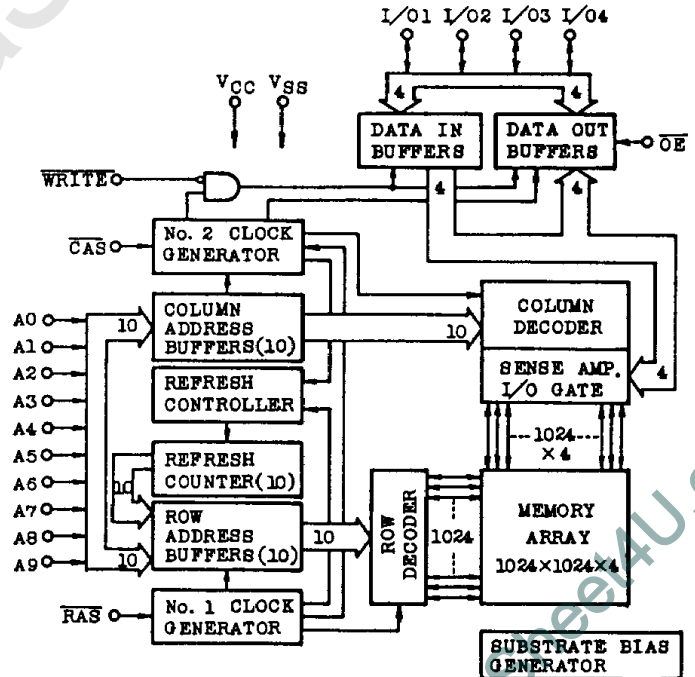
PIN CONNECTION (TOP VIEW)



PIN NAMES

|             |                       |
|-------------|-----------------------|
| A0 ~ A9     | Address Inputs        |
| RAS         | Row Address Strobe    |
| CAS         | Column Address Strobe |
| WRITE       | Read/Write Input      |
| OE          | Output Enable         |
| I/O1 ~ I/O4 | Data Input/Output     |
| VCC         | Power (+5V)           |
| VSS         | Ground                |

BLOCK DIAGRAM



# TC514400J/Z-80

# TC514400J/Z-10

## ABSOLUTE MAXIMUM RATINGS

| ITEM                         | SYMBOL       | RATING    | UNITS    | NOTE |
|------------------------------|--------------|-----------|----------|------|
| Input Voltage                | $V_{IN}$     | -1 ~ 7    | V        | 1    |
| Output Voltage               | $V_{OUT}$    | -1 ~ 7    | V        | 1    |
| Power Supply Voltage         | $V_{CC}$     | -1 ~ 7    | V        | 1    |
| Operating Temperature        | $T_{OPR}$    | 0 ~ 70    | °C       | 1    |
| Storage Temperature          | $T_{STG}$    | -55 ~ 150 | °C       | 1    |
| Soldering Temperature · Time | $T_{SOLDER}$ | 260 · 10  | °C · sec | 1    |
| Power Dissipation            | $P_D$        | 600       | mW       | 1    |
| Short Circuit Output Current | $I_{OUT}$    | 50        | mA       | 1    |

## RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0\sim 70^\circ\text{C}$ )

| SYMBOL   | PARAMETER          | MIN. | TYP. | MAX. | UNIT | NOTE |
|----------|--------------------|------|------|------|------|------|
| $V_{CC}$ | Supply Voltage     | 4.5  | 5.0  | 5.5  | V    | 2    |
| $V_{IH}$ | Input High Voltage | 2.4  | -    | 6.5  | V    | 2    |
| $V_{IL}$ | Input Low Voltage  | -1.0 | -    | 0.8  | V    | 2    |

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V\pm 10\%$ , $T_a=0\sim 70^\circ\text{C}$ )

| SYMBOL     | PARAMETER  | MIN.           | MAX. | UNITS | NOTES         |       |
|------------|--|----------------|------|-------|---------------|-------|
| $I_{CC1}$  | OPERATING CURRENT<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC}=t_{RC}$ MIN.)                            | TC514400J/Z-80 | -    | 105   | mA            | 3,4,5 |
|            |  | TC514400J/Z-10 | -    | 90    |               |       |
| $I_{CC2}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS}=\overline{CAS}=V_{IH}$ )  | TC514400J/Z-80 | -    | 2     | mA            |       |
|            |  | TC514400J/Z-10 | -    | 2     |               |       |
| $I_{CC3}$  | RAS ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$ Only Mode<br>( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC}$ MIN.)      | TC514400J/Z-80 | -    | 105   | mA            | 3,5   |
|            |  | TC514400J/Z-10 | -    | 90    |               |       |
| $I_{CC4}$  | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode<br>( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{PC}=t_{PC}$ MIN.)          | TC514400J/Z-80 | -    | 70    | mA            | 3,4,5 |
|            |  | TC514400J/Z-10 | -    | 60    |               |       |
| $I_{CC5}$  | STANDBY CURRENT<br>Power Supply Standby Current<br>( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )   | TC514400J/Z-80 | -    | 1     | mA            |       |
|            |  | TC514400J/Z-10 | -    | 1     |               |       |
| $I_{CC6}$  | CAS BEFORE RAS REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$ Before<br>RAS Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.) | TC514400J/Z-80 | -    | 105   | mA            | 3     |
|            |  | TC514400J/Z-10 | -    | 90    |               |       |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input<br>( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test=0V)  | TC514400J/Z-80 | -10  | 10    | $\mu\text{A}$ |       |
|            |  | TC514400J/Z-10 | -10  | 10    |               |       |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq 5.5V$ )   | TC514400J/Z-80 | -10  | 10    | $\mu\text{A}$ |       |
|            |  | TC514400J/Z-10 | -10  | 10    |               |       |
| $V_{OH}$   | OUTPUT LEVEL<br>Output "H" Level Voltage ( $I_{OUT}=-5\text{mA}$ )   | TC514400J/Z-80 | 2.4  | -     | V             |       |
|            |  | TC514400J/Z-10 | 2.4  | -     |               |       |
| $V_{OL}$   | OUTPUT LEVEL<br>Output "L" Level Voltage ( $I_{OUT}=4.2\text{mA}$ )  | TC514400J/Z-80 | -    | 0.4   | V             |       |
|            |  | TC514400J/Z-10 | -    | 0.4   |               |       |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 6, 7, 8)

| SYMBOL     | PARAMETER  | TC514400J/Z<br>-80 |         | TC514400J/Z<br>-10 |         | UNIT | NOTES   |
|------------|--|--------------------|---------|--------------------|---------|------|---------|
|            |  | MIN.               | MAX.    | MIN.               | MAX.    |      |         |
| $t_{RC}$   | Random Read or Write Cycle Time                          | 150                | -       | 180                | -       | ns   |         |
| $t_{RMW}$  | Read-Modify-Write Cycle Time                             | 205                | -       | 245                | -       | ns   |         |
| $t_{PC}$   | Fast Page Mode Cycle Time                                | 50                 | -       | 60                 | -       | ns   |         |
| $t_{PRMW}$ | Fast Page Mode Read-Modify-Write Cycle Time              | 105                | -       | 125                | -       | ns   |         |
| $t_{RAC}$  | Access Time from $\overline{RAS}$                        | -                  | 80      | -                  | 100     | ns   | 9,14,15 |
| $t_{CAC}$  | Access Time from $\overline{CAS}$                        | -                  | 20      | -                  | 25      | ns   | 9,14    |
| $t_{AA}$   | Access Time from Column Address                          | -                  | 40      | -                  | 50      | ns   | 9,15    |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge              | -                  | 45      | -                  | 55      | ns   | 9       |
| $t_{CLZ}$  | $\overline{CAS}$ to Output in Low-Z                      | 0                  | -       | 0                  | -       | ns   | 9       |
| $t_{OFF}$  | Output Buffer Turn-off Delay                             | 0                  | 20      | 0                  | 20      | ns   | 10      |
| $t_T$      | Transition Time (Rise and Fall)                          | 3                  | 50      | 3                  | 50      | ns   | 8       |
| $t_{RP}$   | $\overline{RAS}$ Precharge Time                          | 60                 | -       | 70                 | -       | ns   |         |
| $t_{RAS}$  | $\overline{RAS}$ Pulse Width                             | 80                 | 10,000  | 100                | 10,000  | ns   |         |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode)            | 80                 | 200,000 | 100                | 200,000 | ns   |         |
| $t_{RSH}$  | $\overline{RAS}$ Hold Time                               | 20                 | -       | 25                 | -       | ns   |         |
| $t_{CSH}$  | $\overline{CAS}$ Hold Time                               | 80                 | -       | 100                | -       | ns   |         |
| $t_{RHCP}$ | $\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time | 45                 | -       | 55                 | -       | ns   |         |
| $t_{CAS}$  | $\overline{CAS}$ Pulse Width                             | 20                 | 10,000  | 25                 | 10,000  | ns   |         |
| $t_{RCD}$  | $\overline{RAS}$ to $\overline{CAS}$ Delay Time          | 20                 | 60      | 25                 | 75      | ns   | 14      |
| $t_{RAD}$  | $\overline{RAS}$ to Column Address Delay Time            | 15                 | 40      | 20                 | 50      | ns   | 15      |
| $t_{CRP}$  | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time      | 5                  | -       | 10                 | -       | ns   |         |
| $t_{CP}$   | $\overline{CAS}$ Precharge Time                          | 10                 | -       | 10                 | -       | ns   |         |
| $t_{ASR}$  | Row Address Set-Up Time                                  | 0                  | -       | 0                  | -       | ns   |         |
| $t_{RAH}$  | Row Address Hold Time                                    | 10                 | -       | 15                 | -       | ns   |         |
| $t_{ASC}$  | Column Address Set-Up Time                               | 0                  | -       | 0                  | -       | ns   |         |
| $t_{CAH}$  | Column Address Hold Time                                 | 15                 | -       | 20                 | -       | ns   |         |
| $t_{AR}$   | Column Address Hold Time referenced to $\overline{RAS}$  | 60                 | -       | 75                 | -       | ns   |         |
| $t_{RAL}$  | Column Address to $\overline{RAS}$ Lead Time             | 40                 | -       | 50                 | -       | ns   |         |
| $t_{RCS}$  | Read Command Set-Up Time                                 | 0                  | -       | 0                  | -       | ns   |         |
| $t_{RCH}$  | Read Command Hold Time                                   | 0                  | -       | 0                  | -       | ns   | 11      |

TC514400J/Z-80  
TC514400J/Z-10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

| SYMBOL            | PARAMETER  | TC514400J/<br>Z-80 |      | TC514400J/<br>Z-10 |      | UNITS | NOTES |
|-------------------|--|--------------------|------|--------------------|------|-------|-------|
|                   |  | MIN.               | MAX. | MIN.               | MAX. |       |       |
| t <sub>RRH</sub>  | Read Command Hold Time referenced to $\overline{\text{RAS}}$   | 0                  | -    | 0                  | -    | ns    | 11    |
| t <sub>WCH</sub>  | Write Command Hold Time  | 15                 | -    | 20                 | -    | ns    |       |
| t <sub>WCR</sub>  | Write Command Hold Time referenced to $\overline{\text{RAS}}$  | 60                 | -    | 75                 | -    | ns    |       |
| t <sub>WP</sub>   | Write Command Pulse Width  | 15                 | -    | 20                 | -    | ns    |       |
| t <sub>RWL</sub>  | Write Command to $\overline{\text{RAS}}$ Lead Time   | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>CWL</sub>  | Write Command to $\overline{\text{CAS}}$ Lead Time   | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>DS</sub>   | Data Set-Up Time   | 0                  | -    | 0                  | -    | ns    | 12    |
| t <sub>DH</sub>   | Data Hold Time   | 15                 | -    | 20                 | -    | ns    | 12    |
| t <sub>DHR</sub>  | Data Hold Time referenced to $\overline{\text{RAS}}$   | 60                 | -    | 75                 | -    | ns    |       |
| t <sub>REF</sub>  | Refresh Period   | -                  | 16   | -                  | 16   | ms    |       |
| t <sub>WCS</sub>  | Write Command Set-Up Time  | 0                  | -    | 0                  | -    | ns    | 13    |
| t <sub>CWD</sub>  | $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time  | 50                 | -    | 60                 | -    | ns    | 13    |
| t <sub>RWD</sub>  | $\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay Time  | 110                | -    | 135                | -    | ns    | 13    |
| t <sub>AWD</sub>  | Column Address to $\overline{\text{WRITE}}$ Delay Time   | 70                 | -    | 85                 | -    | ns    | 13    |
| t <sub>CPWD</sub> | $\overline{\text{CAS}}$ Precharge to $\overline{\text{WRITE}}$ Delay Time<br>(Fast Page Mode)  | 75                 | -    | 90                 | -    | ns    | 13    |
| t <sub>CSR</sub>  | $\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)                                    | 5                  | -    | 5                  | -    | ns    |       |
| t <sub>CHR</sub>  | $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)                                      | 15                 | -    | 20                 | -    | ns    |       |
| t <sub>RPC</sub>  | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time  | 0                  | -    | 0                  | -    | ns    |       |
| t <sub>CPT</sub>  | $\overline{\text{CAS}}$ Precharge Time<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test Cycle)                 | 40                 | -    | 50                 | -    | ns    |       |
| t <sub>ROH</sub>  | $\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$   | 10                 | -    | 20                 | -    | ns    |       |
| t <sub>OEA</sub>  | $\overline{\text{OE}}$ Access Time   | -                  | 20   | -                  | 25   | ns    |       |
| t <sub>OED</sub>  | $\overline{\text{OE}}$ to Data Delay   | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>OEZ</sub>  | Output Buffer Turn Off Delay Time from $\overline{\text{OE}}$  | 0                  | 20   | 0                  | 20   | ns    | 10    |
| t <sub>OEH</sub>  | $\overline{\text{OE}}$ Command Hold Time   | 20                 | -    | 25                 | -    | ns    |       |
| t <sub>WTS</sub>  | Write Command Set-Up Time (Test Mode In)   | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WTH</sub>  | Write Command Hold Time (Test Mode In)   | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WRP</sub>  | $\overline{\text{WRITE}}$ to $\overline{\text{RAS}}$ Precharge Time<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle) | 10                 | -    | 10                 | -    | ns    |       |
| t <sub>WRH</sub>  | $\overline{\text{WRITE}}$ to $\overline{\text{RAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)      | 10                 | -    | 10                 | -    | ns    |       |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

| SYMBOL            | PARAMETER  | TC514400J/Z<br>-80 |         | TC514400J/Z<br>-10 |         | UNIT | NOTES   |
|-------------------|--|--------------------|---------|--------------------|---------|------|---------|
|                   |  | MIN.               | MAX.    | MIN.               | MAX.    |      |         |
| t <sub>RC</sub>   | Random Read or Write Cycle Time  | 155                | -       | 185                | -       | ns   |         |
| t <sub>PC</sub>   | Fast Page Mode Cycle Time  | 55                 | -       | 65                 | -       | ns   |         |
| t <sub>RAC</sub>  | Access Time from $\overline{\text{RAS}}$                               | -                  | 85      | -                  | 105     | ns   | 9,14,15 |
| t <sub>CAC</sub>  | Access Time from $\overline{\text{CAS}}$                               | -                  | 25      | -                  | 30      | ns   | 9,14    |
| t <sub>AA</sub>   | Access Time from Column Address  | -                  | 45      | -                  | 55      | ns   | 9,15    |
| t <sub>CPA</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                     | -                  | 50      | -                  | 60      | ns   | 9       |
| t <sub>RAS</sub>  | $\overline{\text{RAS}}$ Pulse Width                                    | 85                 | 10,000  | 105                | 10,000  | ns   |         |
| t <sub>RASP</sub> | $\overline{\text{RAS}}$ Pulse Width(Fast Page Mode)                    | 85                 | 200,000 | 105                | 200,000 | ns   |         |
| t <sub>RSH</sub>  | $\overline{\text{RAS}}$ Hold Time                                      | 25                 | -       | 30                 | -       | ns   |         |
| t <sub>CSH</sub>  | $\overline{\text{CAS}}$ Hold Time                                      | 85                 | -       | 105                | -       | ns   |         |
| t <sub>RHCP</sub> | $\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time | 50                 | -       | 60                 | -       | ns   |         |
| t <sub>CAS</sub>  | $\overline{\text{CAS}}$ Pulse Width                                    | 25                 | 10,000  | 30                 | 10,000  | ns   |         |
| t <sub>RAL</sub>  | Column Address to $\overline{\text{RAS}}$ Lead Time                    | 45                 | -       | 55                 | -       | ns   |         |

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

| SYMBOL          | PARAMETER  | MIN. | MAX. | UNIT |
|-----------------|--|------|------|------|
| C <sub>I1</sub> | Input Capacitance (A <sub>0</sub> ~A <sub>9</sub> )  | -    | 5    | pF   |
| C <sub>I2</sub> | Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ , $\overline{\text{OE}}$ ) | -    | 7    | pF   |
| C <sub>O</sub>  | Output Capacitance (I/0 <sub>1</sub> ~I/0 <sub>4</sub> )   | -    | 7    | pF   |

# TC514400J/Z-80

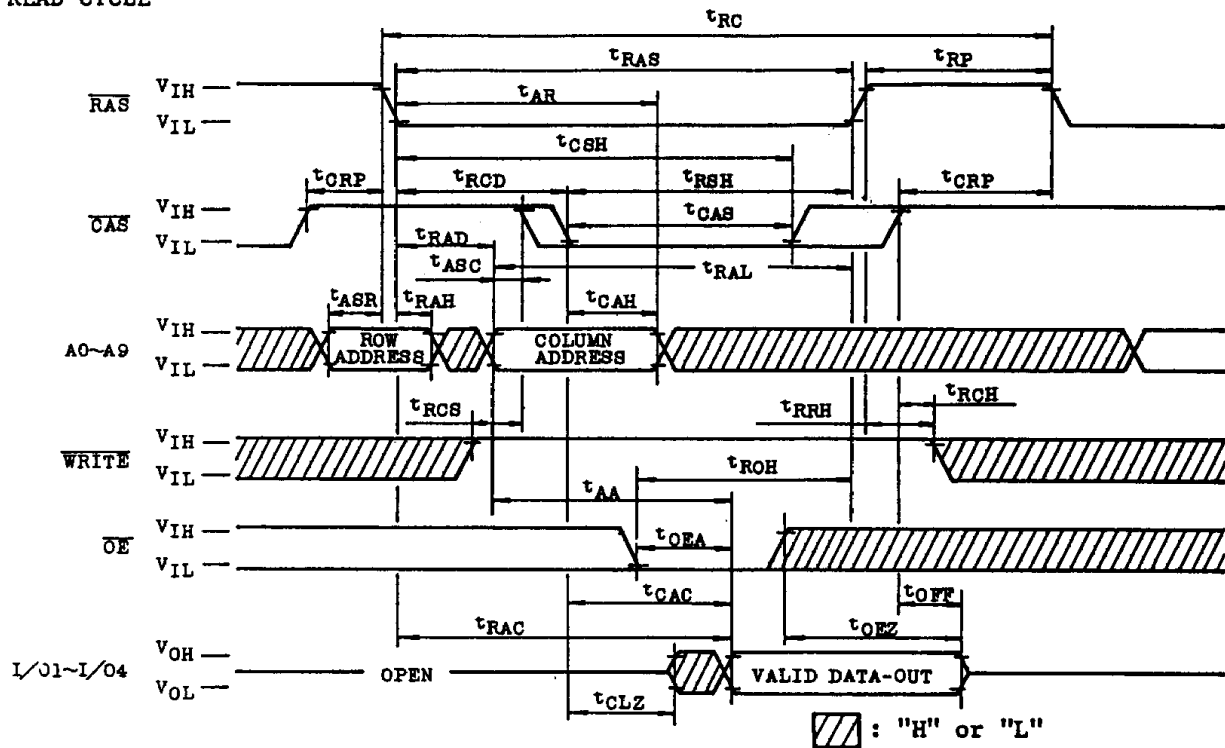
# TC514400J/Z-10

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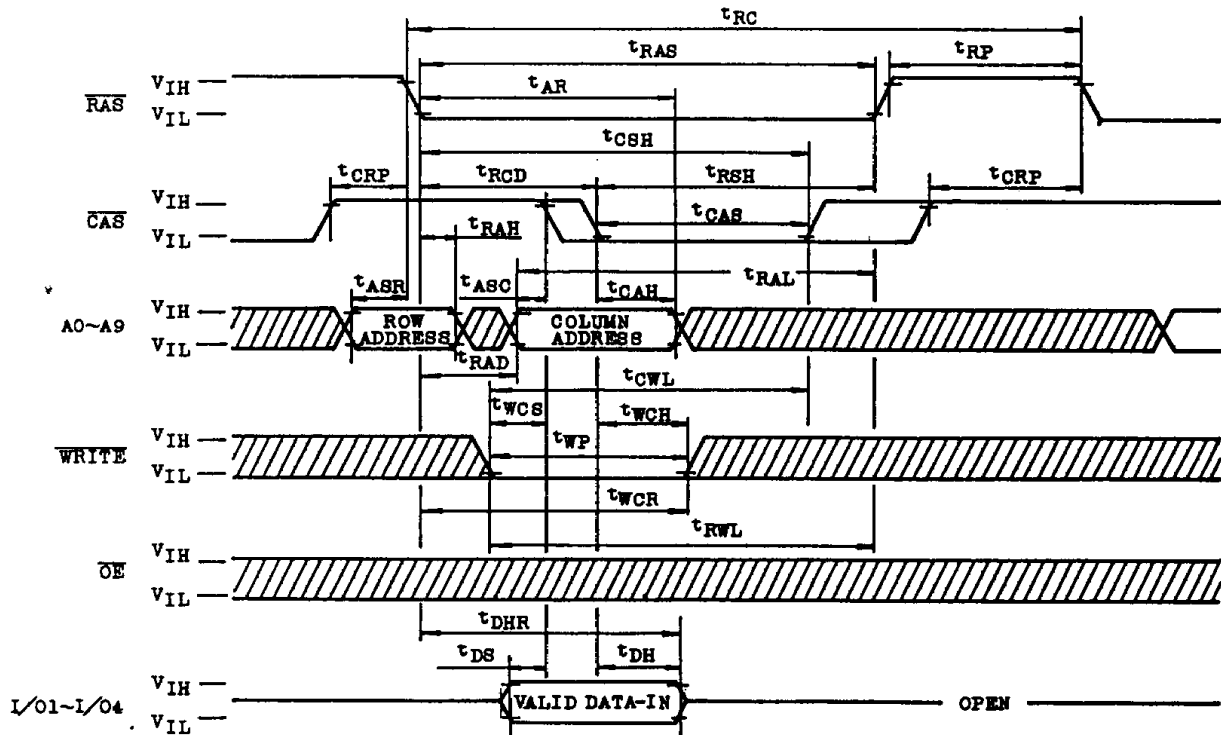
## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while  $\overline{RAS}=V_{IL}$  and  $\overline{CAS}=V_{IH}$ .
6. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles instead of 8  $\overline{RAS}$  only refresh cycles are required.
7. AC measurements assume  $t_f=5$ ns.
8.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10.  $t_{OFF}(\text{max.})$  and  $t_{OEZ}(\text{max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-modify-write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

READ CYCLE

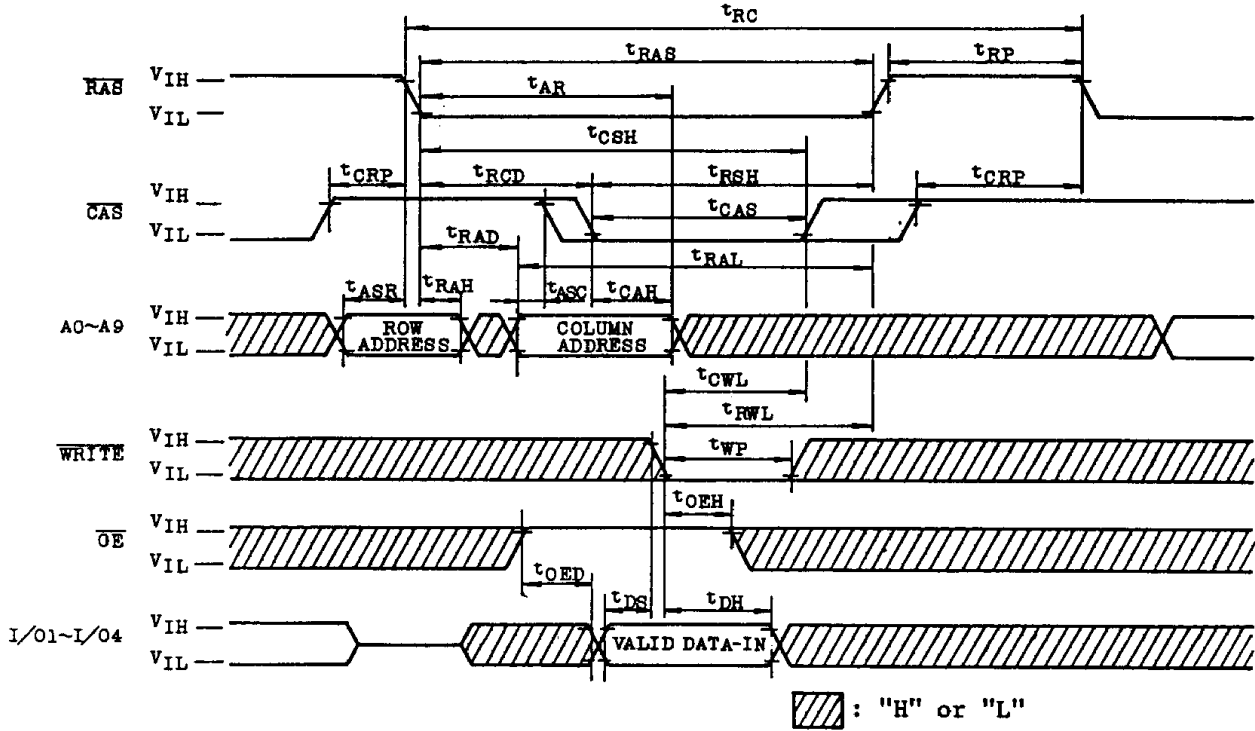


WRITE CYCLE (EARLY WRITE)

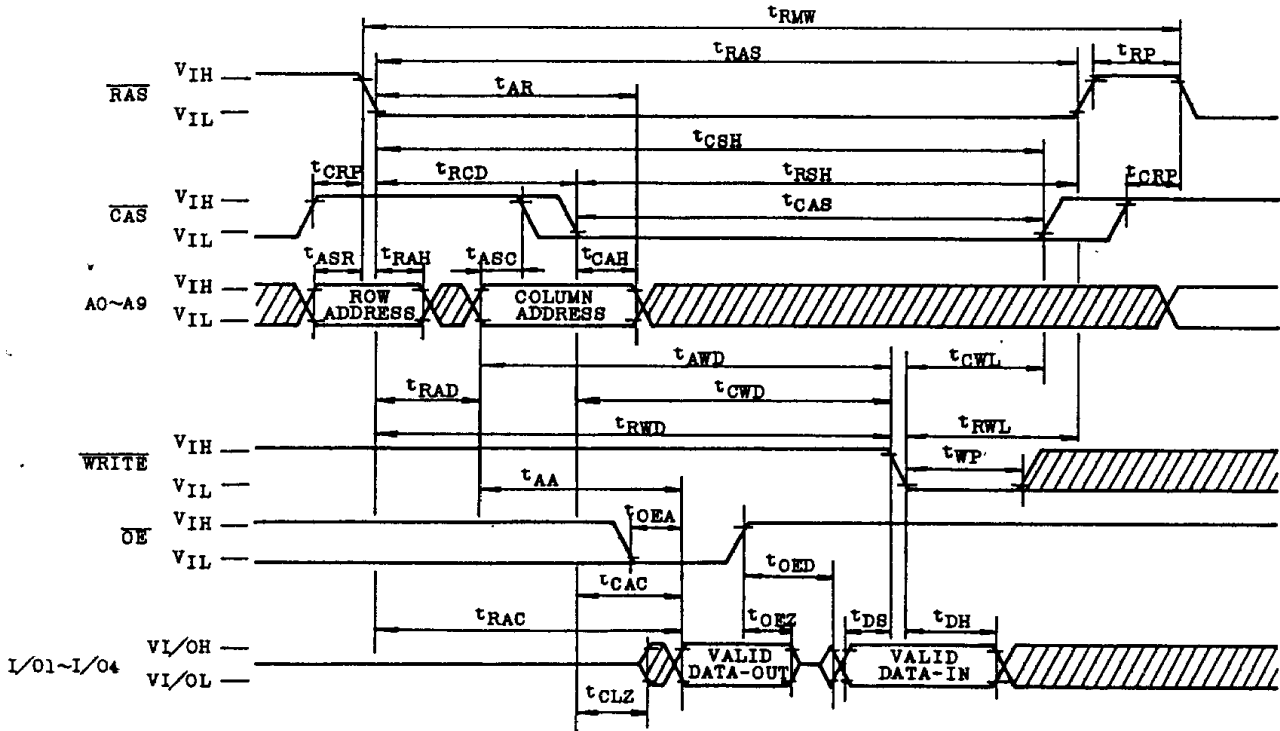


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WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE

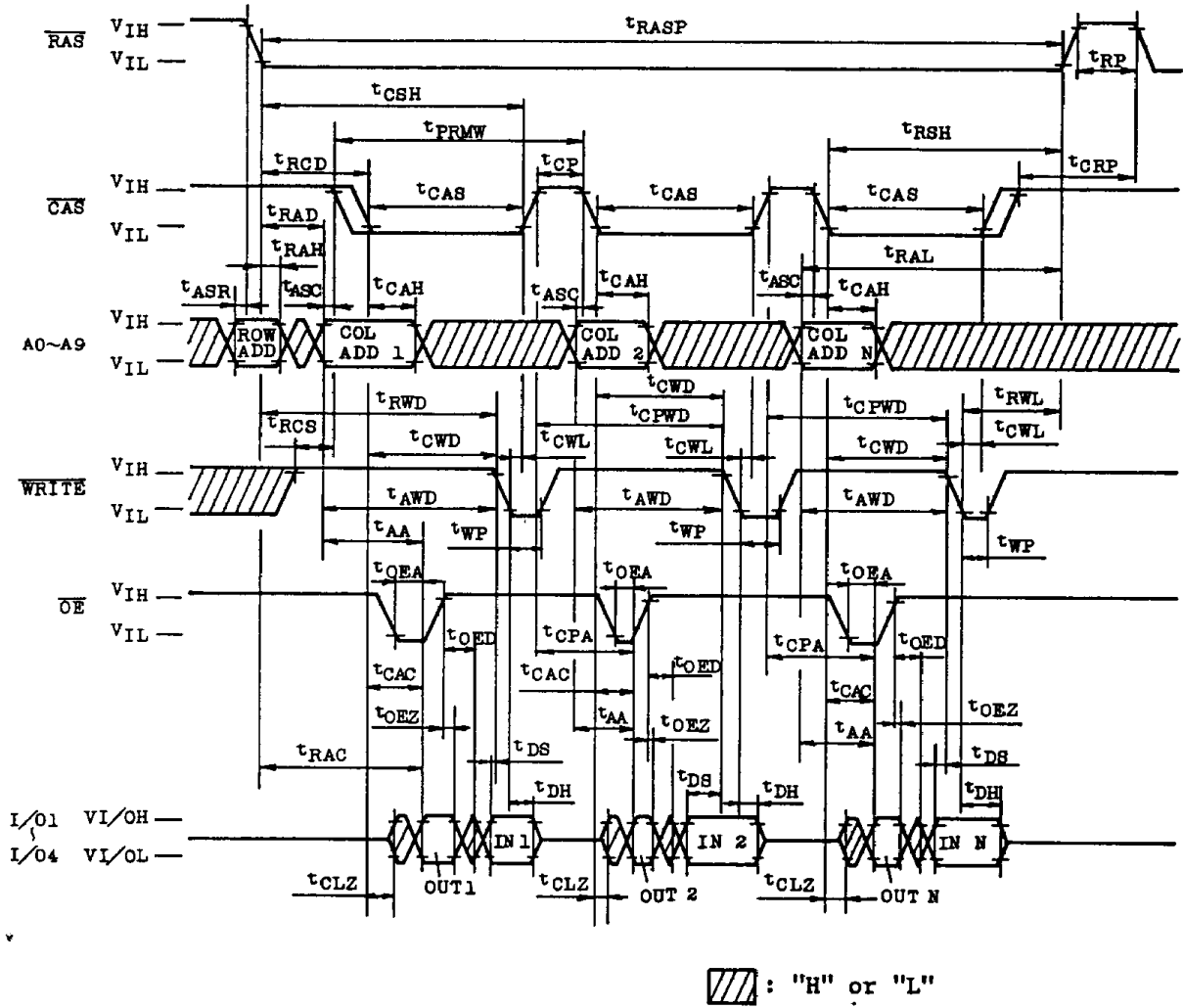




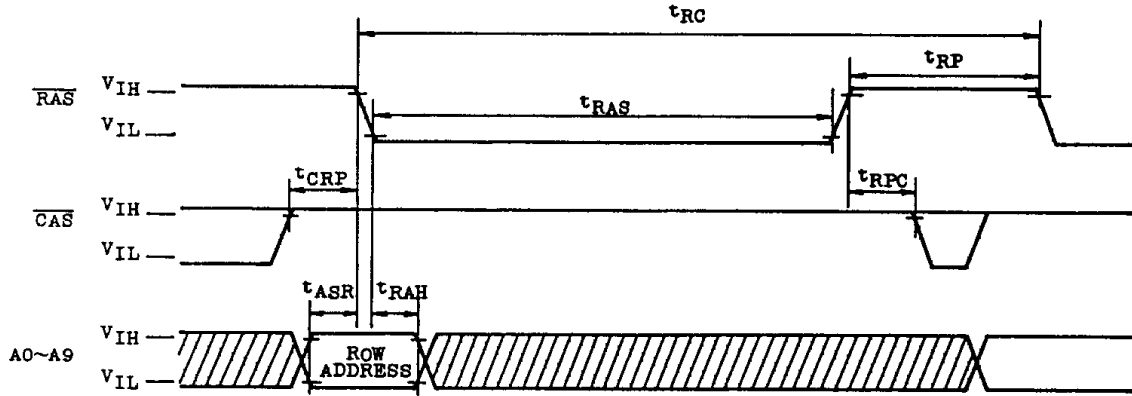


TC514400J/Z-80  
TC514400J/Z-10

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



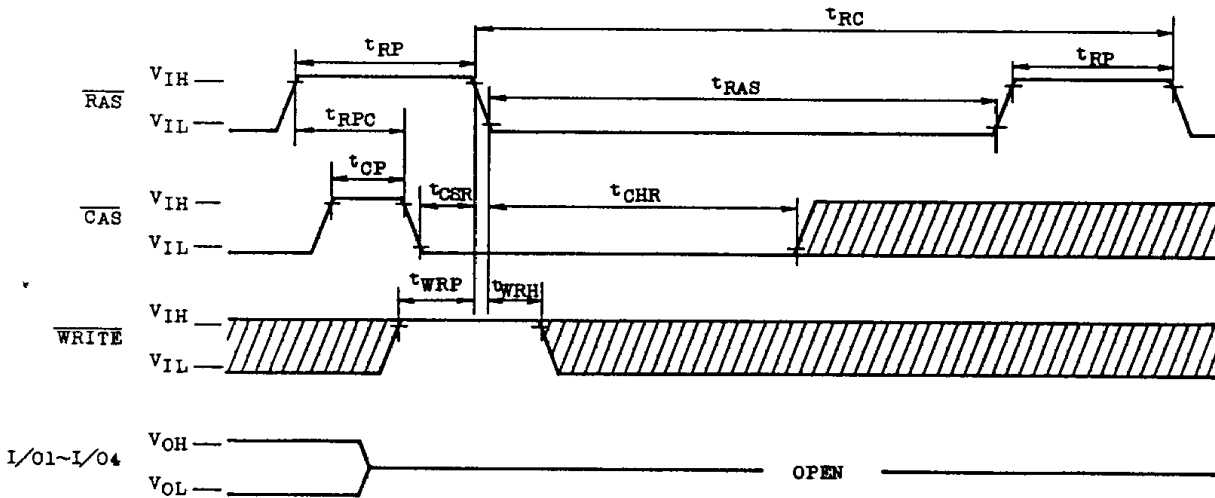
$\overline{\text{RAS}}$  ONLY REFRESH CYCLE



Note:  $\overline{\text{WRITE}}$ ,  $\overline{\text{OE}}$ ="H" or "L"

: "H" or "L"

$\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE

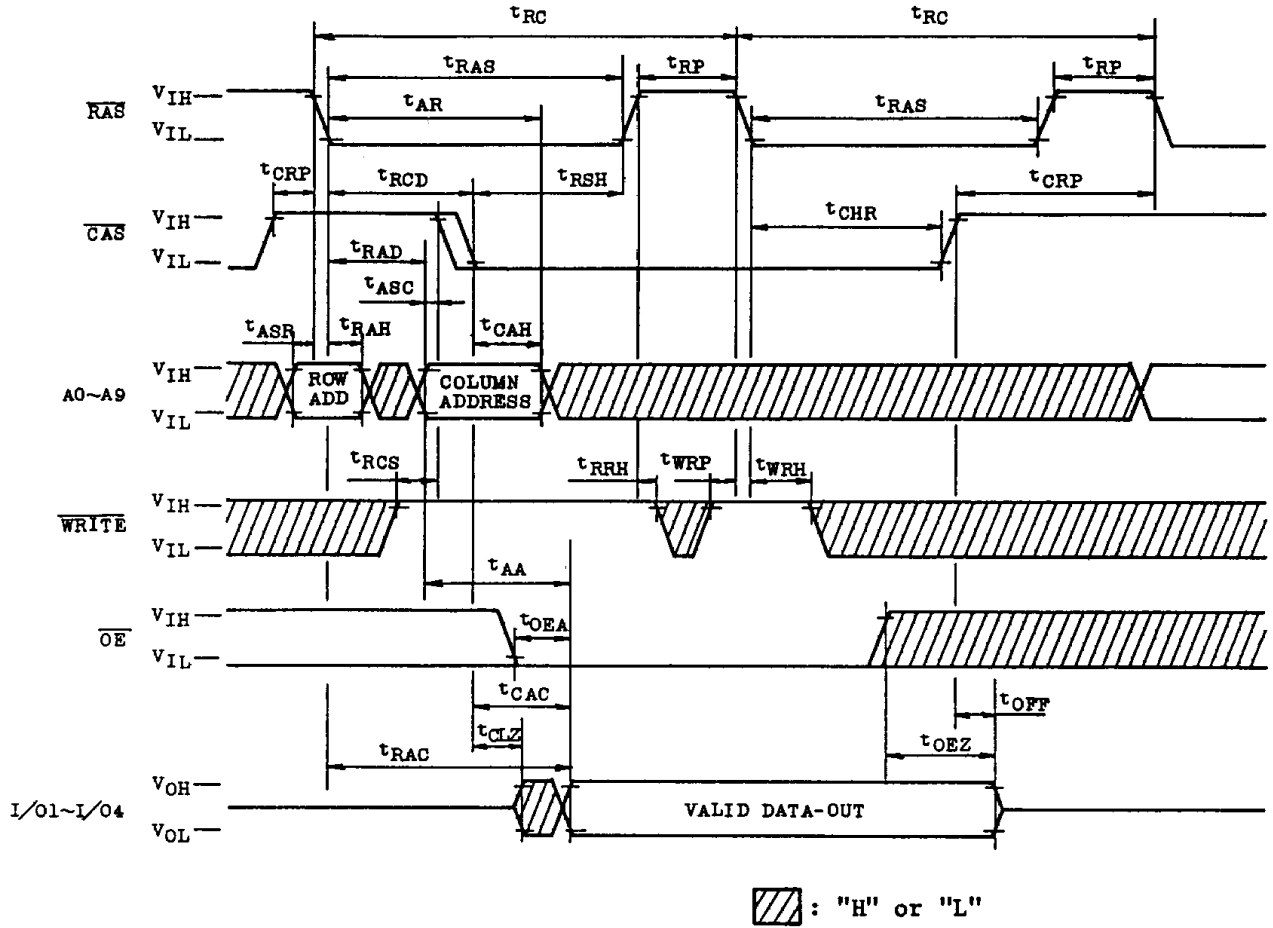


Note:  $\overline{\text{OE}}$ , A0~A9="H" or "L"

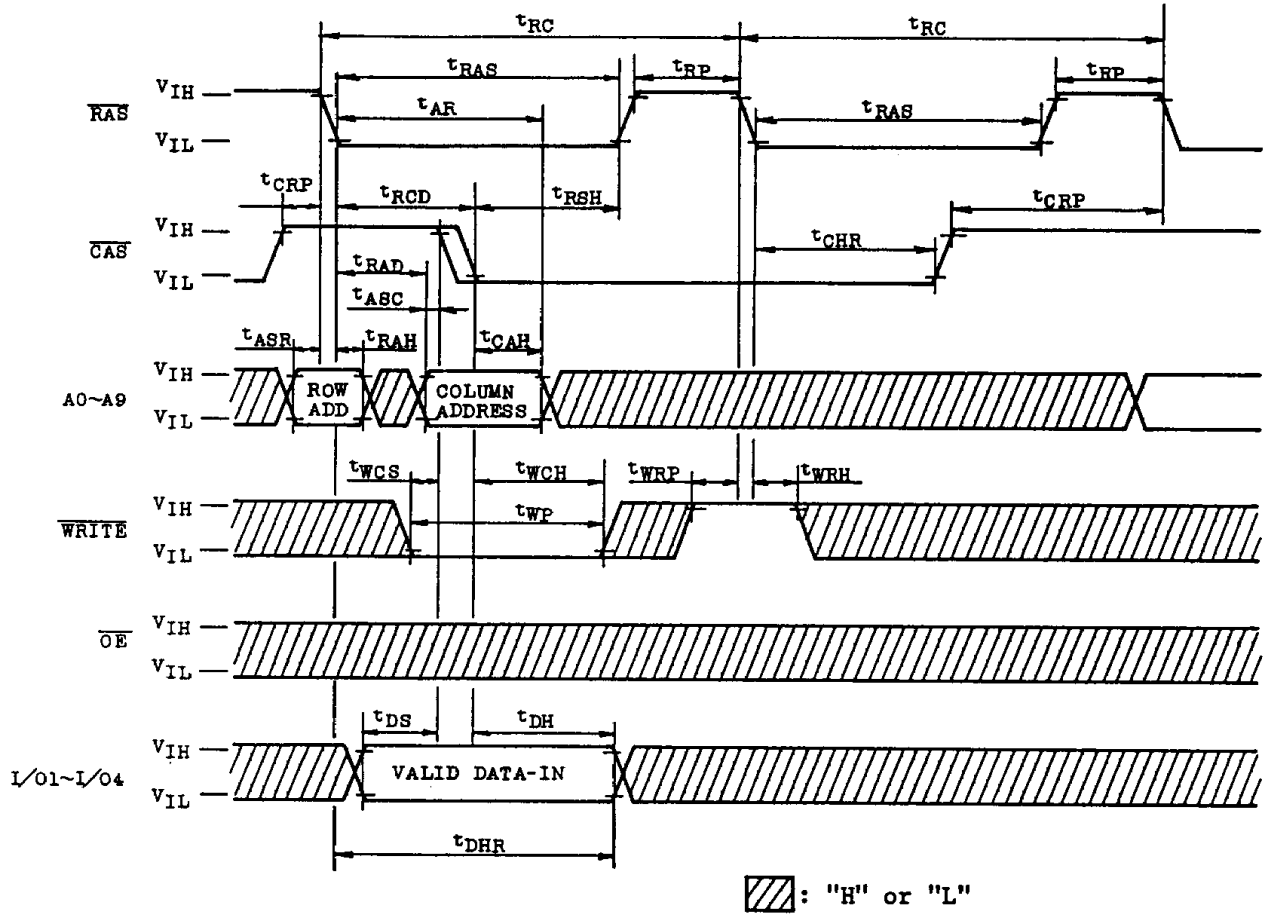
: "H" or "L"

TC514400J/Z-80  
 TC514400J/Z-10

HIDDEN REFRESH CYCLE (READ)

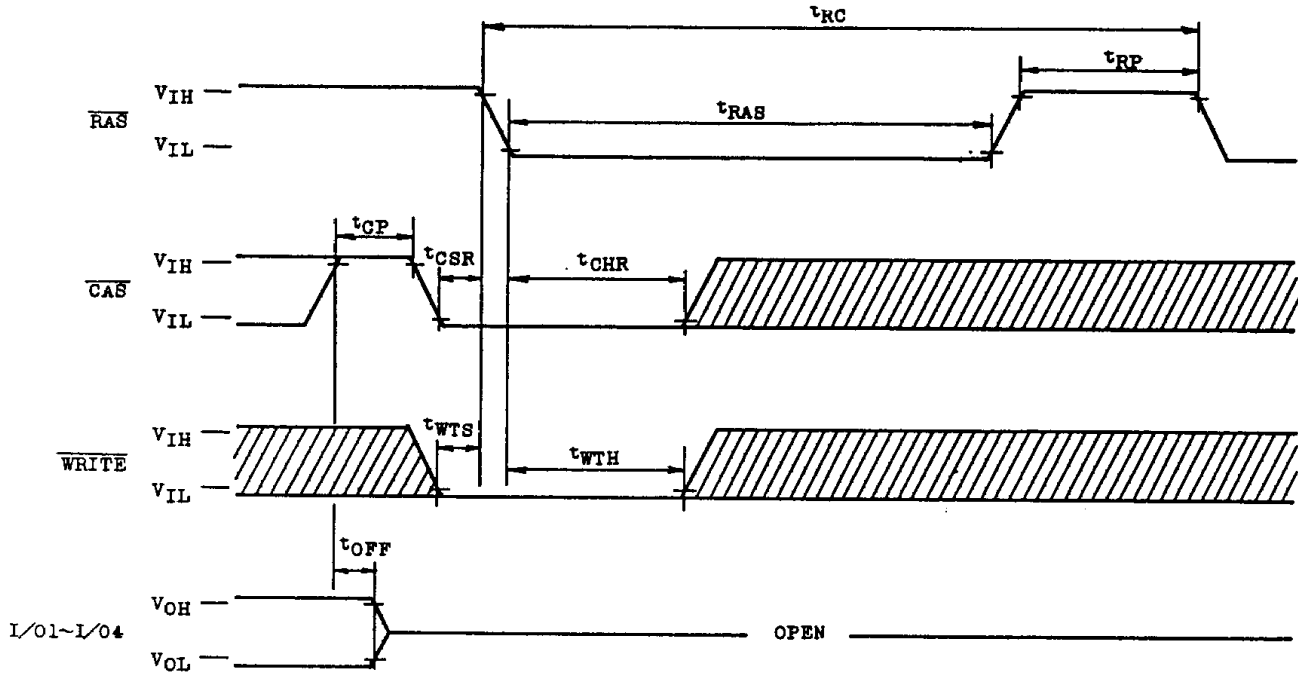


HIDDEN REFRESH CYCLE (WRITE)






WRITE,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE

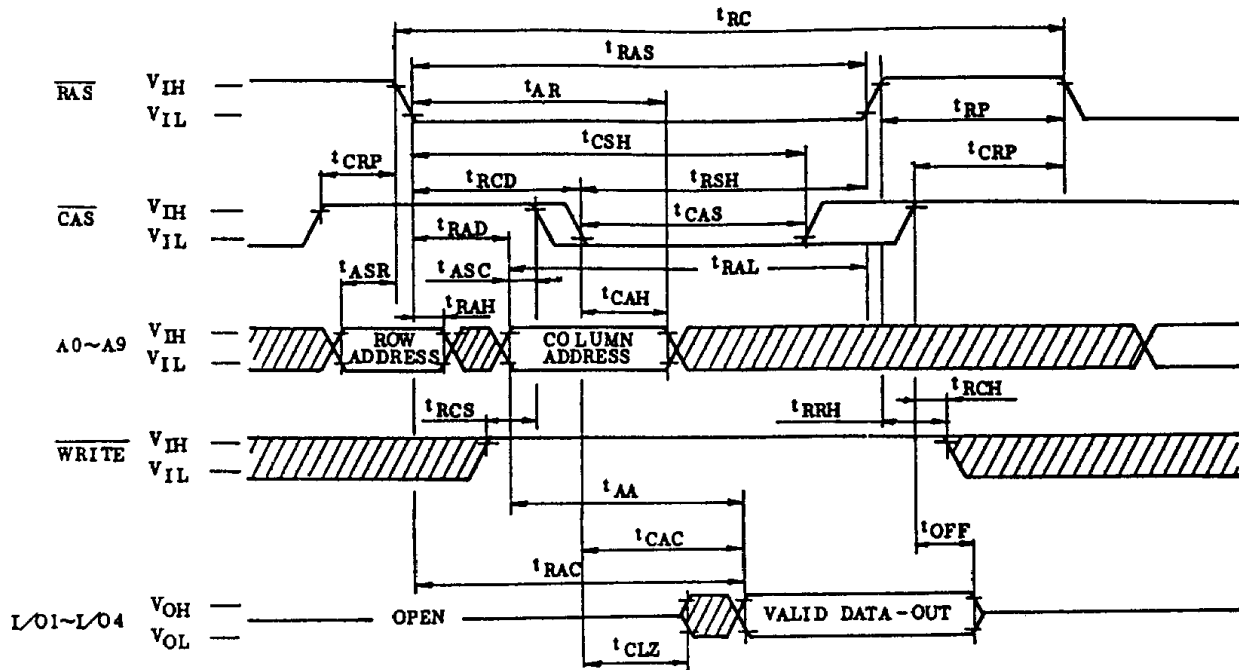


$\overline{\text{OE}}$ , A0~A9: "H" or "L"

 : "H" or "L"

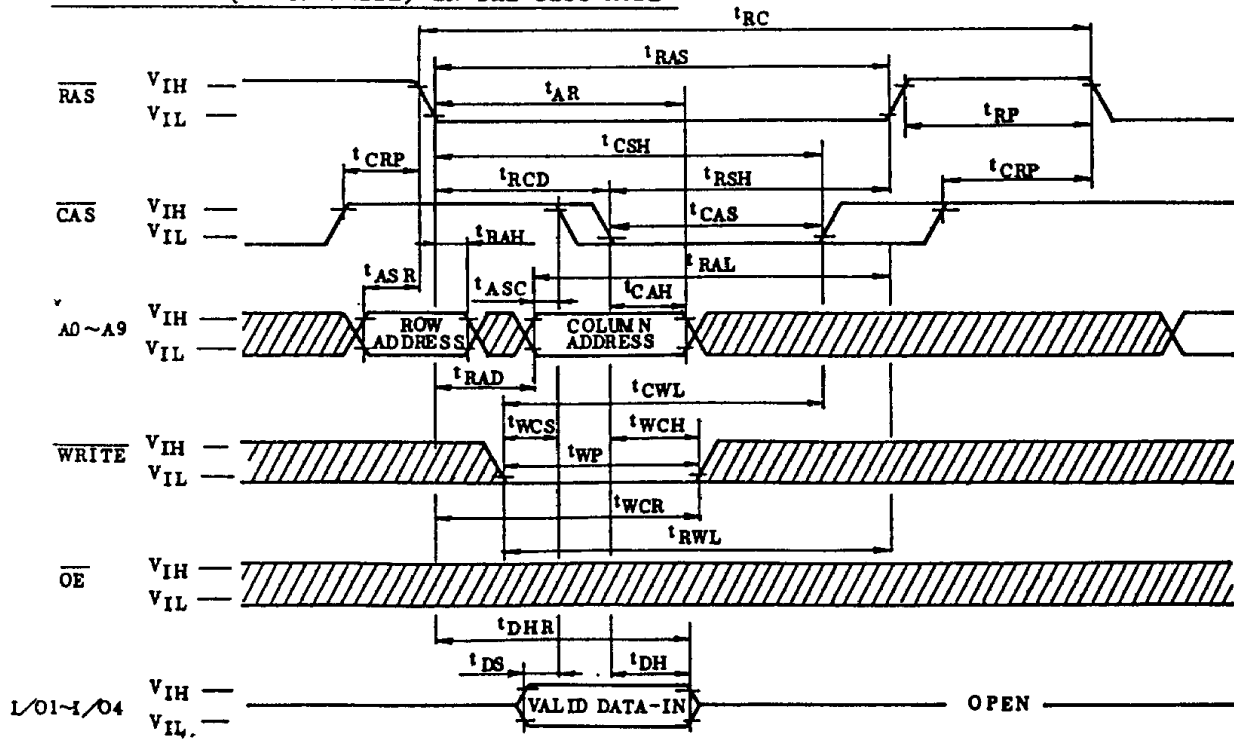
# TC514400J/Z-80 TC514400J/Z-10

## READ CYCLE IN THE TEST MODE



Note:  $\overline{OE}$  = "L"    : "H" or "L"

## WRITE CYCLE (EARLY WRITE) IN THE TEST MODE







# TC514400J/Z-80

## TC514400J/Z-10

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### TEST MODE

The TC514400J/Z is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Aoc is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400J/Z. In "Test Mode", the 1M $\times$ 4 DRAM can be tested as if it were a 512K $\times$ 4 DRAM.

" $\overline{\text{WRITE}}$ ,  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" puts the device into "Test Mode". And " $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" or " $\overline{\text{RAS}}$  Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{WRITE}}$ ,  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

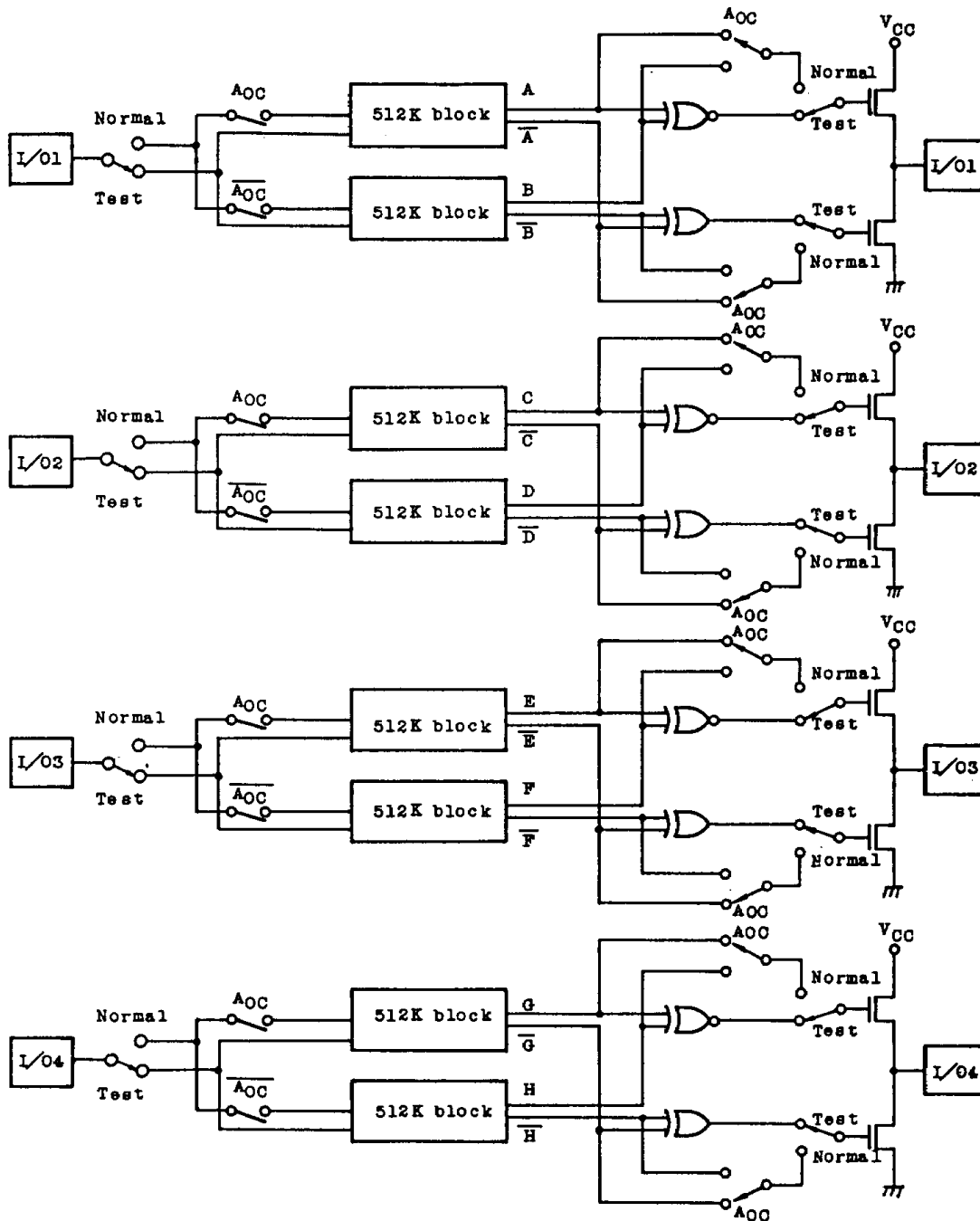


Fig. 1