

**TOSHIBA**

# TC518128AP/ASP/AF/AFW-80/10/12 TC518128APL/ASPL/AFL/AFWL-80/10/12 TC518128AFTL-80/10/12

**SILICON GATE CMOS****131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM****Description**

The TC518128A is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128A utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128A operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518128A features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

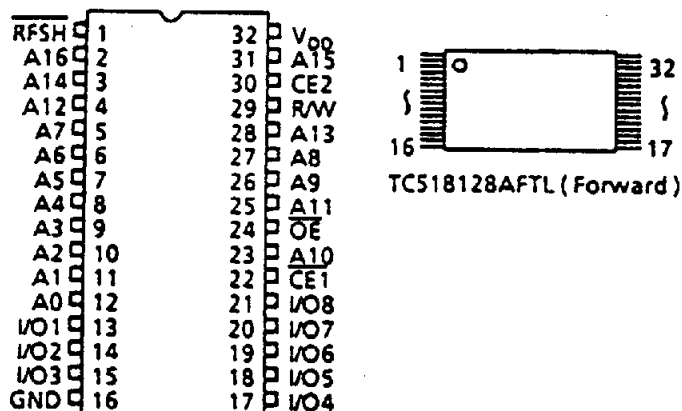
The TC518128A is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

**Features**

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518128A Family		
	-80	-10	-12
$t_{CEA}$ CE Access Time	80ns	100ns	120ns
$t_{OEA}$ $\overline{OE}$ Access Time	35ns	40ns	50ns
$t_{RC}$ Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200 $\mu$ A (L version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
  - TC518128AP/APL : DIP32-P-600
  - TC518128AF/AFL : SOP32-P-450
  - TC518128ASP/ASPL : DIP32-P-300
  - TC518128AFW/AFWL : SOP32-P-525
  - TC518128AFTL : TSOP32-P-0820

**Pin Connection (Top View)****Pin Names**

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
RFSH	Refresh Input
$\overline{CE1}$ , CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$V_{DD}$	Power
GND	Ground

**(TSOP)**

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	CE2	A <sub>15</sub>	$V_{DD}$	RFSH	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A <sub>10</sub>	$\overline{OE}$



### DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	–	V <sub>DD</sub> + 1.0	V	
V <sub>IL</sub>	Input Low Voltage	-1.0	–	0.8	V	

### DC Characteristics (T<sub>a</sub> = 0 ~ 70°C, V<sub>DD</sub> = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I <sub>DDO</sub>	Operating Current (Average) CE1, CE2, Address cycling: t <sub>RC</sub> = t <sub>RC</sub> min.	80ns version	–	50	70	mA 3,4
		100ns version	–	40	60	
		120ns version	–	35	50	
I <sub>DDS1</sub>	Standby Current CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> , RFSH = V <sub>IH</sub>	Normal version	–	–	2	mA
		L version	–	–	1	
I <sub>DDS2</sub>	Standby Current CE1 = V <sub>DD</sub> - 0.2V or CE2 = 0.2V, RFSH = V <sub>DD</sub> - 0.2V	Normal version	–	–	1	mA
		L version	–	100	200	
I <sub>DDF1</sub>	Self Refresh Current (Average) CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> , RFSH = V <sub>IL</sub>	Normal version	–	–	2	mA
		L version	–	–	1	
I <sub>DDF2</sub>	Self Refresh Current (Average) CE1 = V <sub>DD</sub> - 0.2V or CE2 = 0.2V, RFSH = 0.2V	Normal version	–	–	1	mA
		L version	–	100	200	
I <sub>DDF3</sub>	Auto Refresh Current (Average) RFSH cycling: t <sub>FC</sub> = t <sub>FC</sub> min	–	–	2	mA	
I <sub>DDF4</sub>	CE only Refresh Current (Average) CE1, CE2, Address cycling: t <sub>RC</sub> = t <sub>RC</sub> min.	80ns version	–	50	70	mA 3
		100ns version	–	40	60	
		120ns version	–	35	50	
I <sub>I(L)</sub>	Input Leakage Current 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> , All other inputs not under test = 0V	–	–	±10	μA	
I <sub>O(L)</sub>	Output Leakage Current Output Disabled (CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE = V <sub>IH</sub> or R/W = V <sub>IL</sub> ), 0V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>	–	–	±10	μA	
V <sub>OH</sub>	Output High Level I <sub>OH</sub> = -5mA	2.4	–	–	V	
V <sub>OL</sub>	Output Low Level I <sub>OL</sub> = 4.2mA	–	–	0.4	V	

Note: For I<sub>DDS1</sub> and I<sub>DDF1</sub> with CE1 = V<sub>IH</sub> (CE2 = V<sub>IL</sub>), the specified limits are guaranteed under the condition CE2 = V<sub>IH</sub> or CE2 = V<sub>IL</sub> (CE1 = V<sub>IH</sub> or CE1 = V<sub>IL</sub>).  
For I<sub>DDS2</sub> and I<sub>DDF2</sub> with CE1 ≥ V<sub>DD</sub> - 0.2V (CE2 ≤ 0.2V), the specified limits are guaranteed under the condition CE2 ≥ V<sub>DD</sub> - 0.2V or CE2 ≤ 0.2V (CE1 ≥ V<sub>DD</sub> - 0.2V or CE1 ≤ 0.2V).

### Capacitance\* (V<sub>DD</sub> = 5V, T<sub>a</sub> = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C <sub>I1</sub>	Input Capacitance (A0 ~ A16)	–	5	pF
C <sub>I2</sub>	Input Capacitance (CE1, CE2, OE, R/W, RFSH)	–	7	
C <sub>IO</sub>	Input/Output Capacitance	–	7	

\*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V<sub>DD</sub> = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t <sub>RMW</sub>	Read Modify Write Cycle Time	195	–	235	–	280	–		
t <sub>CE</sub>	CE Pulse Width	80	10,000	100	10,000	120	10,000		13
t <sub>p</sub>	CE Precharge Time	40	–	50	–	60	–		
t <sub>CEA</sub>	CE Access Time	–	80	–	100	–	120		
t <sub>OEA</sub>	$\overline{OE}$ Access Time	–	35	–	40	–	50		
t <sub>CLZ</sub>	CE to Output in Low -Z	30	–	30	–	30	–		
t <sub>OLZ</sub>	$\overline{OE}$ to Output in Low -Z	0	–	0	–	0	–		
t <sub>WLZ</sub>	Output Active from End of Write	0	–	0	–	0	–		
t <sub>CHZ</sub>	Chip Disable to Output in High-Z	0	25	0	30	0	35		9
t <sub>OHZ</sub>	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35		9
t <sub>WHZ</sub>	Write Enable to Output in High-Z	0	25	0	30	0	35		9
t <sub>ODS</sub>	$\overline{OE}$ Output Disable Setup Time	0	–	0	–	0	–		
t <sub>ODH</sub>	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–		
t <sub>RCS</sub>	Read Command Setup Time	0	–	0	–	0	–		
t <sub>RCH</sub>	Read Command Hold Time	0	–	0	–	0	–		
t <sub>WP</sub>	Write Pulse Width	60	–	70	–	85	–		
t <sub>WCH</sub>	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t <sub>CWL</sub>	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000		
t <sub>DSW</sub>	Data Setup Time from R/W	30	–	35	–	45	–		10
t <sub>OSC</sub>	Data Setup Time from CE	30	–	35	–	45	–		10
t <sub>DHW</sub>	Data Hold Time from R/W	0	–	0	–	0	–		10
t <sub>DHC</sub>	Data Hold Time from CE	0	–	0	–	0	–		10
t <sub>ASC</sub>	Address Setup Time	0	–	0	–	0	–		11
t <sub>AHC</sub>	Address Hold Time	20	–	25	–	30	–		11
t <sub>RHC</sub>	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–		
t <sub>FC</sub>	Auto Refresh Cycle Time	130	–	160	–	190	–		
t <sub>RFD</sub>	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–		
t <sub>FAP</sub>	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t <sub>FP</sub>	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	12	
t <sub>FAS</sub>	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	12	
t <sub>FRS</sub>	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	12	
t <sub>REF</sub>	Refresh Period (512 cycles, A0 ~ A8)	–	8	–	8	–	8	ms	
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t <sub>CES</sub>	CE2 Low Setup Time	5	–	5	–	5	–	ns	14
t <sub>CEH</sub>	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

## Notes:

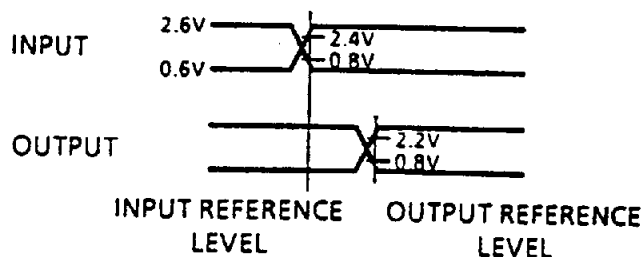
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3)  $I_{DDO}$  and  $I_{DDF4}$  depend on the cycle time.
- 4)  $I_{DDO}$  depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 $\mu$ s with high  $\overline{CE1}$  or low CE2 is required after power-up before proper device operation is achieved.
- 6) AC measurements assume  $t_f = 5$ ns.

## 7) Timing reference levels

Input Levels :  $V_{IH} = 2.6$ V  
                  :  $V_{IL} = 0.6$ V

Input Reference Levels :  $V_{IH} = 2.4$ V  
                              :  $V_{IL} = 0.8$ V

Output Reference Levels :  $V_{OH} = 2.2$ V  
                              :  $V_{OL} = 0.8$ V



- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of  $\overline{RW}$  or  $\overline{CE1}$  rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time ( $t_{DSW}$  or  $t_{DSC}$ ) and hold time ( $t_{DHW}$  or  $t_{DHC}$ ).
- 11) All address inputs are latched at the falling edge of  $\overline{CE1}$  (rising edge of CE2). Therefore, all the address inputs must be valid during  $t_{ASC}$  and  $t_{AHC}$ .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the  $\overline{RFSH}$  pulse width under the condition  $CE1 = V_{IH}$  or  $CE2 = V_{IL}$ .
  - Auto refresh :  $\overline{RFSH}$  pulse width  $\leq t_{FAP}$  (max.)
  - Self refresh :  $\overline{RFSH}$  pulse width  $\geq t_{FAS}$  (min.)

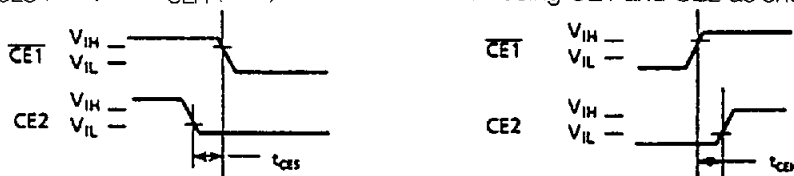
The timing parameter  $t_{FRS}$  must be met for proper device operation under the following conditions:

- after self refresh
- if  $\overline{RFSH} = "L"$  after power-up

- 13) The timings,  $t_{CE}$  (min.) and  $t_{CE}$  (max.) must be met for proper device operation.

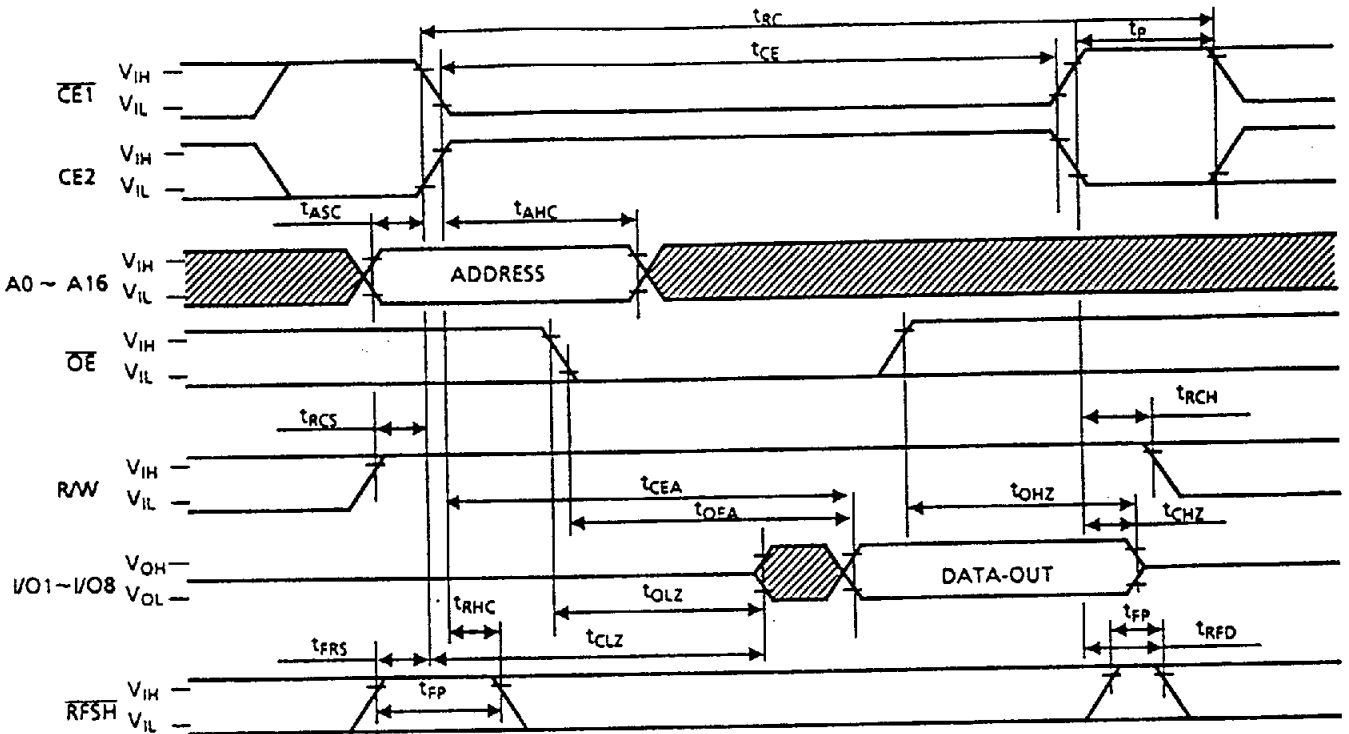
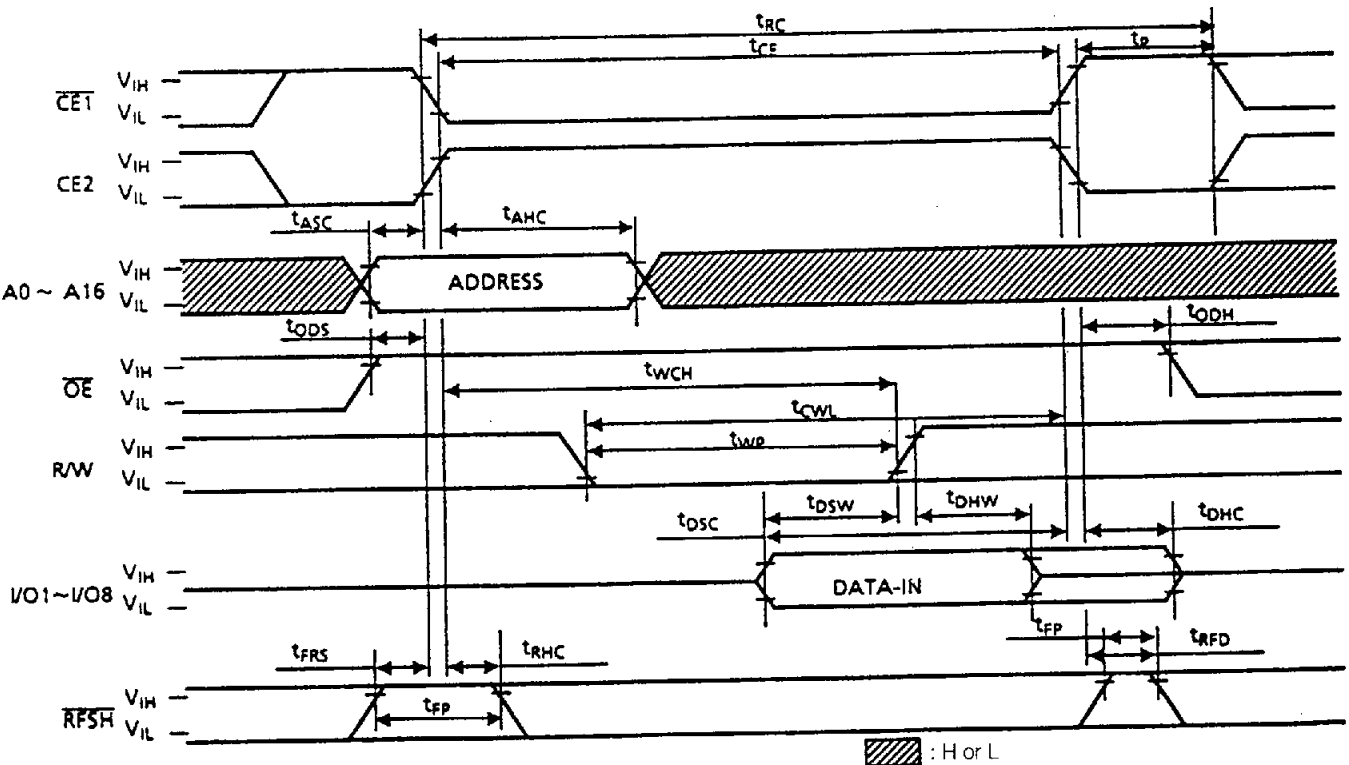


- 14) The timings,  $t_{CES}$  (min.) and  $t_{CEH}$  (min.) must be met when using  $\overline{CE1}$  and CE2 as shown below.



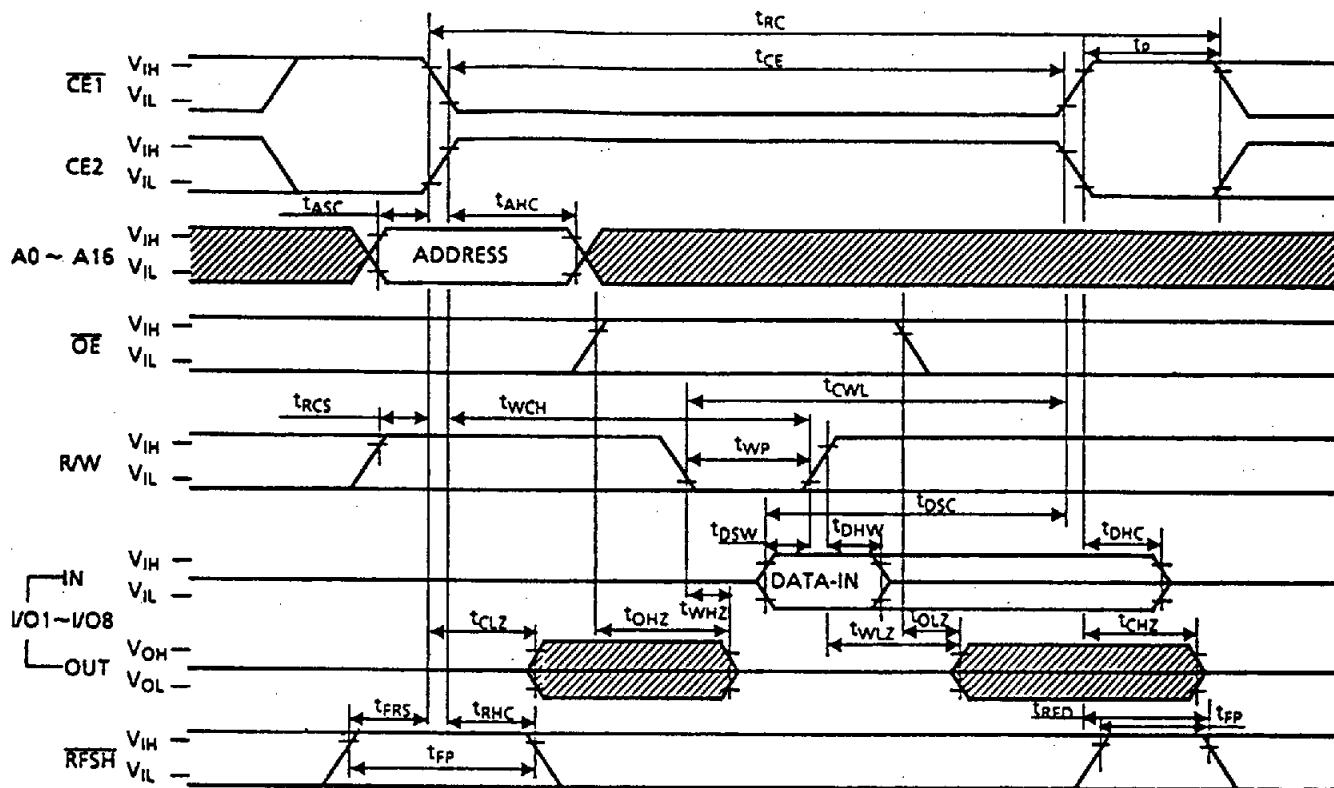
## Timing Waveforms

## Read Cycle

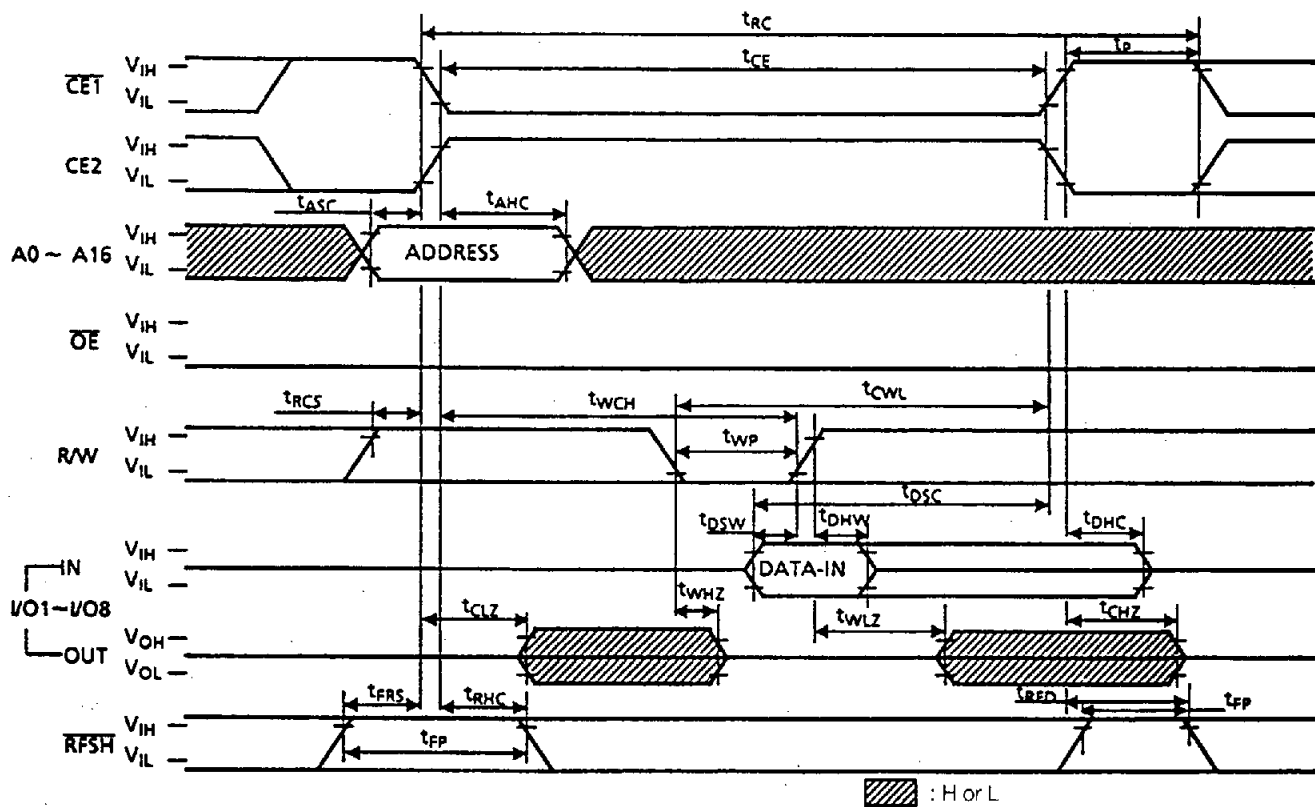
Write Cycle 1 ( $\overline{OE}$  Fixed High)

Note: The device can be operated by cycling  $\overline{CE1}$  (or  $CE2$ ) only provided that  $CE2$  (or  $\overline{CE1}$ ) is connected to  $V_{IH}$  (or  $V_{IL}$ ).

Write Cycle 2 ( $\overline{OE}$  Clocked)



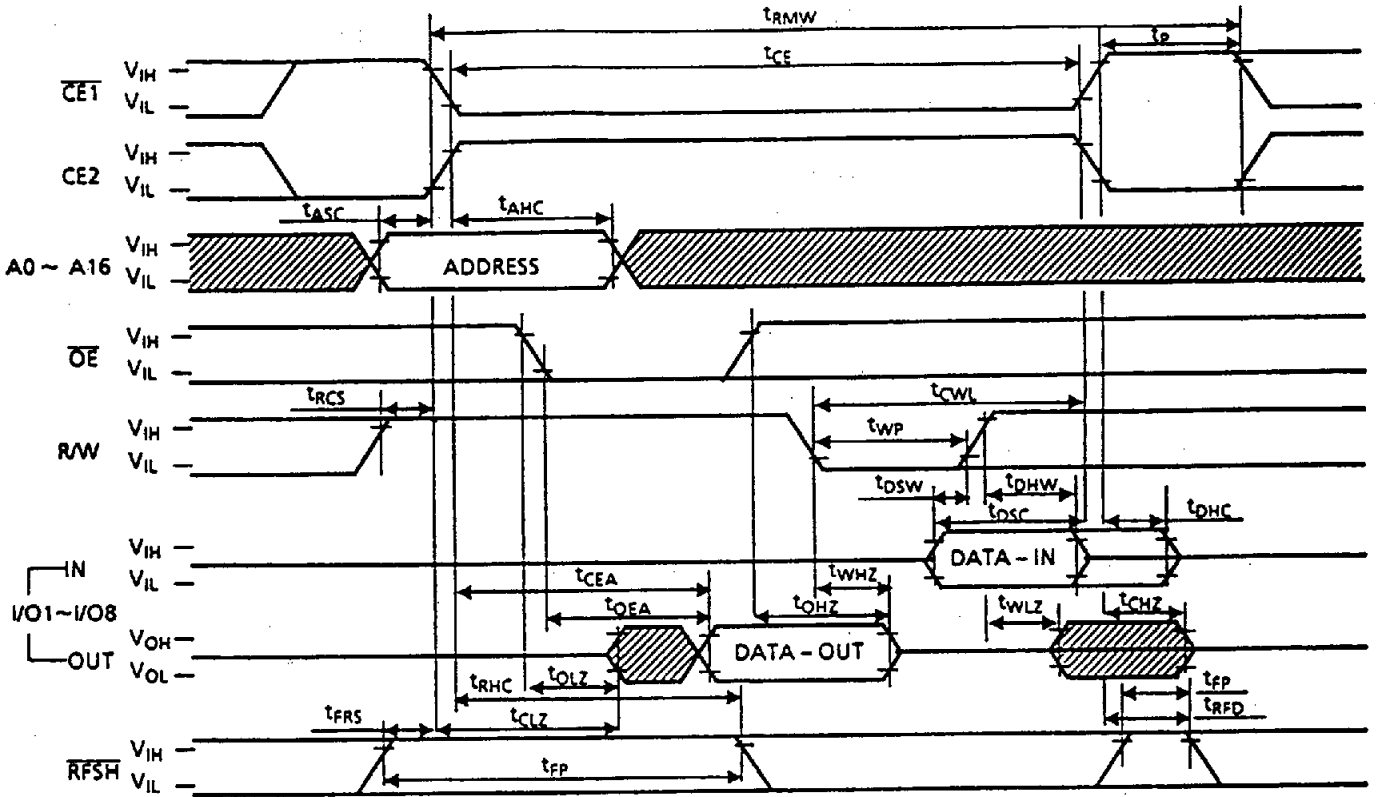
Write Cycle 3 ( $\overline{OE}$  Fixed Low)



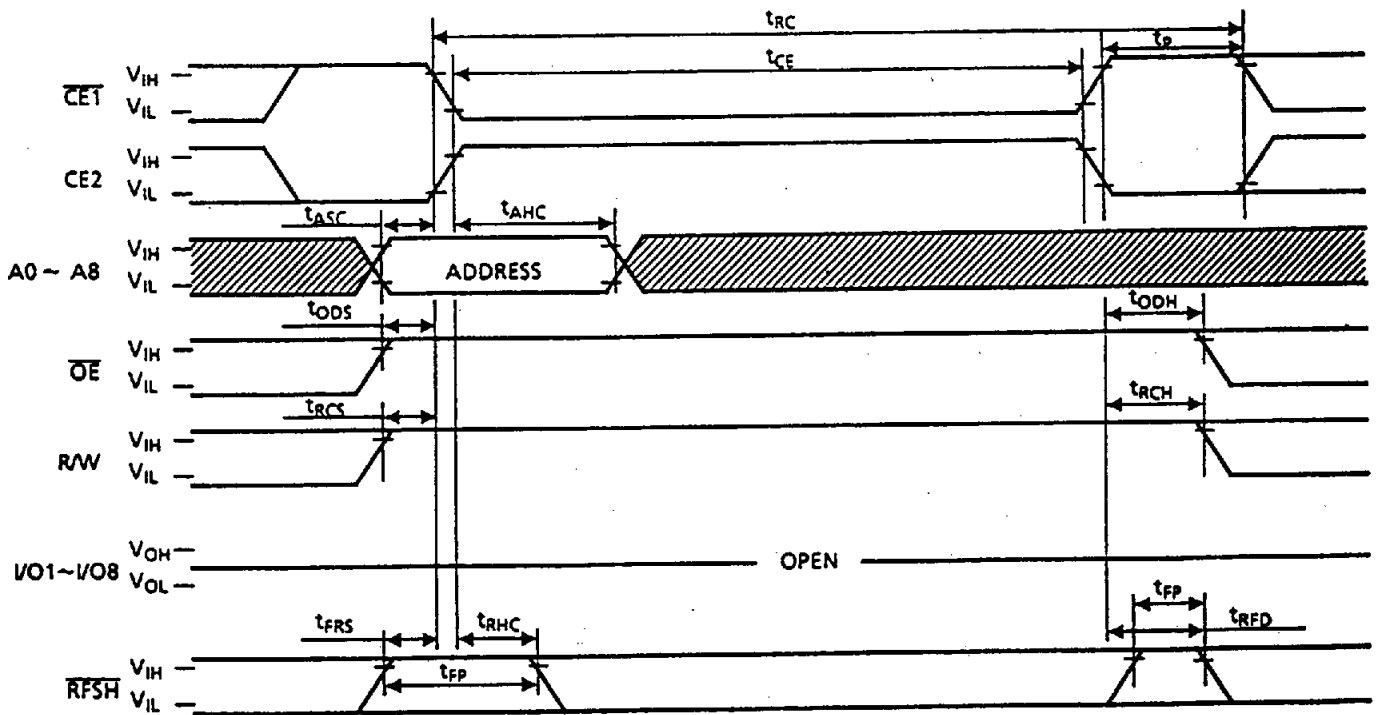
▨ : H or L

Note: The device can be operated by cycling  $\overline{CE1}$  (or  $\overline{CE2}$ ) only provided that  $\overline{CE2}$  (or  $\overline{CE1}$ ) is connected to  $V_{IH}$  (or  $V_{IL}$ ).

Read Modify Write Cycle



CE Only Refresh



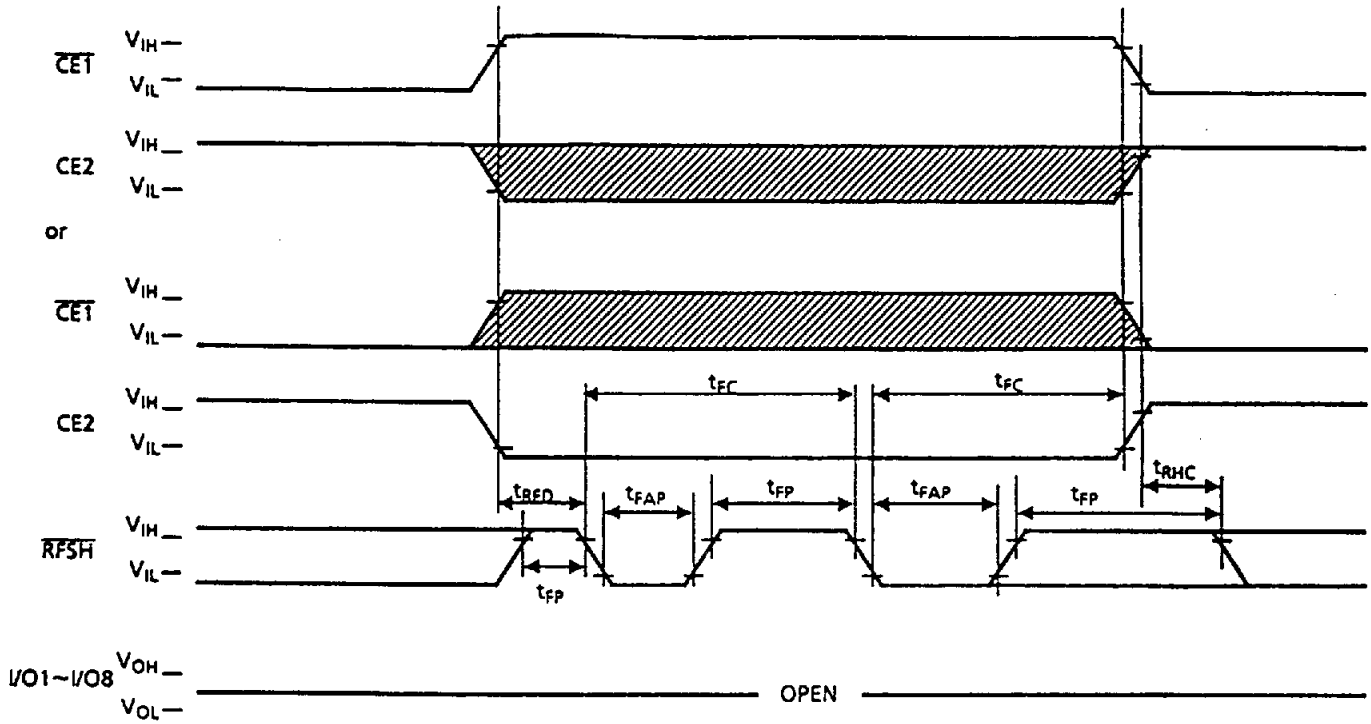
Note : A9 ~ A16 =  $V_{IH}$  or  $V_{IL}$

: H or L

Note: The device can be operated by cycling  $\overline{CE1}$  (or CE2) only provided that CE2 (or  $\overline{CE1}$ ) is connected to  $V_{IH}$  (or  $V_{IL}$ ).



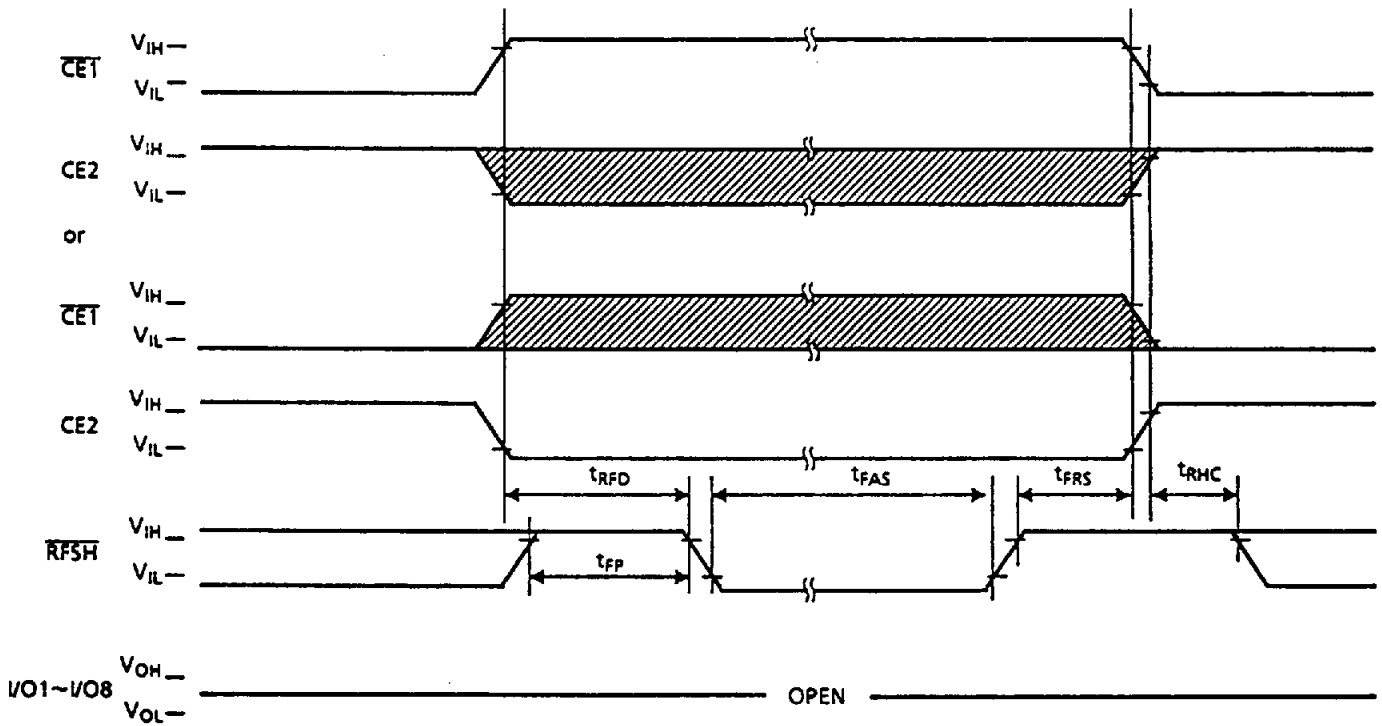
**Auto Refresh**



Note :  $\overline{OE}$ , R/W, A0 ~ A16 =  $V_{IH}$  or  $V_{IL}$

: H or L

**Self Refresh**



Note :  $\overline{OE}$ , R/W, A0 ~ A16 =  $V_{IH}$  or  $V_{IL}$

: H or L