SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129AFWI is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129AFWI utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129AFWI operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC518129AFWI features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129AFWI, with the CE2 pin in the TC518128A family changed to a CS pin. The TC518129AFWI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC518129AFWI is suitable for use in wide operating temperature systems. It is available in a 32-pin, 0.525 inch small outline plastic flat package.

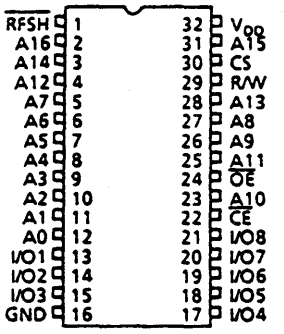
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

t_{CEA} $\overline{CE}$ Access Time	100ns
t_{OEA} $\overline{OE}$ Access Time	40ns
t_{RC} Cycle Time	160ns
Power Dissipation	330mW
Self Refresh Current	200μA

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Wide operating temperature: -40 ~ 85°C
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
  - TC518129AFWI: SOP32-P-525

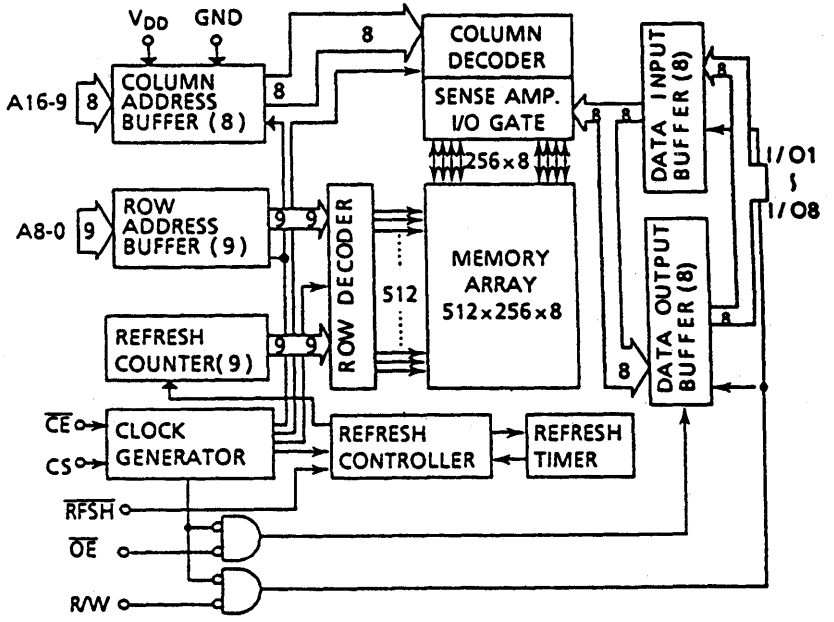
Pin Connection



Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8
Read	L	H	L	H	*	V*	OUT
Write	L	H	*	L	*	V*	IN
$\overline{CE}$ only Refresh	L	H	H	H	*	V*	HZ
CS Standby	L	L	*	*	*	*	HZ
Auto/Self Refresh	H	*	*	*	L	*	HZ
Standby	H	*	*	*	H	*	HZ

H = High level input (V_{IH})
L = Low level input (V_{IL})
* = V_{IH} or V_{IL}
V* = At the falling edge of $\overline{CE}$, all address inputs are latched. At all other times, the address inputs are "*".
HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	-40 ~ 85	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 1.0	V	
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	–	40	60	mA	3,4
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}	–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} - 0.2V, $\overline{RFSH}$ = V_{DD} - 0.2V	–	100	200	µA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}	–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE}$ = V_{DD} - 0.2V, $\overline{RFSH}$ = 0.2V	–	100	200	µA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{RFSH}$ cycling: t_{FC} = t_{FC} min	–	–	2	mA	
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	–	40	60	mA	3
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V	–	–	±10	µA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}	–	–	±10	µA	
V_{OH}	Output High Level I_{OH} = -5mA	2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA	–	–	0.4	V	

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	
C_{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-10		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	160	–	ns	
t_{RMW}	Read Modify Write Cycle Time	235	–		
t_{CE}	$\overline{CE}$ Pulse Width	100	10,000		
t_P	$\overline{CE}$ Precharge Time	50	–		
t_{CEA}	$\overline{CE}$ Access Time	–	100		
t_{OEA}	$\overline{OE}$ Access Time	–	40		
t_{CLZ}	$\overline{CE}$ to Output in Low -Z	30	–		
t_{OLZ}	$\overline{OE}$ to Output in Low -Z	0	–		
t_{WLZ}	Output Active from End of Write	0	–		
t_{CHZ}	Chip Disable to Output in High-Z	0	30		9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	30		9
t_{ODS}	$\overline{OE}$ Output Disable Setup Time	0	–		
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–		
t_{RCS}	Read Command Setup Time	0	–		
t_{RCH}	Read Command Hold Time	0	–		
t_{CSS}	Chip Select Setup Time	0	–		
t_{CSH}	Chip Select Hold Time	25	–		
t_{WP}	Write Pulse Width	70	–		
t_{WCH}	Write Command Hold Time	70	10,000		
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	70	10,000		
t_{DSW}	Data Setup Time from R/W	35	–		10
t_{DSC}	Data Setup Time from $\overline{CE}$	35	–		10
t_{DHW}	Data Hold Time from R/W	0	–		10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–		10
t_{ASC}	Address Setup Time	0	–		11
t_{AHC}	Address Hold Time	25	–		11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–		
t_{FC}	Auto Refresh Cycle Time	160	–		
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	50	–		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000		12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–		12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–		12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	190	–		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	ns	

Notes:

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO} and I_{DDF4} depend on the cycle time.

4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T = 5ns.

7) Timing reference levels

Input Levels	: V_{IH} = 2.6V V_{IL} = 0.6V	INPUT	2.6V, 0.6V, 2.4V, 0.8V
Input Reference Levels	: V_{IH} = 2.4V V_{IL} = 0.8V	OUTPUT	2.2V, 0.8V
Output Reference Levels	: V_{OH} = 2.2V V_{OL} = 0.8V		INPUT REFERENCE LEVEL, OUTPUT REFERENCE LEVEL

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data in latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

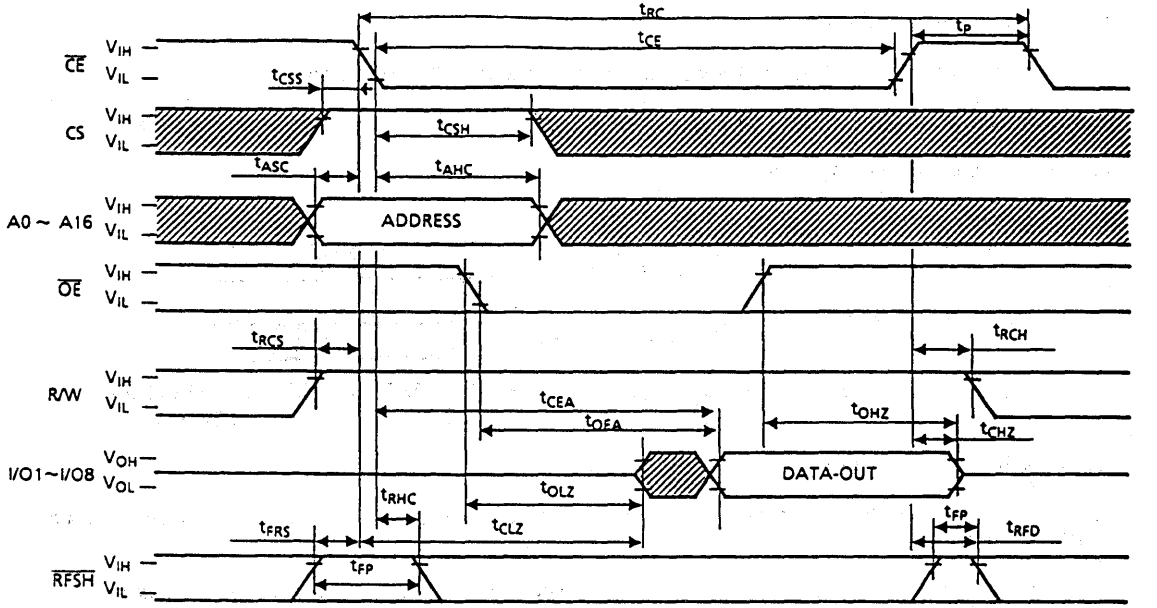
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC}.

12) The two refresh operations, auto refresh and self refresh, are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE}$ = V_{IH}.
Auto refresh : $\overline{RFSH}$ pulse width ≤ t_{FAP} (max.)
Self refresh : $\overline{RFSH}$ pulse width ≥ t_{FAS} (min.)

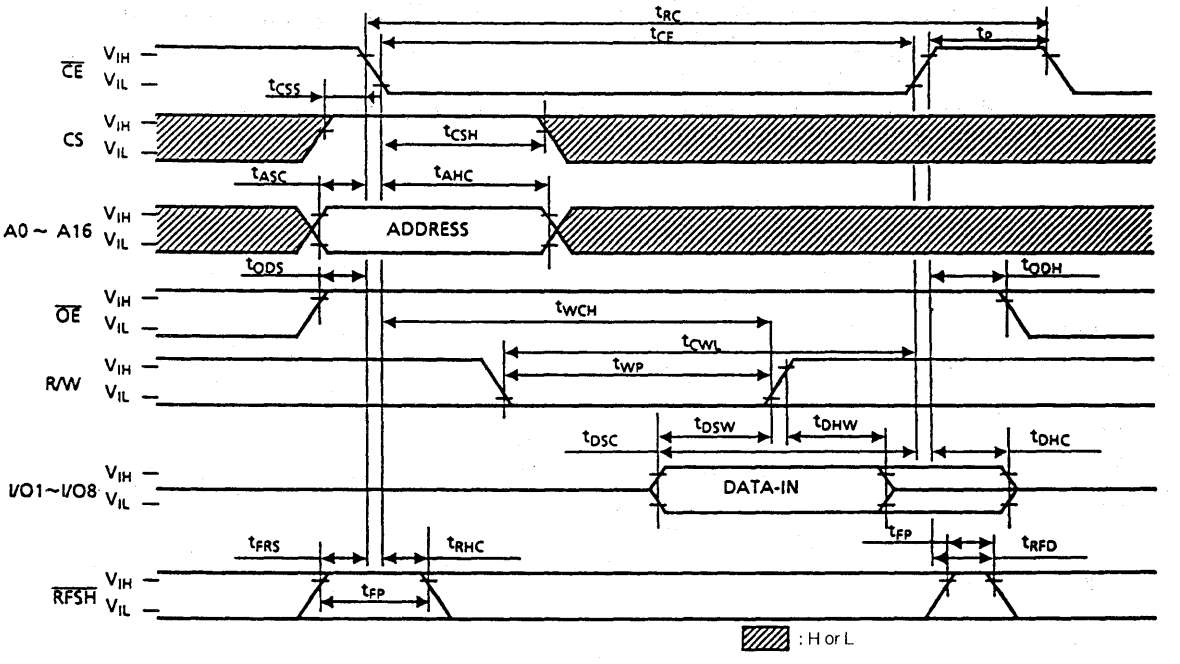
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
- if $\overline{RFSH}$ = "L" after power-up

Timing Waveforms

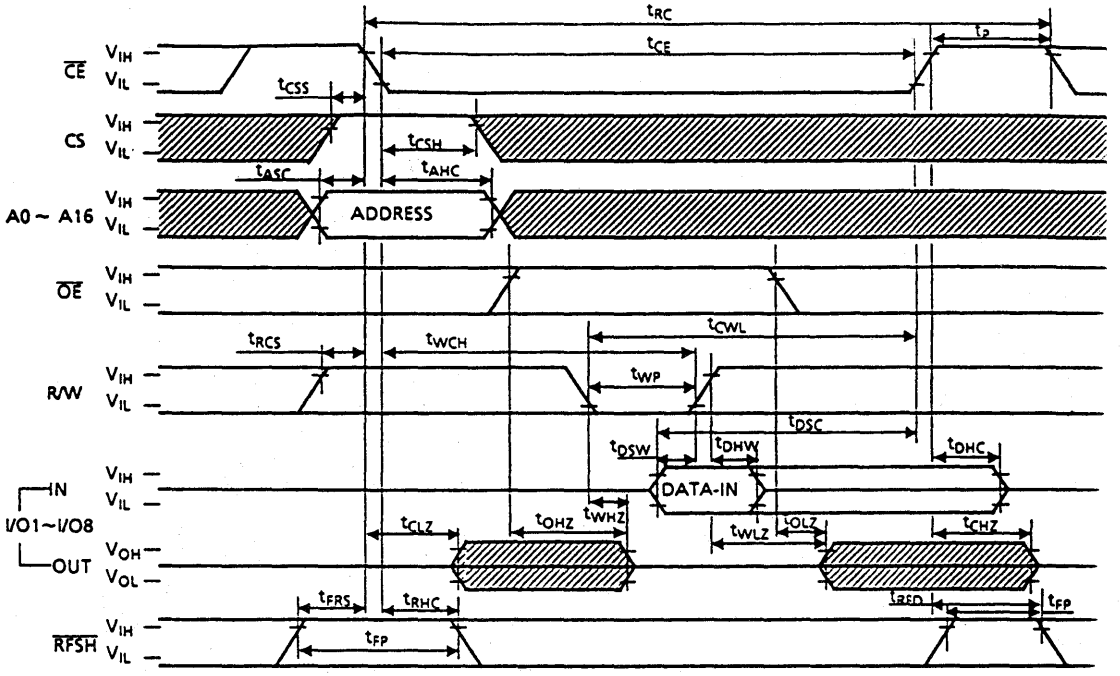
Read Cycle



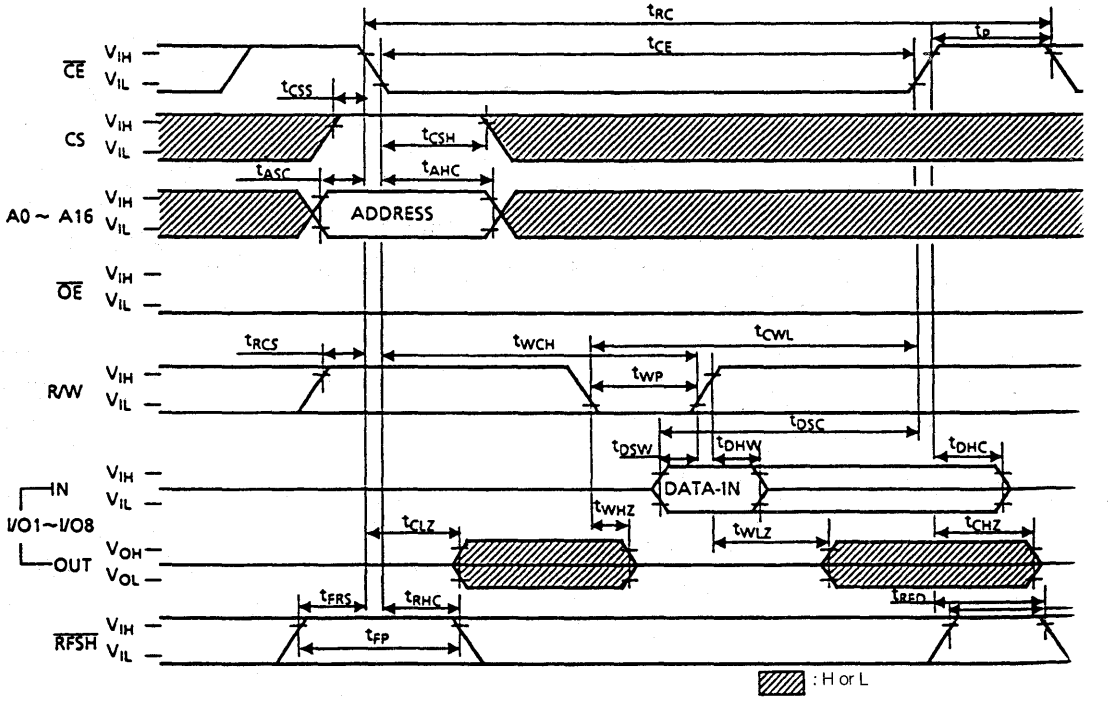
Write Cycle 1 ($\overline{OE}$ = Fixed High)



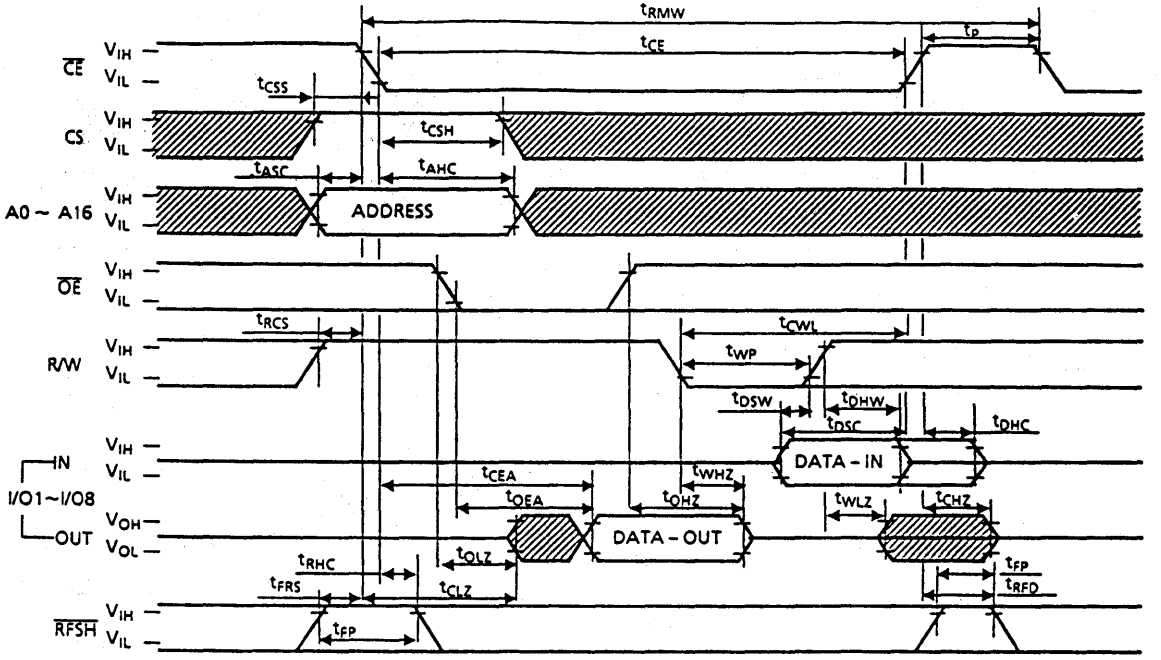
Write Cycle 2 ($\overline{OE}$ Clocked)



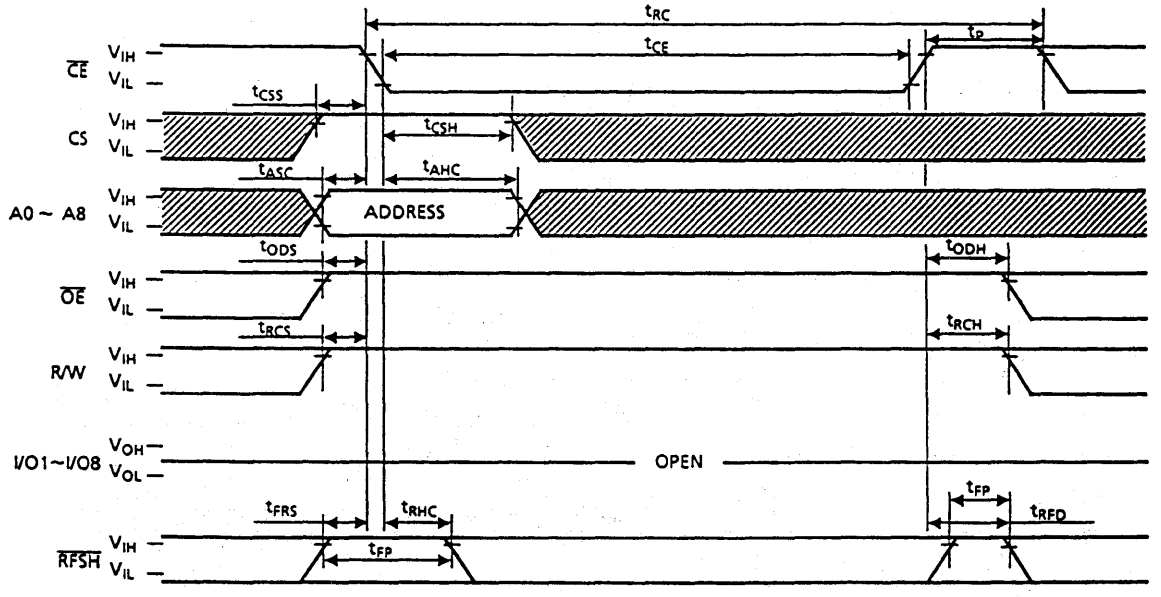
Write Cycle 3 ($\overline{OE}$ Fixed Low)



Read Modify Write Cycle



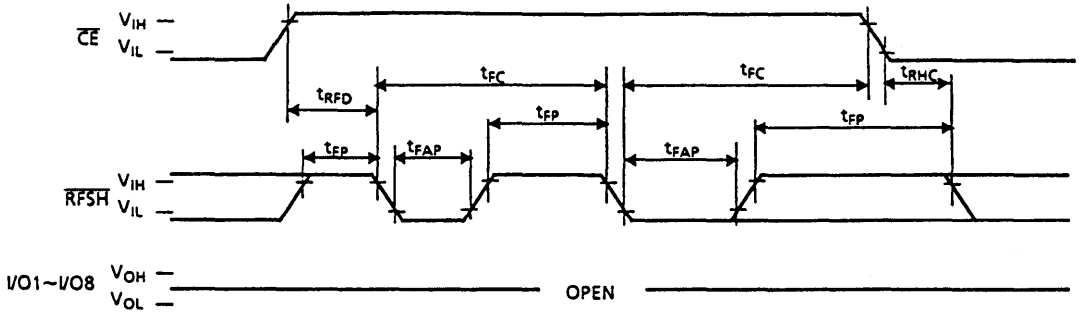
CE Only Refresh



NOTE : A9 ~ A16 = V_{IH} or V_{IL}

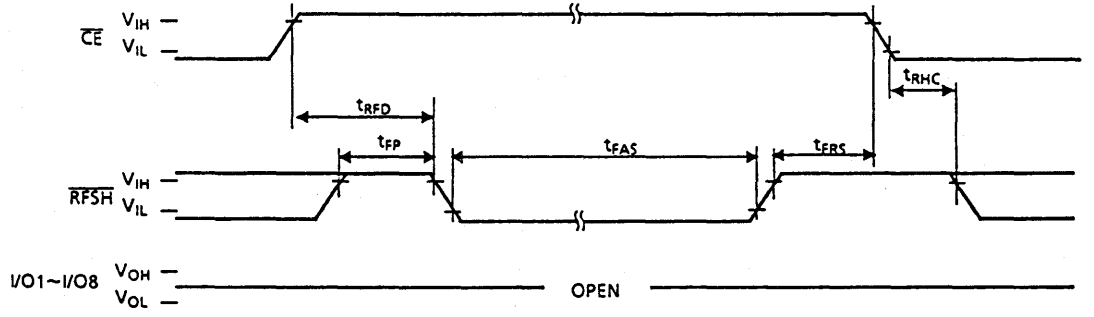
▨ : H or L

Auto Refresh



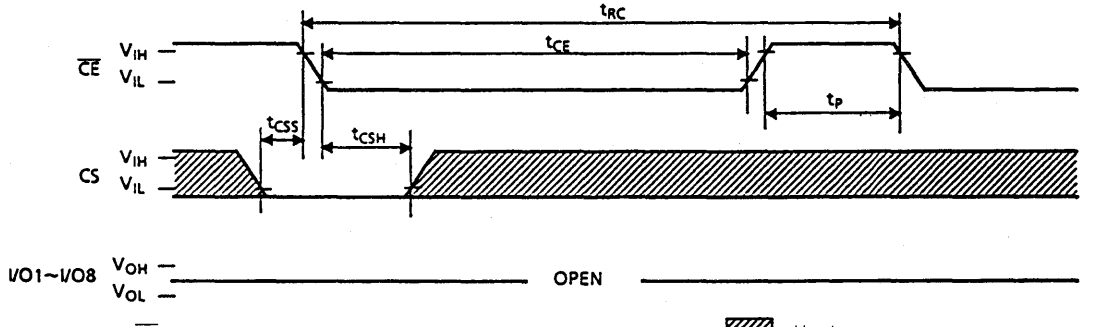
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = V_{IH} or V_{IL}

Self Refresh



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = V_{IH} or V_{IL}

CS Standby Mode



NOTE : $\overline{OE}$, R/W, A0 ~ A16 = V_{IH} or V_{IL}

: H or L