

TC518129AP/ASP/AF/AFW-80/10/12 TC518129APL/ASPL/AFL/AFWL-80/10/12 TC518129AFTL-80/10/12

SILICON GATE CMOS**131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM****Description**

The TC518129A is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129A utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129A operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129A features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

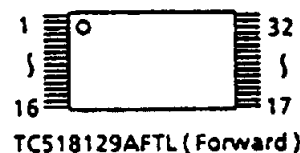
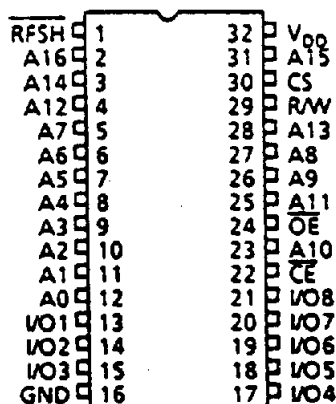
A CS standby mode interface is incorporated in the TC518129A family, with the CE2 pin in the TC518128A family changed to a CS pin. The TC518129A is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518129A Family		
	-80	-10	-12
t_{CEA} \overline{CE} Access Time	80ns	100ns	120ns
t_{OEA} \overline{OE} Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200 μ A (L version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129AP/APL : DIP32-P-600
 - TC518129AF/AFL : SOP32-P-450
 - TC518129ASP/ASPL : DIP32-P-300
 - TC518129AFW/AFWL : SOP32-P-525
 - TC518129AFTL : TSOP32-P-0820

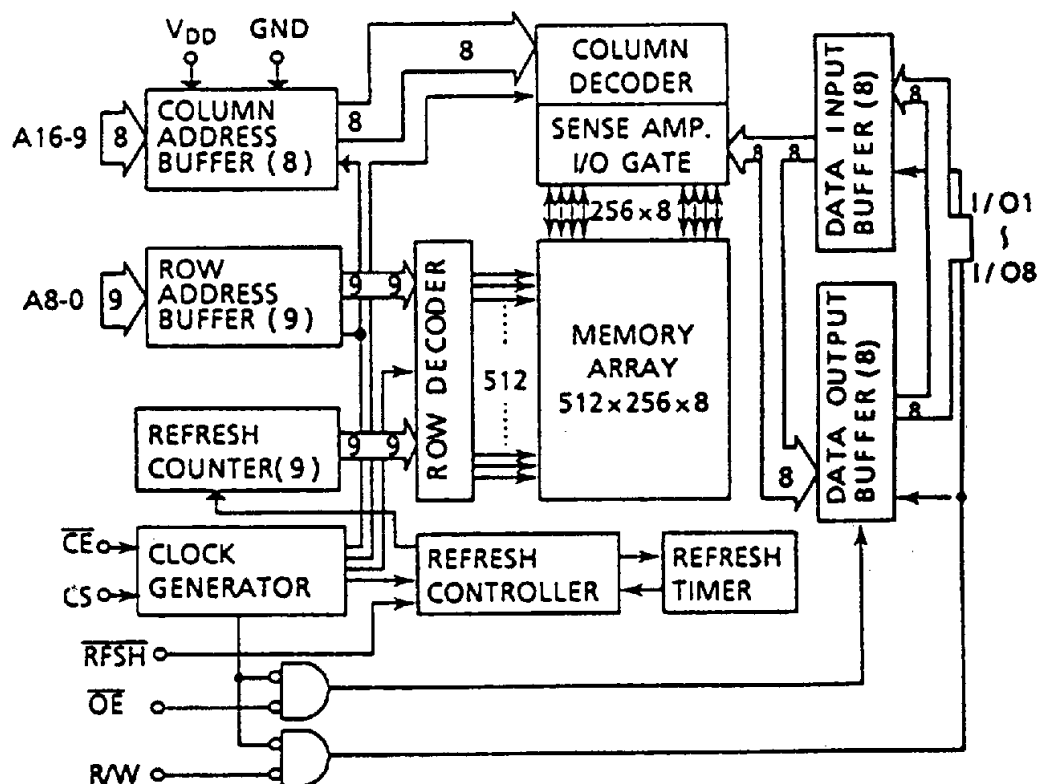
Pin Connection (Top View)**TC518129APL / AFL / ASPL / AFWL****Pin Names**

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V_{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	\overline{RFSH}	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})L = Low level input (V_{IL})* = V_{IH} or V_{IL} V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	–	V _{DD} + 1.0	V	
V _{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES	
I _{DDO}	Operating Current (Average) CE, Address cycling: t _{RC} = t _{RC} min.	80ns version	–	50	70	mA	3,4
		100ns version	–	40	60		
		120ns version	–	35	50		
I _{DDS1}	Standby Current CE = V _{IH} , RFSH = V _{IH}	Normal version	–	–	2	mA	
		L version	–	–	1		
I _{DDS2}	Standby Current CE = V _{DD} - 0.2V, RFSH = V _{DD} - 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200		
I _{DDF1}	Self Refresh Current (Average) CE = V _{IH} , RFSH = V _{IL}	Normal version	–	–	2	mA	
		L version	–	–	1		
I _{DDF2}	Self Refresh Current (Average) CE = V _{DD} - 0.2V, RFSH = 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200		
I _{DDF3}	Auto Refresh Current (Average) RFSH cycling: t _{FC} = t _{FC} min	–	–	2	mA		
I _{DDF4}	CE only Refresh Current (Average) CE, Address cycling: t _{RC} = t _{RC} min.	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	–	–	±10	μA		
I _{O(L)}	Output Leakage Current Output Disabled (CE = V _{IH} or OE = V _{IH} or R/W = V _{IL}), 0V ≤ V _{OUT} ≤ V _{DD}	–	–	±10	μA		
V _{OH}	Output High Level I _{OH} = -5mA	2.4	–	–	V		
V _{OL}	Output Low Level I _{OL} = 4.2mA	–	–	0.4	V		

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C _{I2}	Input Capacitance (CE, CS, OE, R/W, RFSH)	–	7	
C _{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t _{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	80	10,000	100	10,000	120	10,000		
t _p	$\overline{\text{CE}}$ Precharge Time	40	–	50	–	60	–		
t _{CEA}	$\overline{\text{CE}}$ Access Time	–	80	–	100	–	120		
t _{OEa}	$\overline{\text{OE}}$ Access Time	–	35	–	40	–	50		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low -Z	30	–	30	–	30	–		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low -Z	0	–	0	–	0	–		
t _{WLZ}	Output Active from End of Write	0	–	0	–	0	–		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35		9
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	25	0	30	0	35		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35		9
t _{ODS}	$\overline{\text{OE}}$ Output Disable Setup Time	0	–	0	–	0	–		
t _{ODH}	$\overline{\text{OE}}$ Output Disable Hold Time	10	–	10	–	10	–		
t _{RCS}	Read Command Setup Time	0	–	0	–	0	–		
t _{RCH}	Read Command Hold Time	0	–	0	–	0	–		
t _{CSS}	Chip Select Setup Time	0	–	0	–	0	–		
t _{CSH}	Chip Select Hold Time	20	–	25	–	30	–		
t _{WP}	Write Pulse Width	60	–	70	–	85	–		
t _{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	60	10,000	70	10,000	85	10,000		
t _{DSW}	Data Setup Time from R/W	30	–	35	–	45	–		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	30	–	35	–	45	–		10
t _{DHW}	Data Hold Time from R/W	0	–	0	–	0	–		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	–	0	–	0	–		10
t _{ASC}	Address Setup Time	0	–	0	–	0	–		11
t _{AHC}	Address Hold Time	20	–	25	–	30	–		11
t _{RHC}	RFSH Command Hold Time	15	–	15	–	15	–		
t _{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	40	–	50	–	60	–		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t _{FP}	RFSH Precharge Time	30	–	30	–	30	–		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–		12
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	160	–	190	–	225	–	12	
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	–	8	–	8	–	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

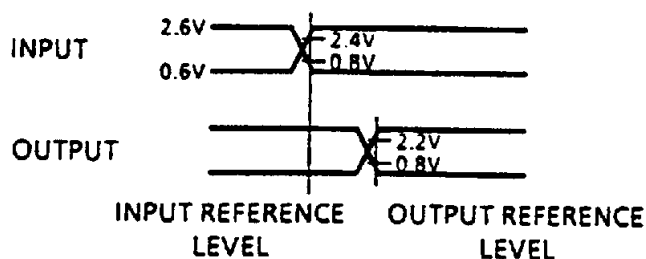
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} and I_{DDF4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels : $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

Input Reference Levels : $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

Output Reference Levels : $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$



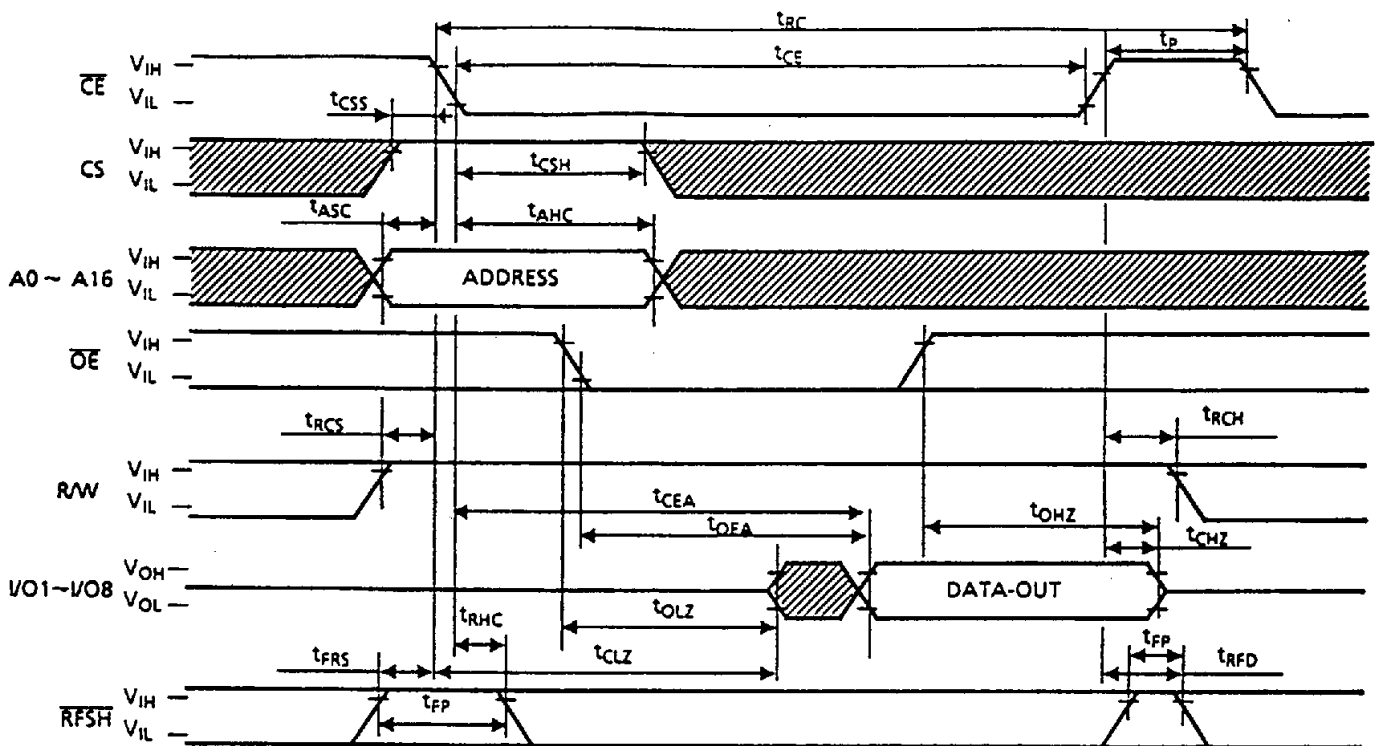
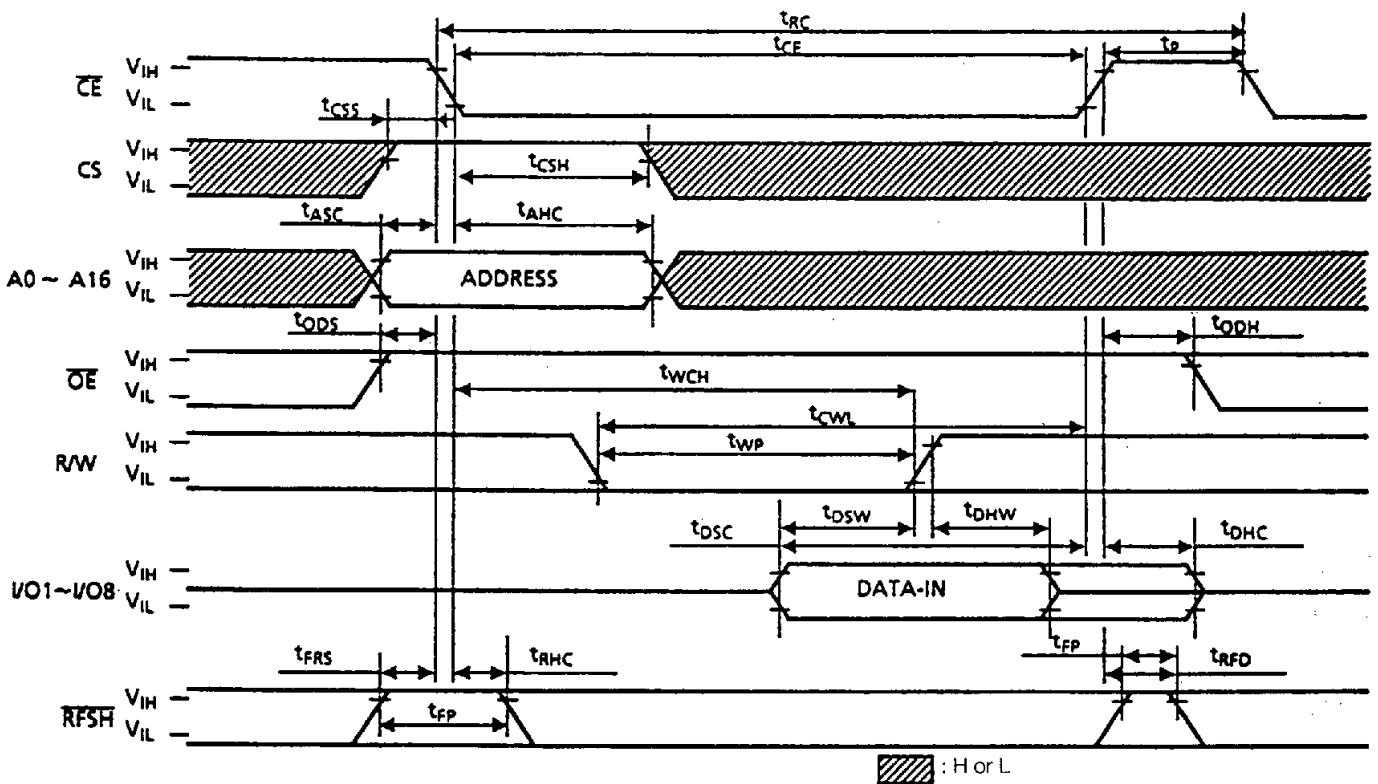
- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

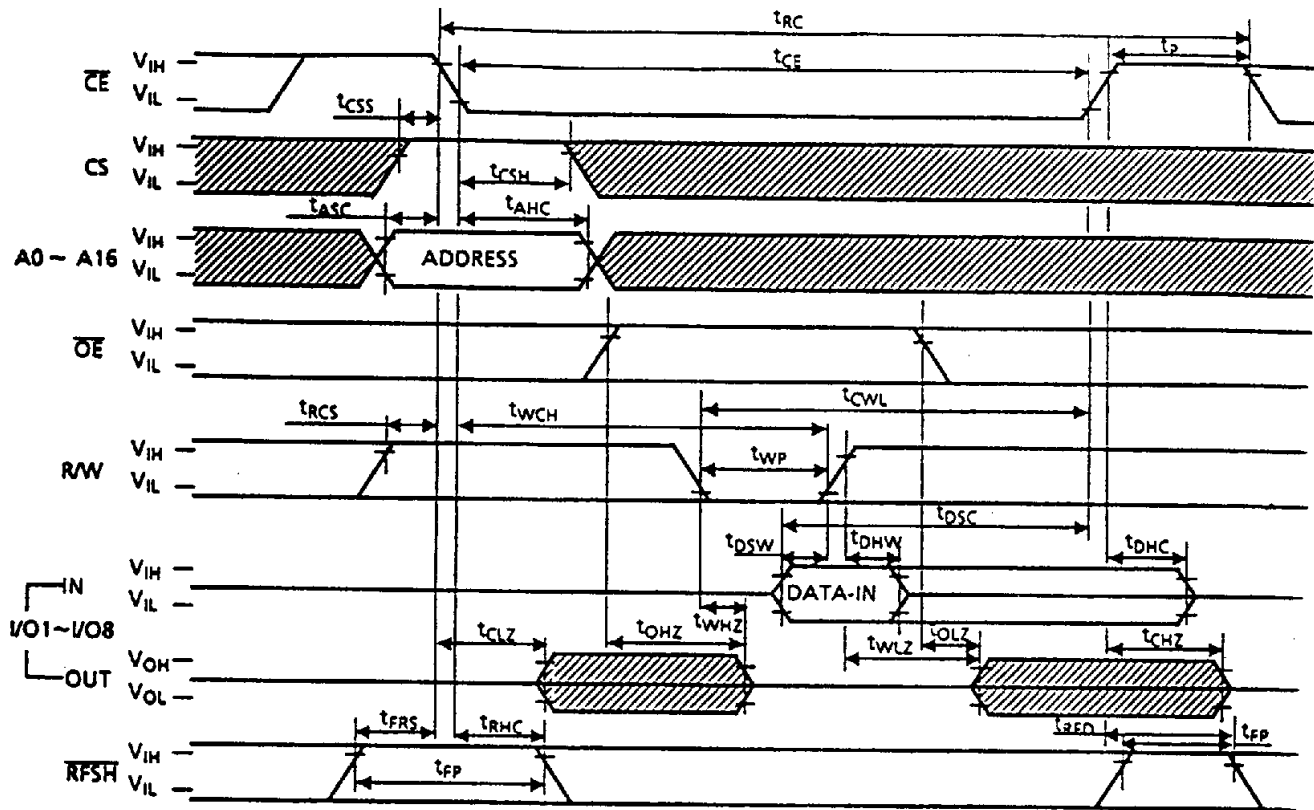
- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

Timing Waveforms

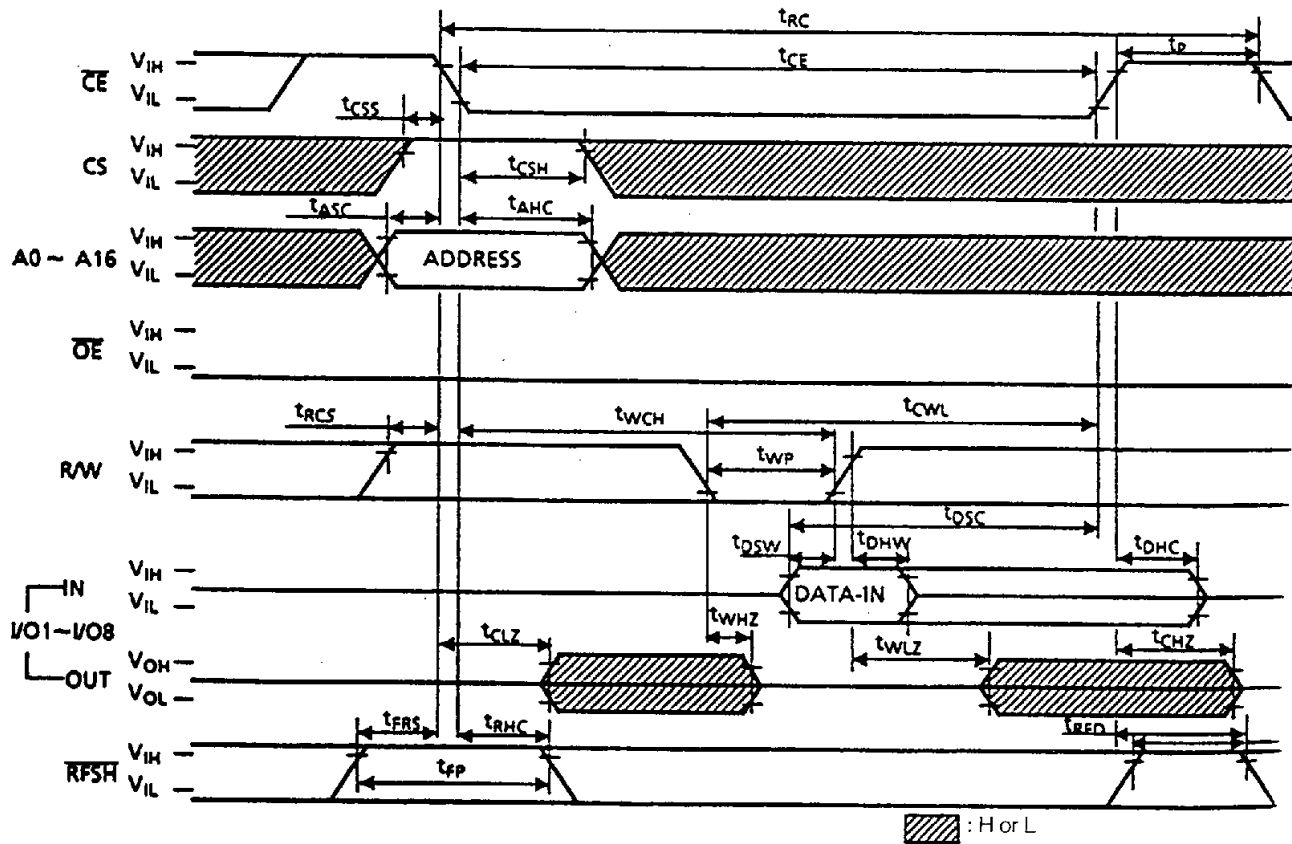
Read Cycle

Write Cycle 1 (\overline{OE} Fixed High)

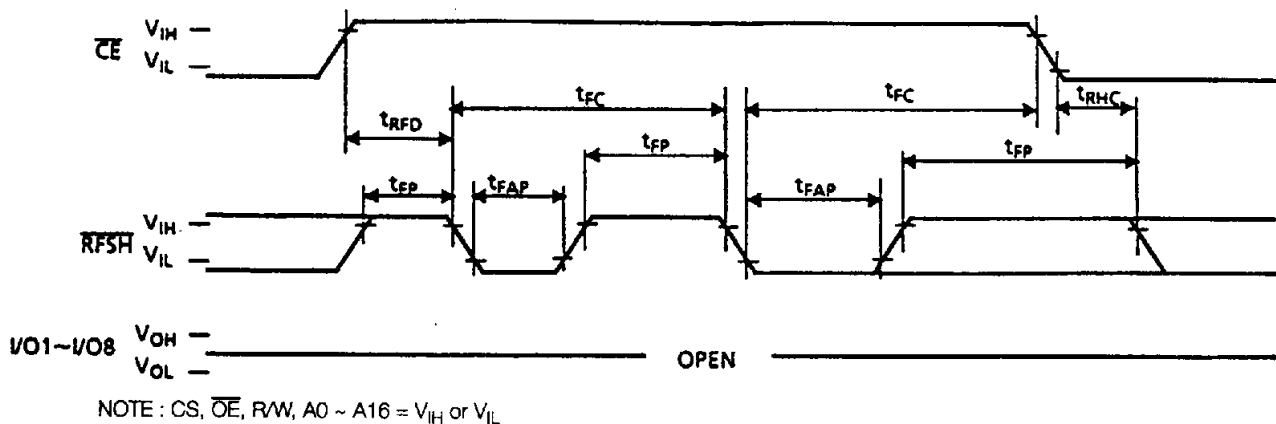
Write Cycle 2 (\overline{OE} Clocked)



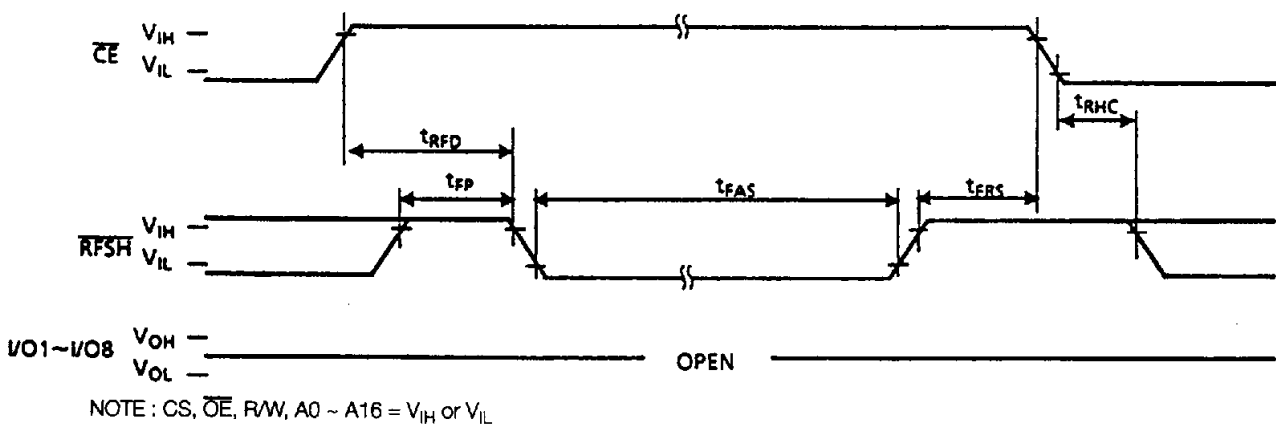
Write Cycle 3 (\overline{OE} Fixed Low)



Auto Refresh



Self Refresh



CS Standby Mode

