

TC518129BPL/BFL/BFWL/BFTL-70V/80V/10V

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518129B-V is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518129B-V utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518129B-V operates from a single power supply of 2.7 ~ 5.5V. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC518129B-V features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

A CS standby mode interface is incorporated in the TC518129B-V family, with the CE2 pin in the TC518128B-V family changed to a CS pin. The TC518129B-V is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

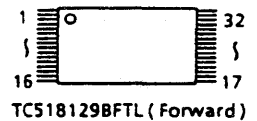
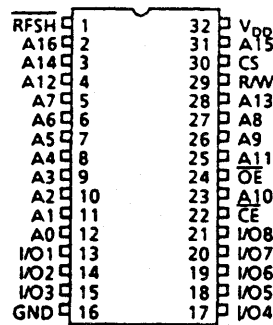
Features

- Organization: 131,072 words x 8 bits
- Low voltage operation: 2.7V ~ 5.5V
- Data retention supply voltage: 2.7V ~ 5.5V
- Fast access time

	TC518129B-V Family		
	-70	-80	-10
t_{CEA} \overline{CE} Access Time	70ns	80ns	100ns
t_{OEA} \overline{OE} Access Time	25ns	30ns	40ns
t_{RC} Cycle Time	115ns	130ns	160ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	5.5V	50 μ A	
	3.0V	25 μ A	

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Package
 - TC518129BPL-V: DIP32-P-600
 - TC518129BFL-V: SOP32-P-450
 - TC518129BFWL-V: SOP32-P-525
 - TC518129BFTL-V: TSOP32-P-0820

Pin Connection (Top View)



TC518129BPL / BFL / BFWL

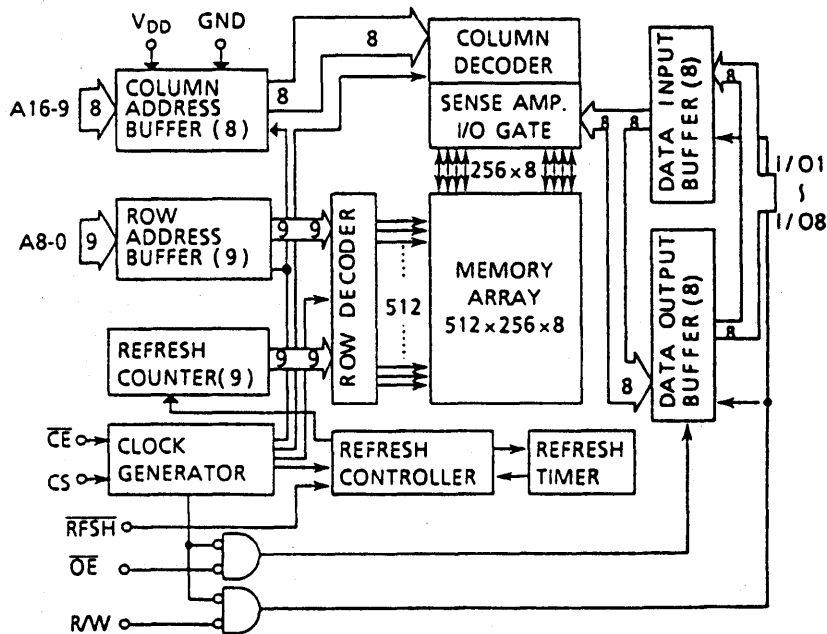
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
RFSH	Refresh Input
\overline{CE}	Chip Enable Input
CS	Chip Select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CS	A ₁₅	V _{DD}	RFSH	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	CS	\overline{OE}	R/W	\overline{RFSH}	A0 ~ A16	I/O1 ~ 8
Read		L	H	L	H	*	V*	OUT
Write		L	H	*	L	*	V*	IN
\overline{CE} only Refresh		L	H	H	H	*	V*	HZ
CS Standby		L	L	*	*	*	*	HZ
Auto/Self Refresh		H	*	*	*	L	*	HZ
Standby		H	*	*	*	H	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "*".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE, Address cycling: $t_{RC} = t_{RC}$ min.	70ns version	–	50	70	mA 3,4
		80ns version	–	40	60	
		100ns version	–	35	50	
I_{DDS1}	Standby Current CE = V_{IH} , RFSH = V_{IH}	–	–	1	mA	
I_{DDS2}	Standby Current CE = $V_{DD} - 0.2V$, RFSH = $V_{DD} - 0.2V$	–	35	50	μA	
I_{DDF1}	Self Refresh Current (Average) CE = V_{IH} , RFSH = V_{IL}	–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average) CE = $V_{DD} - 0.2V$, RFSH = $0.2V$	–	35	50	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC}$ min.	–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE, Address cycling: $t_{RC} = t_{RC}$ min.	70ns version	–	50	70	mA 3
		80ns version	–	40	60	
		100ns version	–	35	50	
I_{IL}	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other inputs not under test = $0V$	–	–	± 10	μA	
I_{OL}	Output Leakage Current Output Disabled (CE = V_{IH} or OE = V_{IH} or R/W = V_{IL}), $0V \leq V_{OUT} \leq V_{DD}$	–	–	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1.0\text{mA}$	2.4	–	–	V	
V_{OL}	Output Low Level $I_{OL} = 2.1\text{mA}$	–	–	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance (CE, CS, OE, R/W, RFSH)	–	7	
C_{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—	ns	
t _{RMW}	Read Modify Write Cycle Time	160	—	180	—	220	—		
t _{CE}	\overline{CE} Pulse Width	70	10,000	80	10,000	100	10,000		
t _p	\overline{CE} Precharge Time	35	—	40	—	50	—		
t _{CEA}	\overline{CE} Access Time	—	70	—	80	—	100		
t _{OEa}	\overline{OE} Access Time	—	25	—	30	—	40		
t _{CLZ}	\overline{CE} to Output in Low -Z	20	—	20	—	20	—		
t _{OLZ}	\overline{OE} to Output in Low -Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{ODS}	\overline{OE} Output Disable Setup Time	0	—	0	—	0	—		
t _{ODH}	\overline{OE} Output Disable Hold Time	10	—	10	—	10	—		
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{CSS}	Chip Select Setup Time	0	—	0	—	0	—		
t _{CSH}	Chip Select Hold Time	20	—	25	—	30	—		
t _{WP}	Write Pulse Width	20	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	35	10,000	40	10,000	50	10,000		
t _{CWL}	Write Command to \overline{CE} Lead Time	20	10,000	25	10,000	30	10,000		
t _{DSW}	Data Setup Time from R/W	15	—	20	—	25	—		10
t _{DSC}	Data Setup Time from \overline{CE}	15	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from \overline{CE}	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	25	—	30	—		11
t _{RHC}	RFSH Command Hold Time	15	—	15	—	15	—		
t _{FC}	Auto Refresh Cycle Time	115	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from \overline{CE}	35	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—	12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t _{FRS}	\overline{CE} Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—	12	
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	—	8	—	8	—	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

3.0V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	—	$V_{DD} + 1.0V$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3.0V \pm 0.3V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) CE Address cycling: $t_{RC} = t_{RC}$ min.	—	15	20	mA	3,4
I_{DSS2}	Standby Current	—	15	25	μA	
I_{DDF2}	Self Refresh Current (Average)	—	15	25	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC}$ min.	—	—	2	mA	
I_{DDF4}	CE only Refresh Current (Average) CE Address cycling: $t_{RC} = t_{RC}$ min.	—	15	20	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable, $0V \leq V_{OUT} \leq V_{DD}$	—	—	± 10	μA	
V_{OH}	Output High Level	$I_{OH} = -1\text{mA}$	2.4	—	—	V
		$I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2V$	—	—	
V_{OL}	Output Low Level	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
		$I_{OL} = 100\mu\text{A}$	—	—	0.2	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.0V±0.3V) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	240	–		
t _{RMW}	Read Modify Write Cycle Time	320	–		
t _{CE}	CE Pulse Width	150	10,000		13
t _p	CE Precharge Time	80	–		
t _{CEA}	CE Access Time	–	150		
t _{OEA}	OE Access Time	–	80		
t _{CLZ}	CE to Output in Low -Z	20	–		
t _{OLZ}	OE to Output in Low -Z	5	–		
t _{WLZ}	Output Active from End of Write	5	–		
t _{CHZ}	Chip Disable to Output in High-Z	0	30		9
t _{OHZ}	OE Disable to Output in High-Z	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	40		9
t _{ODS}	OE Output Disable Setup Time	0	–		
t _{ODH}	OE Output Disable Hold Time	10	–		
t _{RCS}	Read Command Setup Time	0	–		
t _{RCH}	Read Command Hold Time	0	–		
t _{WP}	Write Pulse Width	35	–	ns	
t _{WCH}	Write Command Hold Time	70	10,000		
t _{CWL}	Write Command to CE Lead Time	35	10,000		
t _{DSW}	Data Setup Time from R/W	30	–		10
t _{DSC}	Data Setup Time from CE	30	–		10
t _{DHW}	Data Hold Time from R/W	0	–		10
t _{DHC}	Data Hold Time from CE	0	–		10
t _{ASC}	Address Setup Time	0	–		11
t _{AHC}	Address Hold Time	35	–		11
t _{RHC}	RFSH Command Hold Time	15	–		
t _{FC}	Auto Refresh Cycle Time	240	–		
t _{RFD}	RFSH Delay Time from CE	80	–		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	50	8,000		12
t _{FP}	RFSH Precharge Time	50	–		12
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	–		12
t _{FRS}	CE Delay Time from RFSH (Self Refresh)	300	–		12
t _{REF}	Refresh Period (512 cycles, A0 ~ A8)	–	8	ms	
t _T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

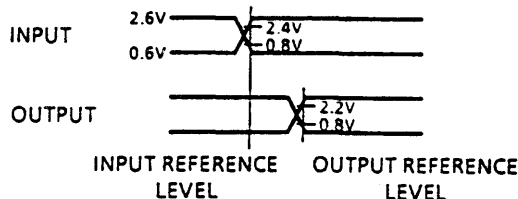
Output Reference Levels: 1.5V/1.5V

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDO} and I_{DDF4} depend on the cycle time.
- 4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels	: $V_{IH} = 2.6V$ $V_{IL} = 0.6V$
Input Reference Levels	: $V_{IH} = 2.4V$ $V_{IL} = 0.8V$
Output Reference Levels	: $V_{OH} = 2.2V$ $V_{OL} = 0.8V$



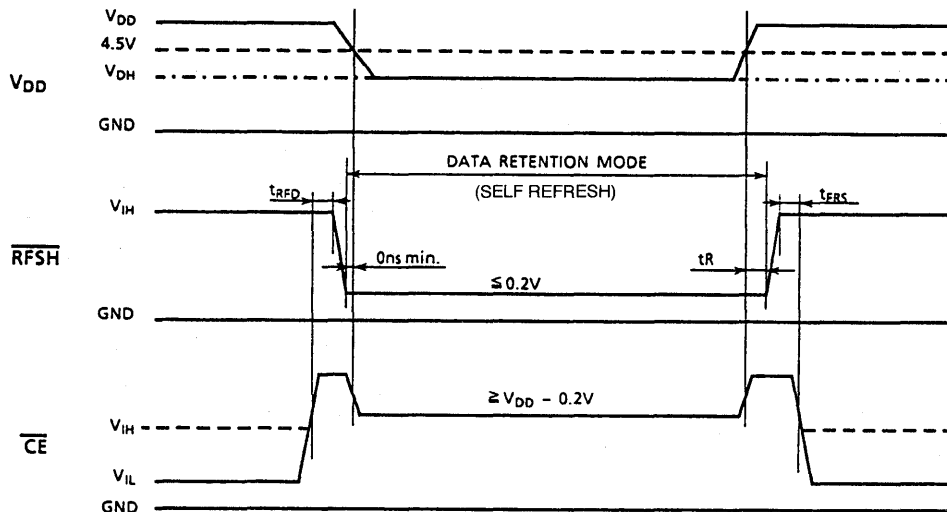
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of R/W or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{RFSH} = "L"$ after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

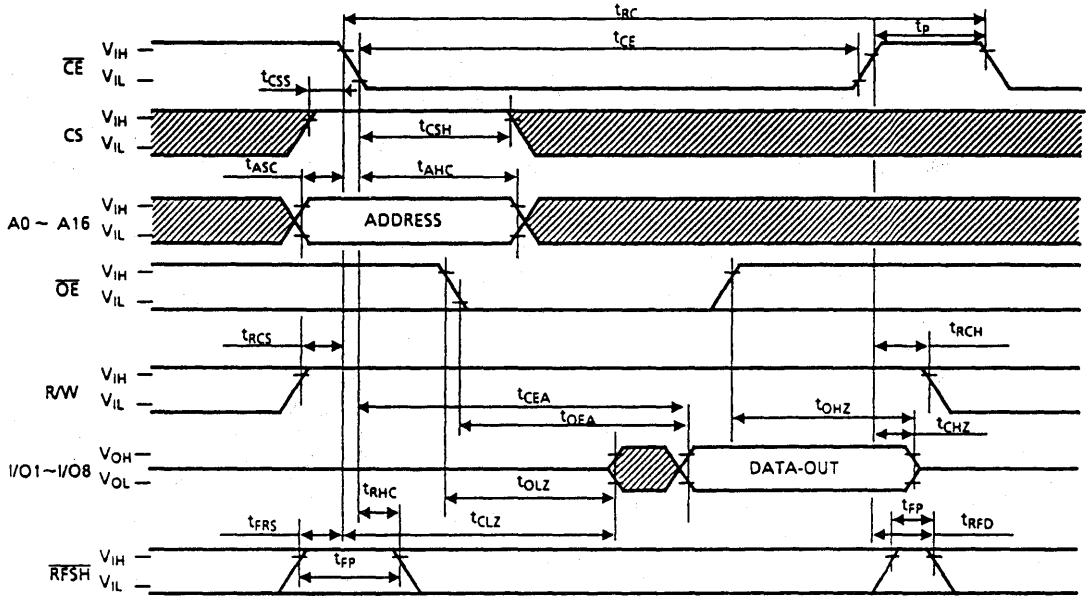
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.7	-	5.5	V
I _{DDF2}	Self Refresh Current	V _{DH} = 3.0V	-	15	μA
		V _{DH} = 5.5V	-	35	
t _R	Recovery Time	5	-	-	ms



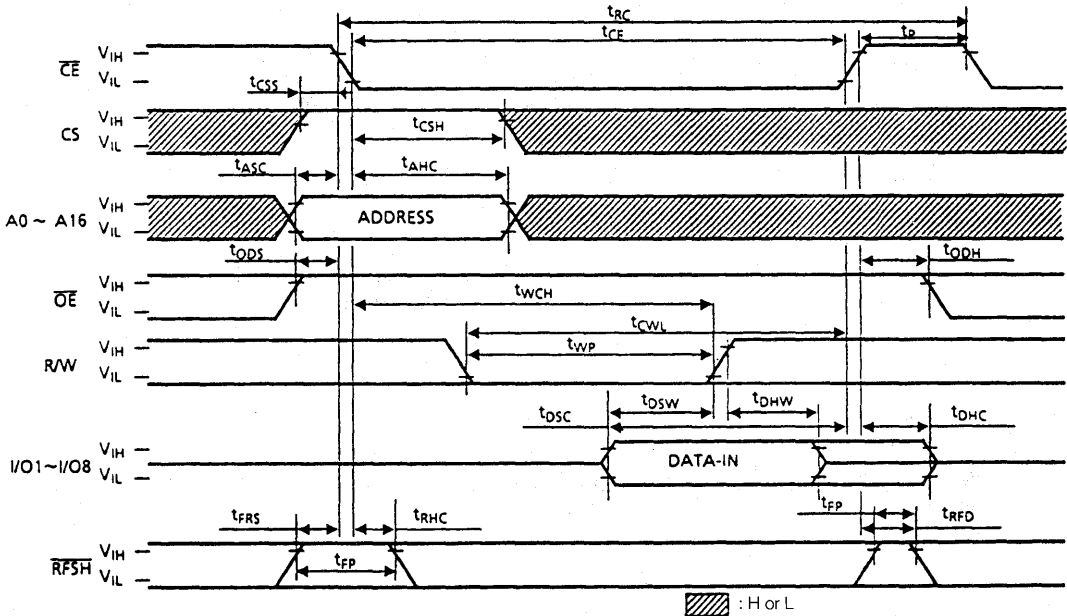
Notes: CS, \overline{OE} , R/W, A0 ~ A16 = V_{IH} or V_{IL}
 I_{DDF1} is applicable when \overline{RFSH} = V_{IL} (max.), \overline{CE} = V_{IH} (min.).

Timing Waveforms

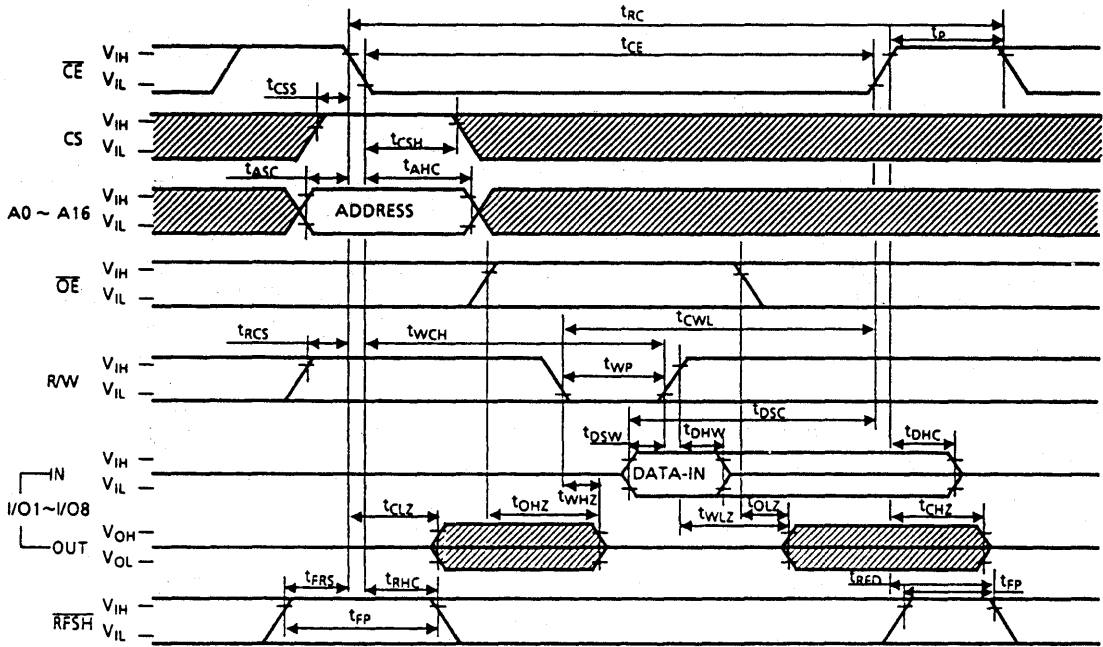
Read Cycle



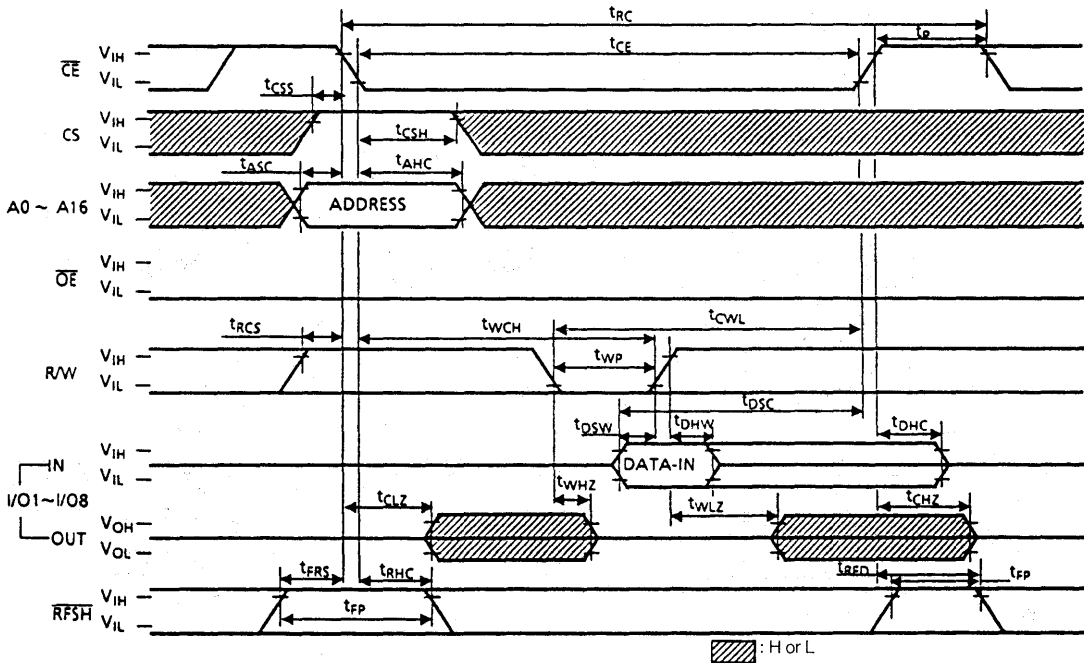
Write Cycle 1 (\overline{OE} Fixed High)



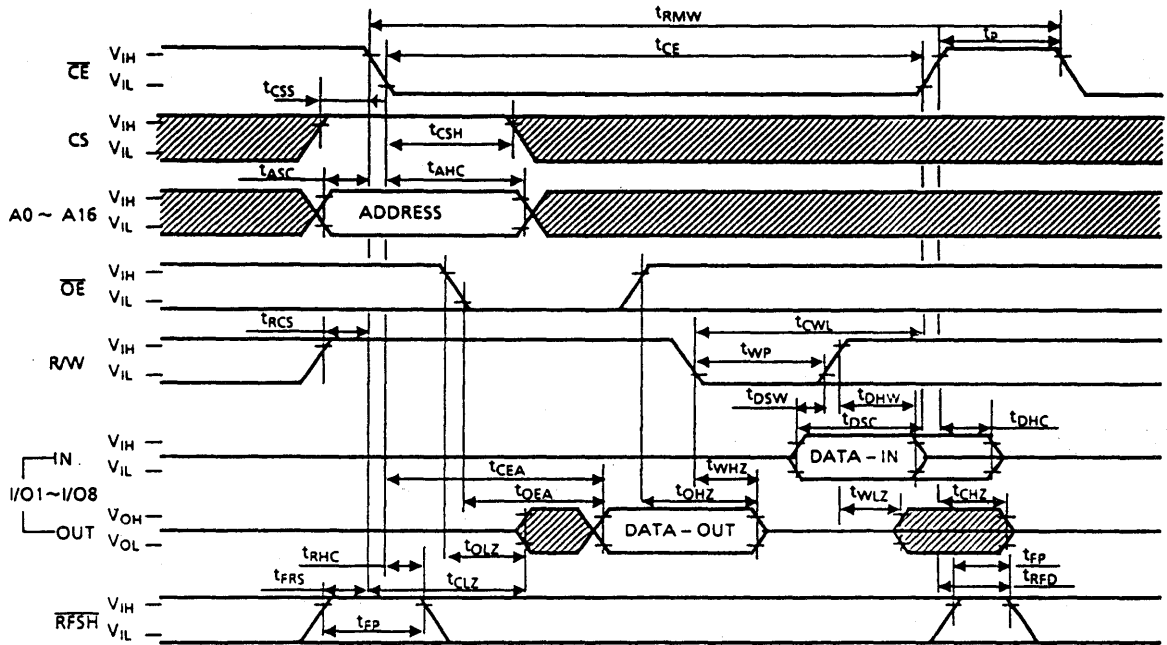
Write Cycle 2 (\overline{OE} Clocked)



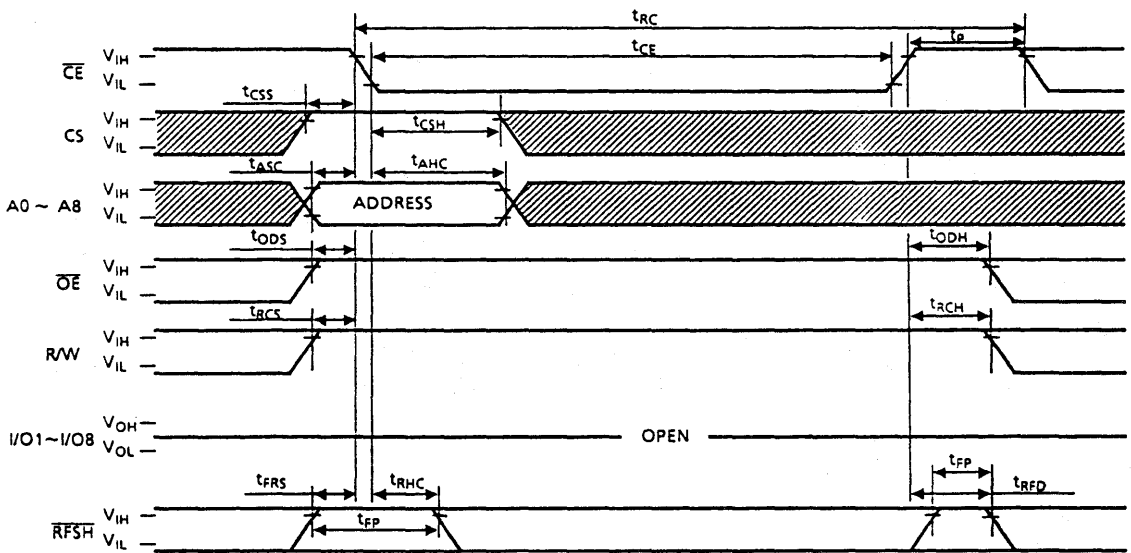
Write Cycle 3 (\overline{OE} Fixed Low)



Read Modify Write Cycle



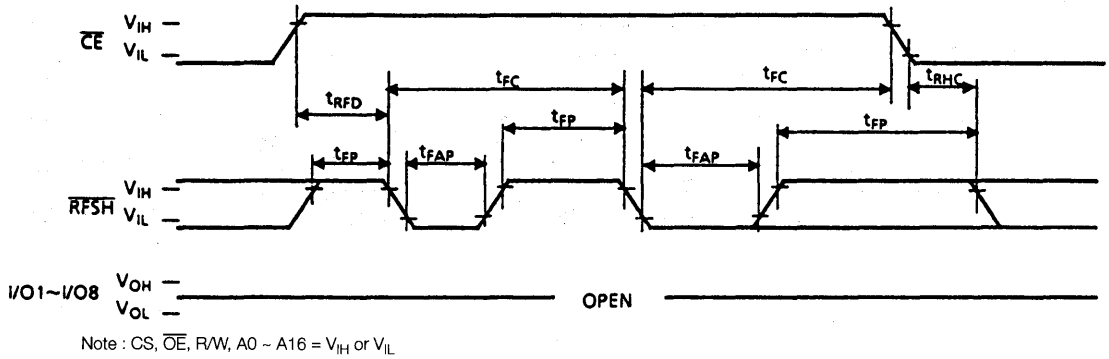
\overline{CE} Only Refresh



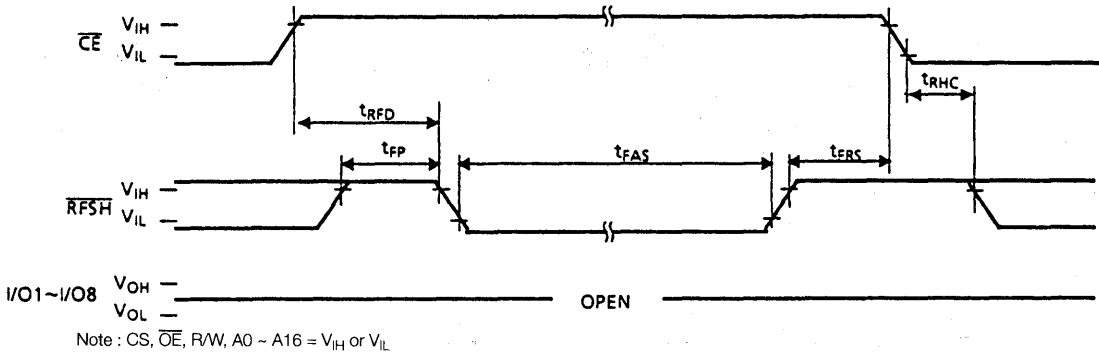
Note: A9 ~ A16 = V_{IH} or V_{IL}

▨ : H or L

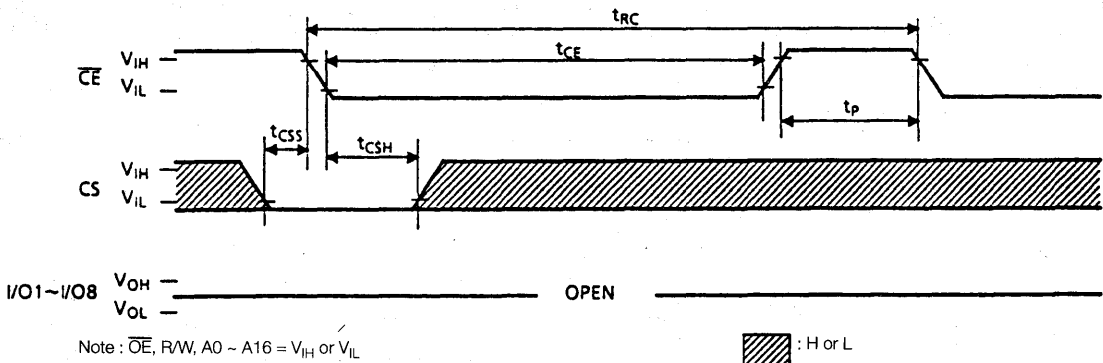
Auto Refresh



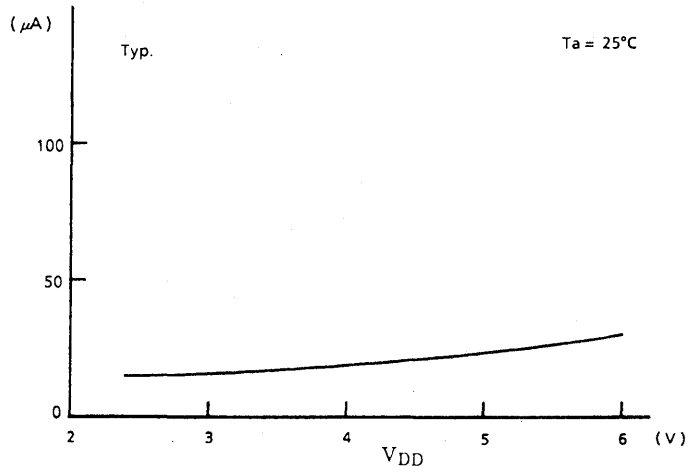
Self Refresh



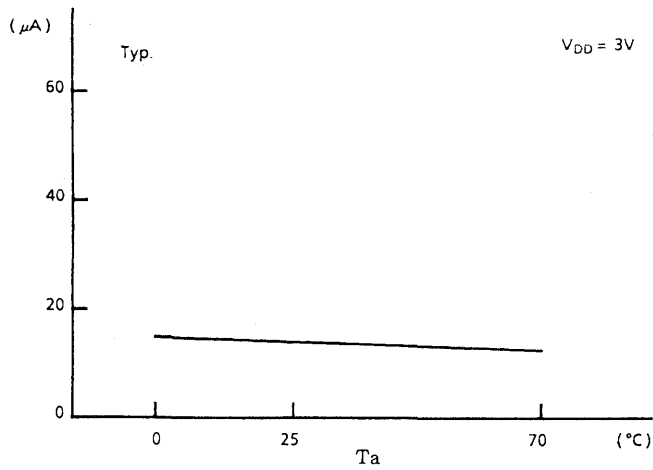
CS Standby Mode



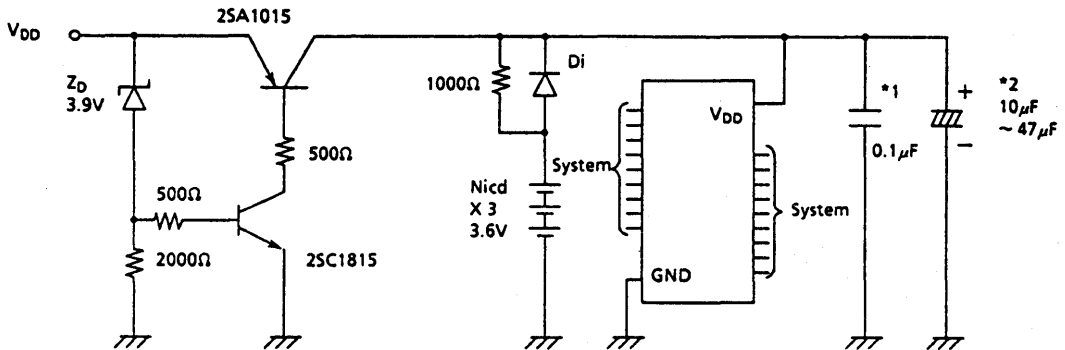
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Backup Application Example



*1: Ceramic condenser

*2: Tantalum condenser

(A large bypass condenser is preferable to absorb noise when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turnoff of the power supply must be avoided. Enter the Self Refresh mode before changing to the battery backup power supply.