TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 CMOS PSEUDO STATIC RAM
SILICON MONOLITHIC
SILICON GATE CMOS

TC51832PL-85, TC51832PL-10
TC51832PL-12

DESCRIPTION

The TC51832PL is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832PL utilized one transistor dynamic memory cell with CMOS peripheral circuit to provide large capacity, high speed and low power features. System oriented features include single power supply of 5V±10% torelance. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation — auto refresh and self refresh. The TC51832PL also features static RAM like write function that the input data iswritten into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832PL is a pin-compatible with 256K bit CMOS static RAM - TC55257P and is moulded a standard 0.6 inch width plastic DIP.

FEATURES

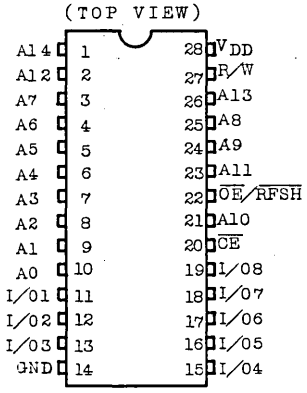
- Organization: 32,768 word 8 bit
- Fast Access Time and Cycle Time

	TC51832PL-85	TC51832PL-10	TC51832PL-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V±10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  - Operating : 303mW(TC51832PL-85)
    248mW(TC51832PL-10)
    220mW(TC51832PL-12)
  - Standby : 1.1mW
  - Self Refresh: 1.1mW
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin compatible with 256K bit CMOS Static TAM TC55257P

PIN CONNECTION

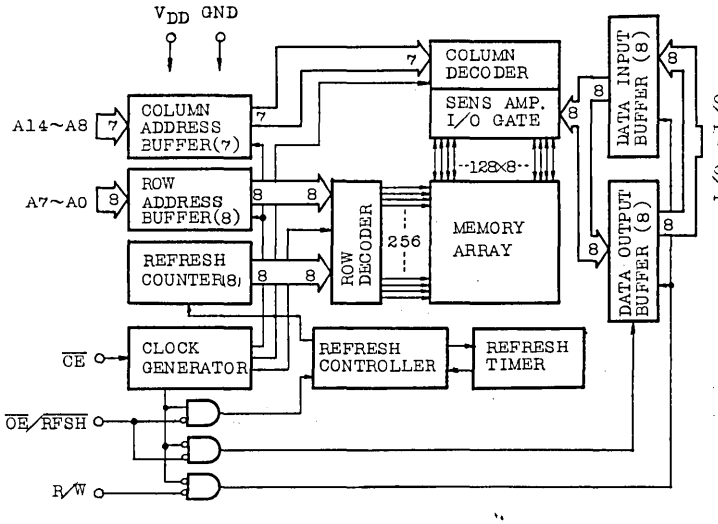
(TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}	Input Voltage	-1.0 ∿ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ∿ 7.0	V	1
V_{DD}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{OPR}	Operating Temperature	0 ∿ 70	°C	1
T_{STG}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec	1
P_D	Power Dissipation	600	mW	1
I_{OUR}	Short Circuit Output Current	50	mA	1

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{DDO}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{CE}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC51832PL-85	-	55	mA	3, 4
		TC51832PL-10	-	45		
		TC51832PL-12	-	40		
I_{DDS1}	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ($\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH})		-	1	mA	
I_{DDS2}	STANDBY CURRENT 2 Power Supply Standby Current, CMOS Level Input ($\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{DD}-0.2V)		-	0.2	mA	
I_{DDF}	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ($\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V)		-	0.2	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ V_{DD}, All Other Inputs not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ V_{DD})		-10	10	μA	
V_{OH}	OUTPUT HIGH LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LOW LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	R/W to Output in Low-Z	0	-	0	-	0	-	ns	
t_{CHZ}	$\overline{CE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHZ}	$\overline{OE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t_{WHZ}	R/W to Output in High-Z	0	20	0	30	0	30	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	

(Continued)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	-	190	-	225	-	ns	13
t_{FSR}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time(Auto Refresh Cycle)	65	-	80	-	95	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	-	8,000	-	8,000	-	ns	13
t_{FRS}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	-	190	-	225	-	ns	13
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ∿ A14)	-	5	pF
CI2	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	-	7	pF
CIO	Input/Output Capacitance (I/O1 ∿ I/O8)	-	7	pF

NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are reference to GND.

3) I_{DDO} depend on cycle rate.

4) I_{DDO} depend on output loading. Specified value are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RESH}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input($\overline{OE}$) and refresh control input(RFSH) under the condition of that $\overline{CE}$=V_{IL} and $\overline{CE}$=V_{IH}, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).

12) All address are latched at the falling edge of $\overline{CE}$. Therefore must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are determind by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}$=V_{IH}.

    Auto refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\leqq t_{FAP}$(max.)

    Self refresh: $\overline{OE}/\overline{RFSH}$ pulse width $\geqq t_{FAS}$(min.)

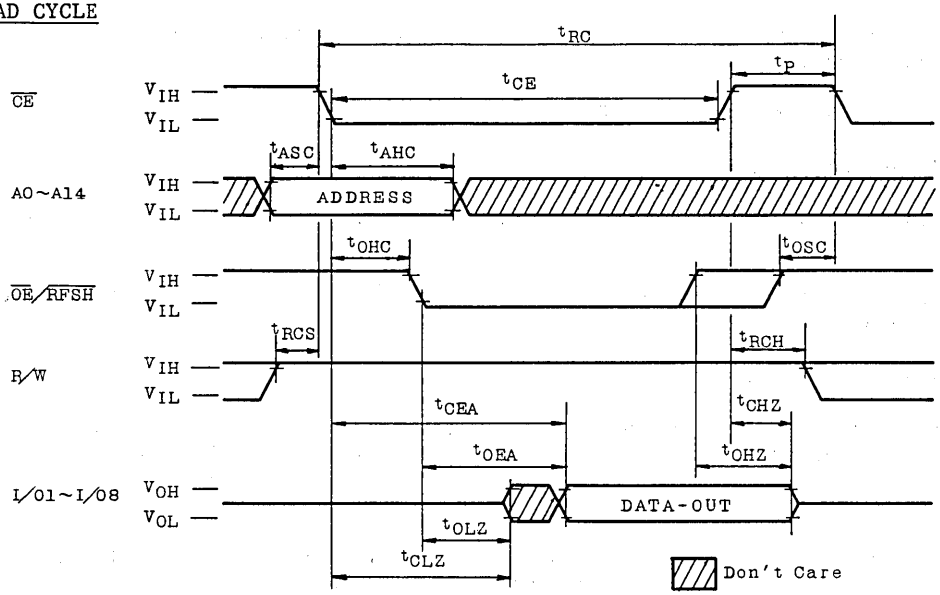
    The following timing parameter must be kept before device proper operatio is achieved after refresh.

    Auto refresh: t_{FCE} and t_{FSR}

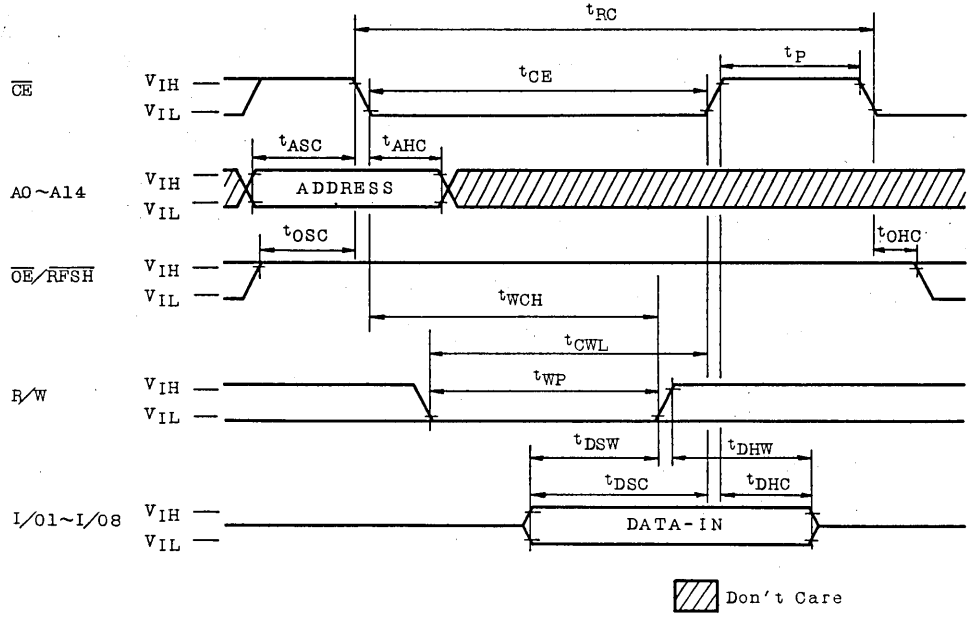
    Self refresh: t_{FRS}

TIMING CHART

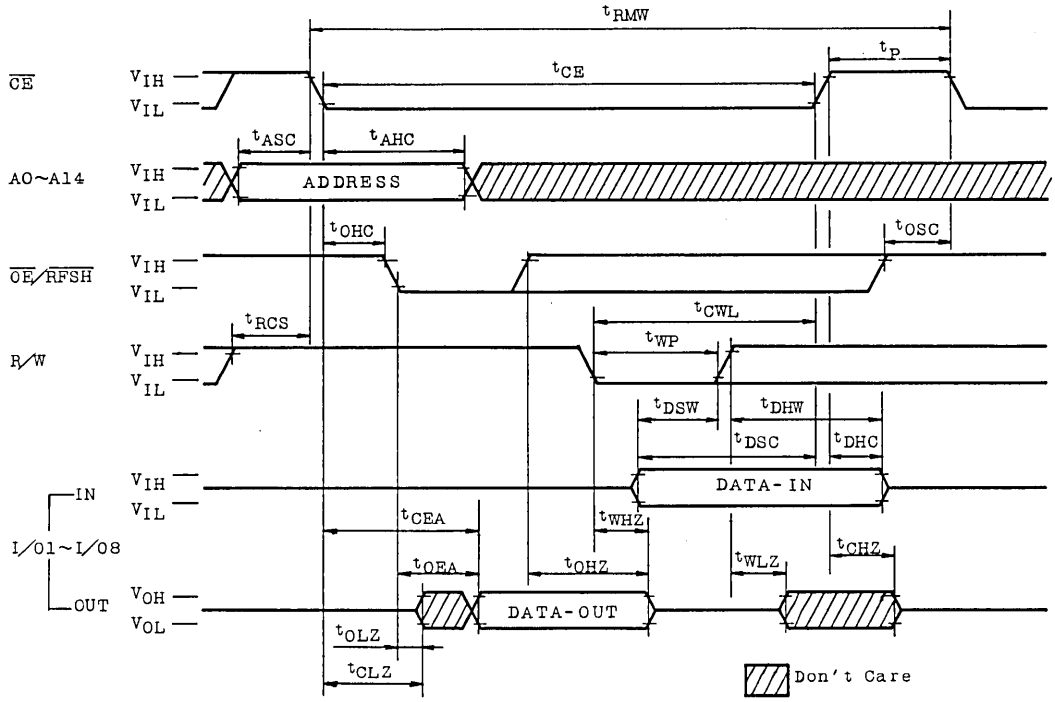
READ CYCLE



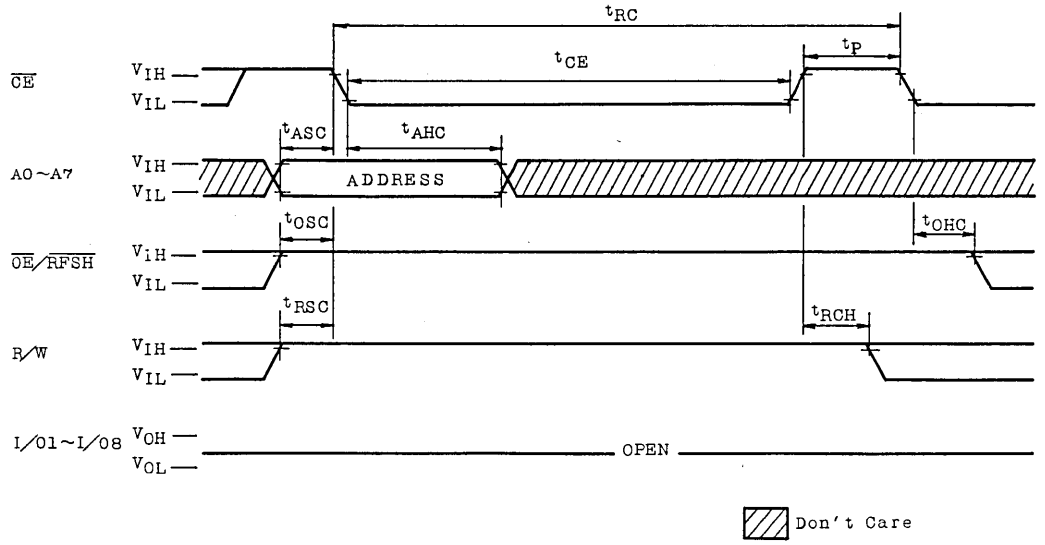
WRITE CYCLE



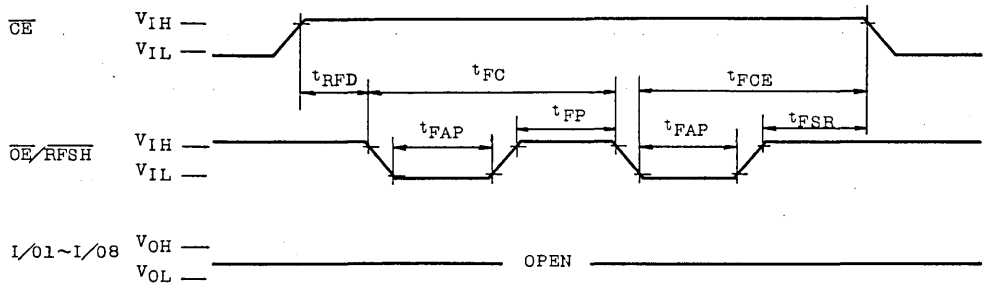
READ WRITE CYCLE



$\overline{CE}$ ONLY REFRESH CYCLE

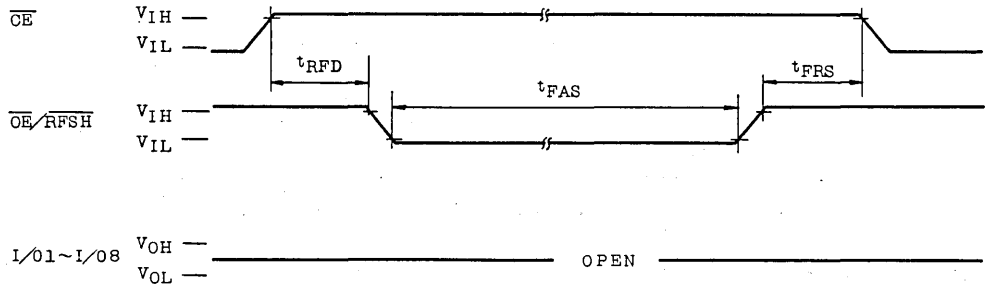


AUTO REFRESH CYCLE



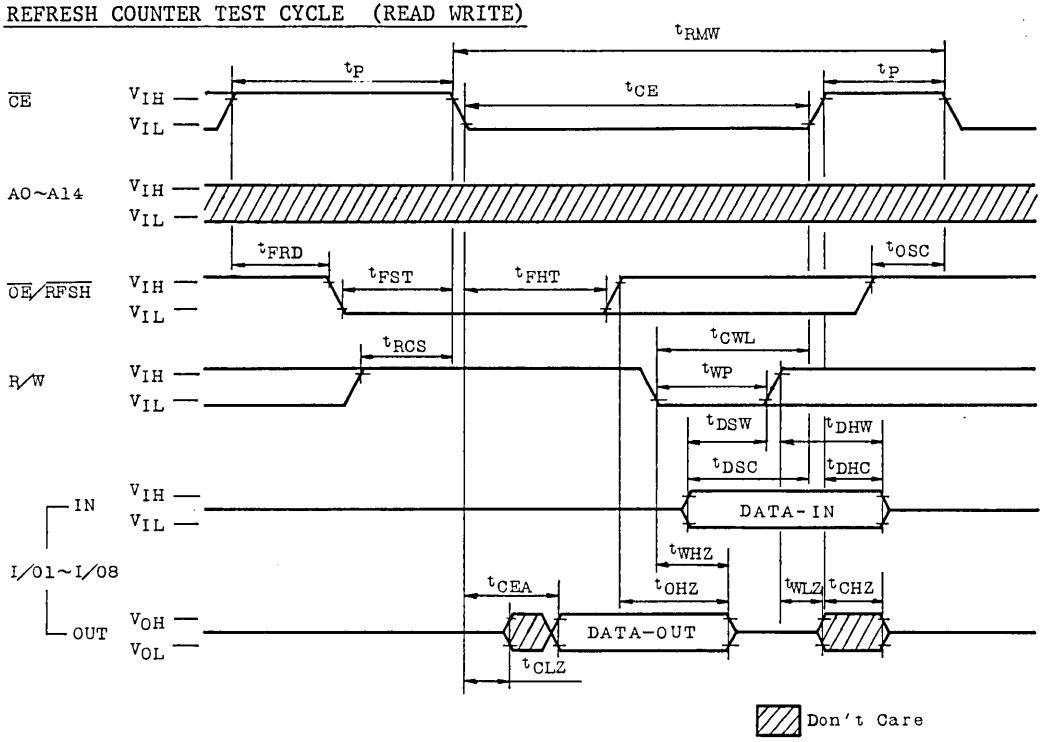
Note) A0~A14, R/$\overline{W}$=Don't Care

SELF REFRESH CYCLE



Note) A0~A14, R/$\overline{W}$=Don't Care

REFRESH COUNTER TEST CYCLE (READ WRITE)



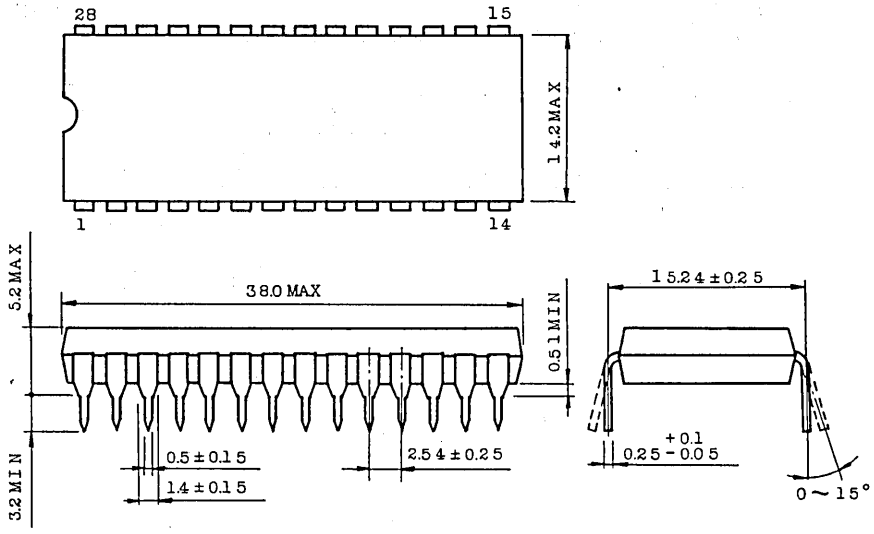
REFRESH COUNTER TEST

The internal refresh operation of TC51832PL can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.
The test procedure is as follows.

① Write "0" into all the memory cells at normal wirte mode.
② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (6D28A-P)

Unit in mm



NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads. All dimensions are in millimeters.