PRELIMINARY

262,144 WORD X 16 BIT DYNAMIC RAM

Description

The TC51V4265DFTS is the new generation dynamic RAM organized 262,144 word by 16 bits. The TC51V4265DFTS utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC51V4265DFTS to be packaged in a standard 44/40 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 262,144 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  - 360mW MAX. Operating
  - (TC51V4265DFTS-60)
  - 306mW MAX. Operating
  - (TC51V4265DFTS-70)
  - 0.8mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Self Refresh, and Hyper Page Mode (EDO) capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/64ms
- Package TC51V4265DFTS: TSOP44-P-400B

Note: For packaging details see Mechanical Dimensions section.

Key Parameters

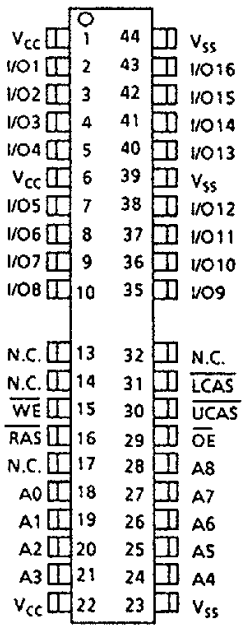
ITEM		TC51V4265DFTS	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Name

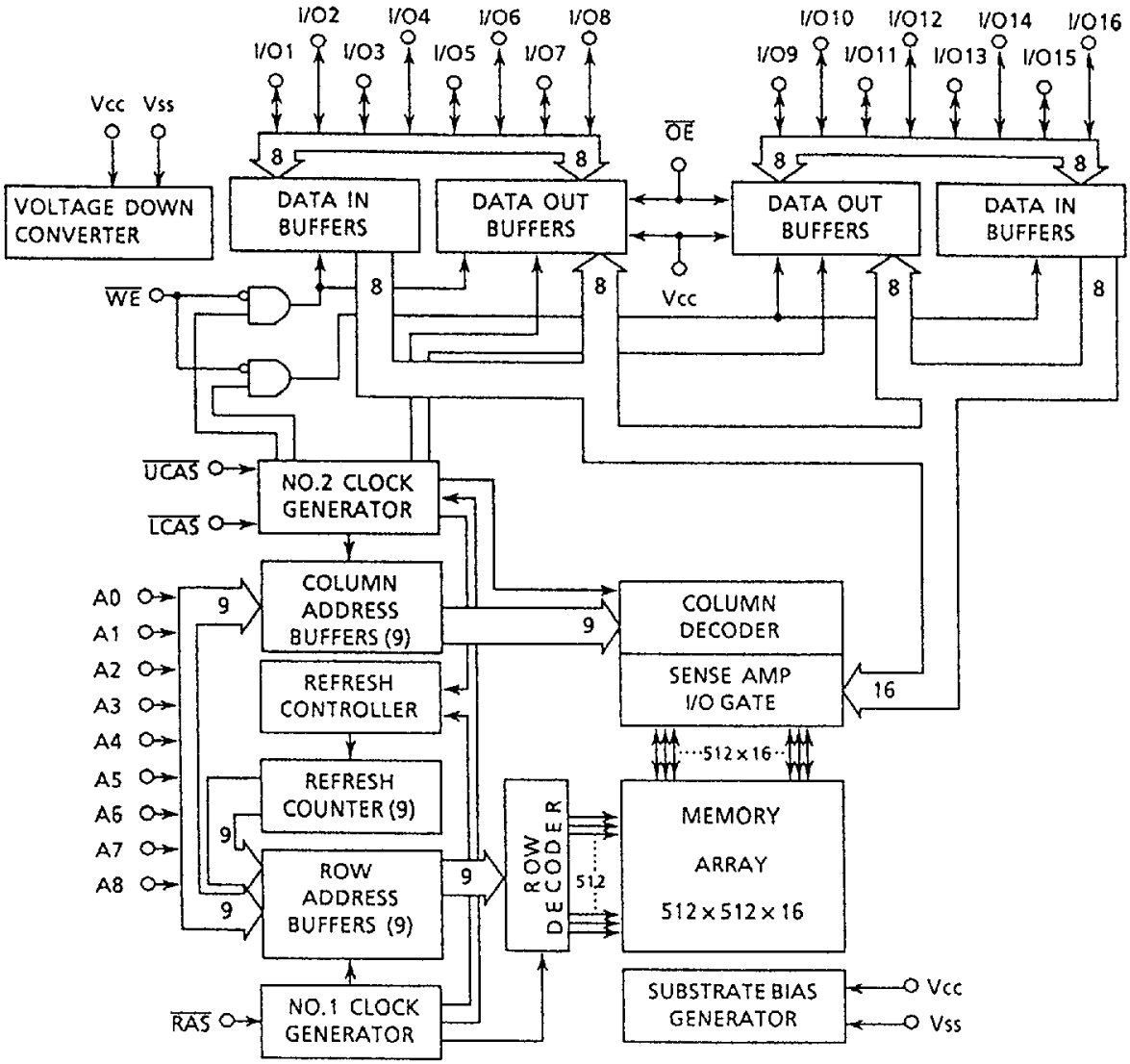
A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 ~ I/O16	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
N.C.	No Connection

Pin Connection (Top View)

Plastic TSOP
(Normal Bend Type)



Block Diagram



Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-0.3~V_{CC}+0.3	V	1
Output Voltage	V_{OUT}	-0.3~V_{CC}+0.3	V	1
Power Supply Voltage	V_{CC}	-0.3~4.6	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	500	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC} + 0.3*	V	2
V_{IL}	Input Low Voltage	-0.3**	-	0.8	V	2

*V_{CC} + 1.2V at pulse width ≤ 20ns (pulse width is measured at V_{CC})
**-1.2V at pulse width ≤ 20ns (pulse width is measured at V_{SS})

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC51V4265DFTS-60	-	100	mA	3,4 5
		TC51V4265DFTS-70	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$=$\overline{LCAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC51V4265DFTS-60	-	100	mA	3, 5
		TC51V4265DFTS-70	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC51V4265DFTS-60	-	70	mA	3,4 5
		TC51V4265DFTS-70	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$= V_{CC}-0.2V)			200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC51V4265DFTS-60	-	100	mA	3, 5
		TC51V4265DFTS-70	-	85		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery Back Up Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$ or $\overline{LCAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, A0~A8=V_{CC}-0.2V or 0.2V, I/O1~I/O18 = V_{CC} - 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~ 1µs)		-	300	µA	3, 6
I_{CCS}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$= V_{IL},$\overline{OE}$, $\overline{WE}$, A0~A8=V_{CC}-0.2V or 0.2V, I/O1~I/O18 = V_{CC} - 0.2V, 0.2V or OPEN)		-	250	µA	
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (0V≤V_{OUT}≤V_{CC})		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-2mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=2mA)		-	0.4	V	

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C) (Notes 7,8,9)

SYMBOL	PARAMETER	TC51V4265DFTS				UNIT	NOTE
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	ns	
t_{RMW}	Read-Modify-Write Cycle	134	-	157	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	30	-	35	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	11
t_T	Transition Time (Rise and Fall)	1	50	1	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	10	-	12	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Hyper Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	12	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	45	14	50	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	12	35	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	10	-	12	-	ns	

Capacitance (V_{CC} = 3.3V ± 0.3V, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	
C_O	Input Capacitance (I/O1~I/O16)	-	7	

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC51V4265DFTS				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	12	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	12	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	12	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time referenced to $\overline{RAS}$	10	-	12	-	ns	13
t_{REF}	Refresh Period	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	34	-	39	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	79	-	89	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	49	-	54	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	54	-	59	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	0	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	10	-	10	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{RNCD}	$\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode)	60	-	70	-	ns	
t_{HPC}	Hyper Page Mode Cycle Time	25	-	30	-	ns	
t_{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	68	-	75	-	ns	
$t_{H\ CAC}$	Access Time from $\overline{CAS}$ (Hyper Page Mode)	–	20	–	25	ns	
t_{HCWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Hyper Page Mode)	39	-	44	-	ns	
t_{COH}	Output Data Hold Time	5	-	5	-	ns	
t_{REZ}	Output buffer turn off Delay Time from $\overline{RAS}$	0	15	0	15	ns	11, 17
t_{WEZ}	Output buffer turn off Delay Time from $\overline{WE}$	0	15	0	15	ns	11
t_{WED}	$\overline{WE}$ to Data Delay	15	-	15	-	ns	
t_{OE}	$\overline{OE}$ Pulse Width	15	-	20	-	ns	
t_{OEP}	$\overline{OE}$ Precharge Time	10	-	12	-	ns	
t_{CPO}	$\overline{CAS}$ to $\overline{OE}$ Precharge Time	5	-	5	-	ns	

Note: Please refer to Timing Diagrams Number 1.

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}$=V_{IL}. In case of I_{CC4}, it can be changed once or less during a Hyper page mode cycle (t_{HPC}).
6. t_{RAS} (max.) = 1µs is only applied to refresh of battery back-up. t_{RAS} (max.) = 10µs is applied to functional operating.
7. An initial pause of 500µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T=2ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. This parameter is measured with a load equivalent to 1 LVTTL load and 100pF at V_{OH} = 2.0V (I_{OUT} = -2mA), V_{OL} = 0.8V (I_{OUT} = 2mA).
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$, leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
17. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going (t_{OFF}). If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going (t_{REZ}).

Data Out Hi-Z Control Logic

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"H"		"L"	"H"	t_{OFF}
	"H"	"L"	"H"	t_{REZ}
"L"	"L"		"H"	t_{OEZ}
"L"	"H"	"L"		t_{WEZ}

Data Out Lo-Z Control Logic

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
"L"		"L"	"H"	t_{CLZ}
"L"	"L"		"H"	t_{OLZ}
"L"	"L"		"H"	t_{OLZ}