TOSHIBA MOS MEMORY PRODUCT

2M BIT (256K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC532000P

DESCRIPTION

The TC532000P is a 2,097, 152 bits read only memory organized as 262, 144 words by 8 bits with a low bit cost thus being suitable for use in program memory of microprocessor, especially character generator. The TC532000P using CMOS technoloby is most suitable for low power applications where battery operation is required.

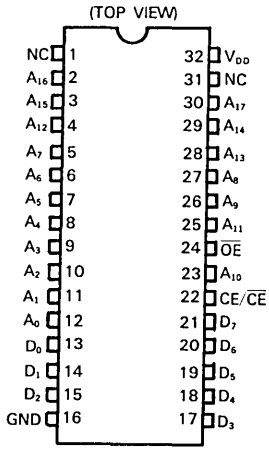
The TC532000P has one programmable chip enable input $\overline{CE}$/CE for device selection, and one output enable input $\overline{OE}$ for fast memory access and output control.

The TC532000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

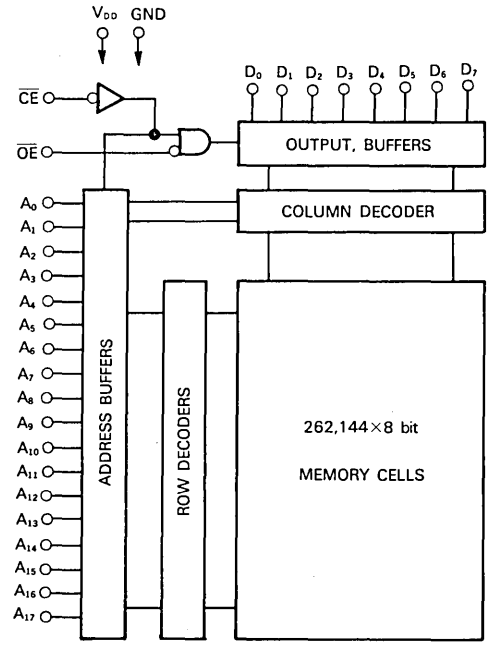
FEATURES

- Single 5V Power Supply
- Access Time: 200ns(Max.)
- Power Dissipetion
  - Operating Current : 30mA(Max.)
  - Standby Current : 20uA(Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32pin 600mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A_0~A_{17}	Address inputs
D_0~D_7	Data outputs
$\overline{OE}$	Output Enable input
$\overline{CE}$/CE	Chip enable input
N.C.	No Conuection
V_{DD}	Power supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	−55~150	°C
T_{ORR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note: *Plastic FP

D.C. OPERATING CONDITIONS

(Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

D.C. and OPERATING CHARACTERISTICS

(Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	—	±1.0	uA
I_{LO}	Output Leakage Cunnent	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_{OUT} = OV~V_{DD}	—	±5.0	uA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	—	5	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} and V_{IN} = OV (V_{DD})	—	20	uA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 200ns, I_{OUT} = 0mA	—	40	mA
I_{DDO2}		V_{IN} = V_{DD}/OV, t_{cycle} = 200ns, I_{OUT} = 0mA	—	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	—	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

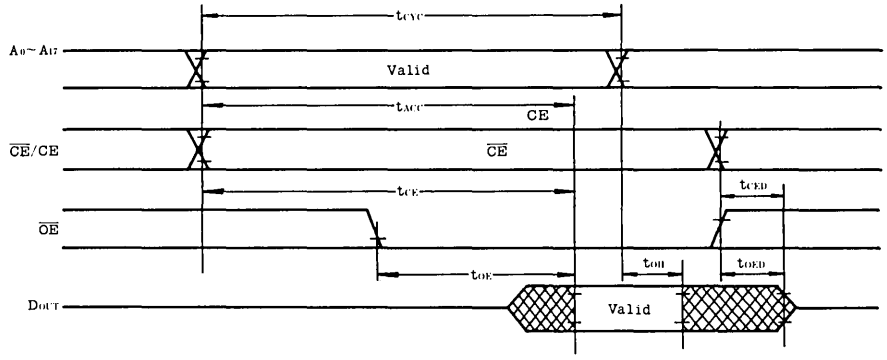
($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{CE}	Chip Enable Access Time	—	200	ns
t_{OE}	Output Enable Access Time	—	70	ns
t_{CED}, t_{OED}	Output Disable Time	0	60	ns
t_{OH}	Output Hold Time	0	—	ns

AC TEST CONDITIONS

Output Load : 100pF+1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.0V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



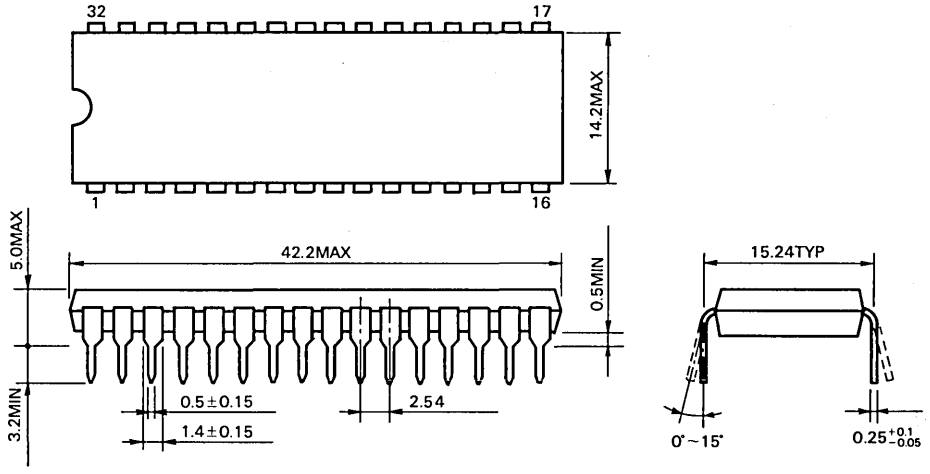
OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A_0-A_{17}	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Unit : mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.