

TC551001BPL/BFL/BFTL/BTRL-70L/85L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bit CMOS static random access memory organized as 131,072 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2 μ A typically. The TC551001BPL has three control inputs. Chip enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an output enable input (\overline{OE}) provides fast memory access. The TC551001BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4 μ A (max.) at Ta = 25°C
- Single 5V power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL		
	-70L	-85L	-10L
Access Time	70ns	85ns	100ns
$\overline{CE1}$ Access Time	70ns	85ns	100ns
CE2 Access Time	70ns	85ns	100ns
\overline{OE} Access Time	35ns	45ns	50ns

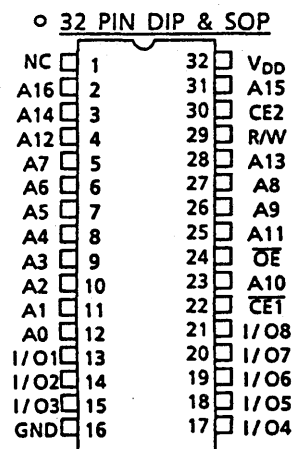
- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC551001BPL : DIP32-P-600
 - TC551001BFL : SOP32-P-525
 - TC551001BFTL : TSOP32-P-0820
 - TC551001BTRL : TSOP32-P-0820A

Pin Names

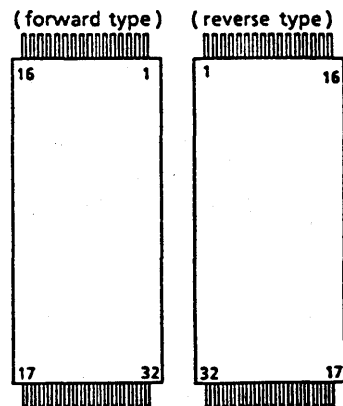
A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A ₁₀	\overline{OE}

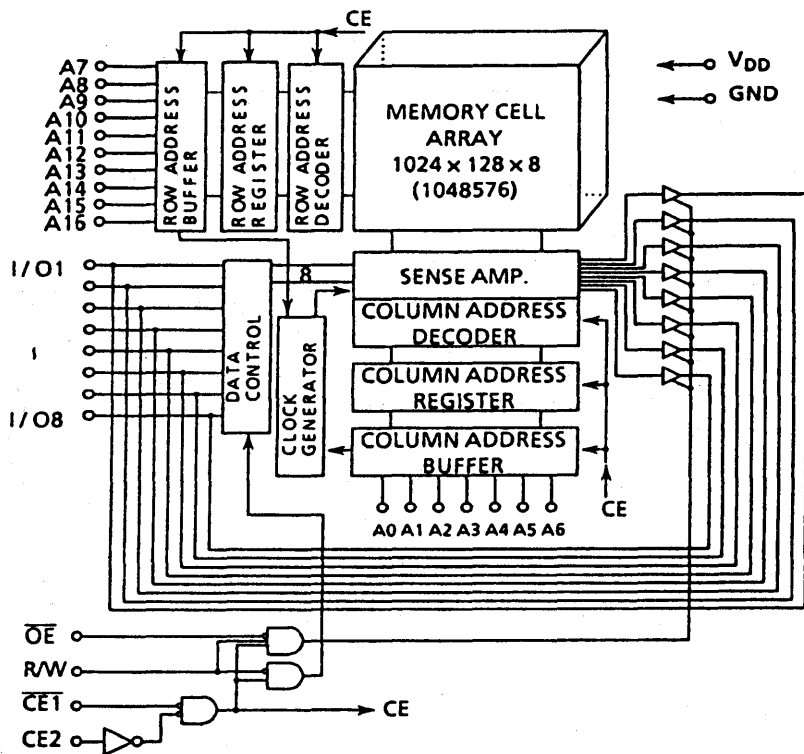
Pin Connection (Top View)



o 32 PIN TSOP



Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE1}$	CE2	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDs}
	*	L	*	*	High-Z	I _{DDs}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	±1.0	μA		
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	–	–	±1.0	μA		
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	–	–	mA		
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	–	–	mA		
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0mA$ Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
I_{DDO2}				1μs	–	–	20	
	I_{DDO2}	$\overline{CE1} = 0.2V$ and $CE2 = V_{DD} - 0.2V$ $R/W = V_{DD} - 0.2V$ $I_{OUT} = 0mA$ Other Inputs $= V_{DD} - 0.2V/0.2V$	t_{cycle}	Min.	–	–	60	
1μs				–	–	10		
I_{DSS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	–	–	–	3	mA	
$I_{DSS2}^{(1)}$		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	Ta = 0 ~ 70°C		–	–	30	μA
		Ta = 25°C		–	2	4		

Note (1): If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t_{ACC}	Address Access Time	–	70	–	85	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	–	100	
t_{CO2}	$CE2$ Access Time	–	70	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, $CE2$) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, $CE2$) to Output in High-Z	–	25	–	30	–	35	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

Write Cycle

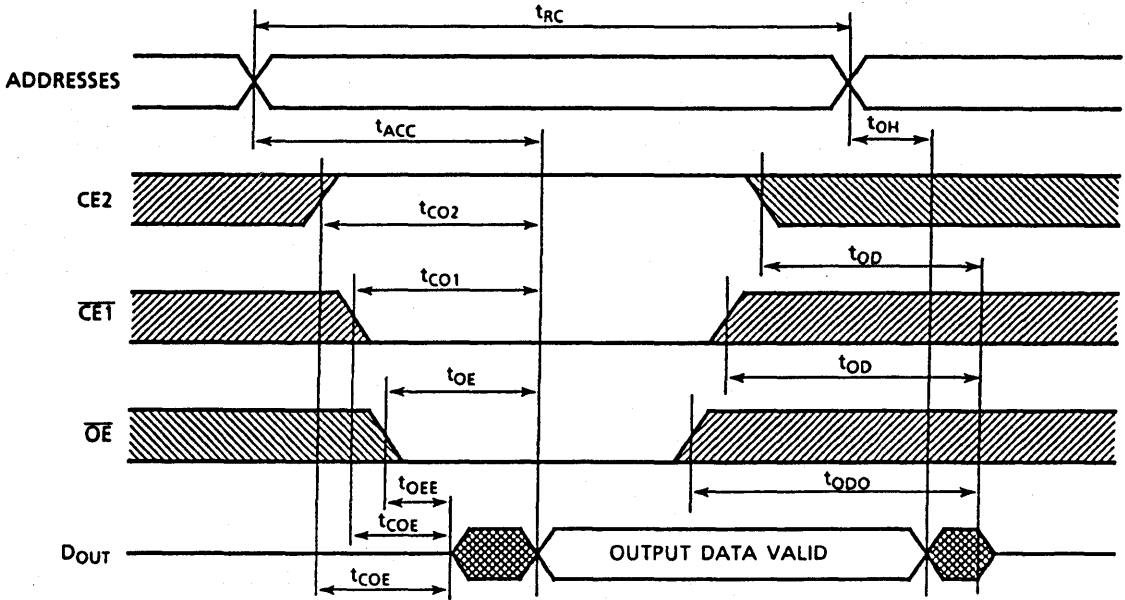
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL						UNIT
		-70L		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	–	35	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC Test Conditions

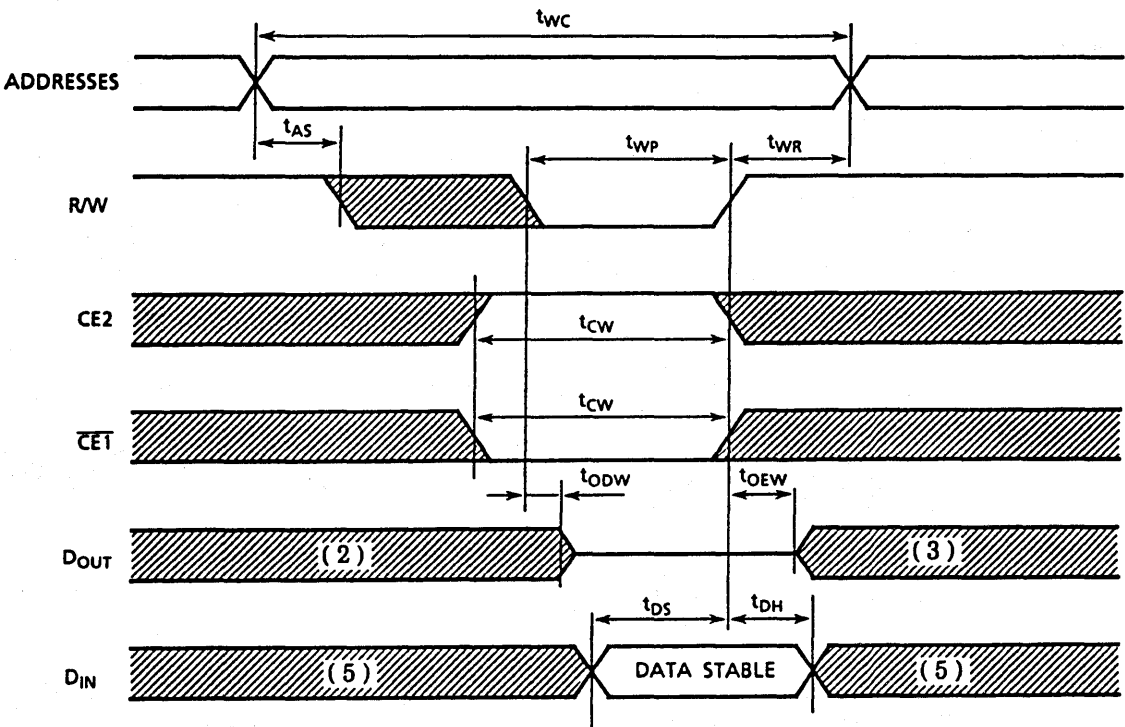
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

Timing Waveforms

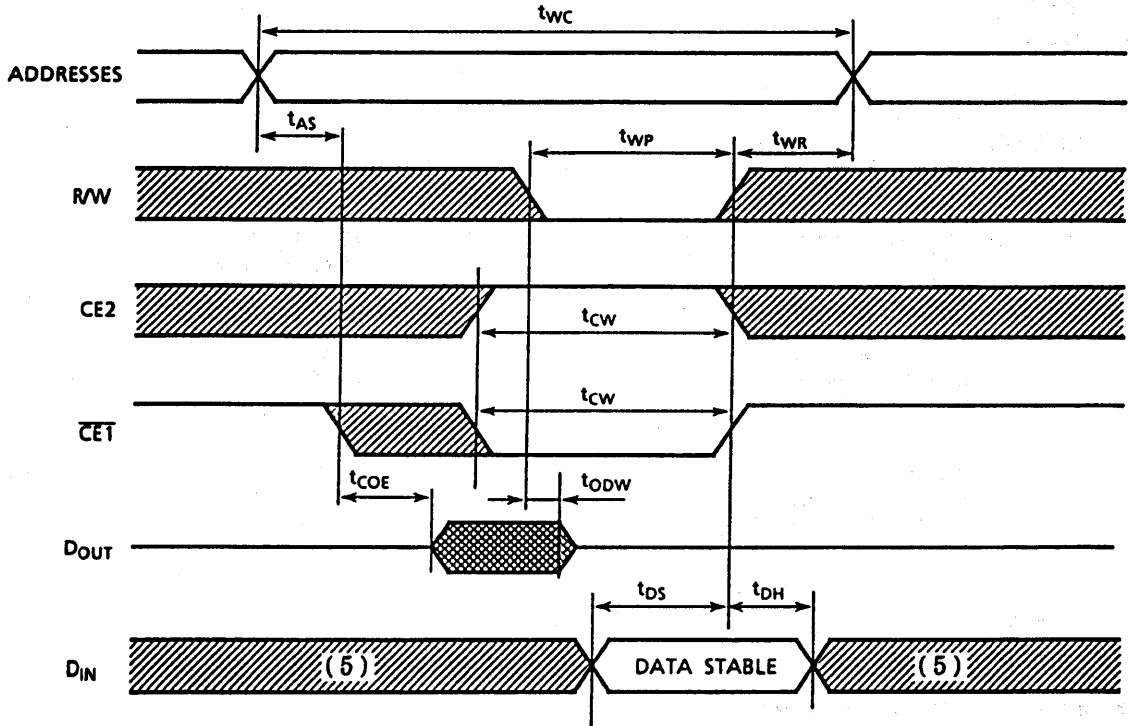
Read Cycle ⁽¹⁾



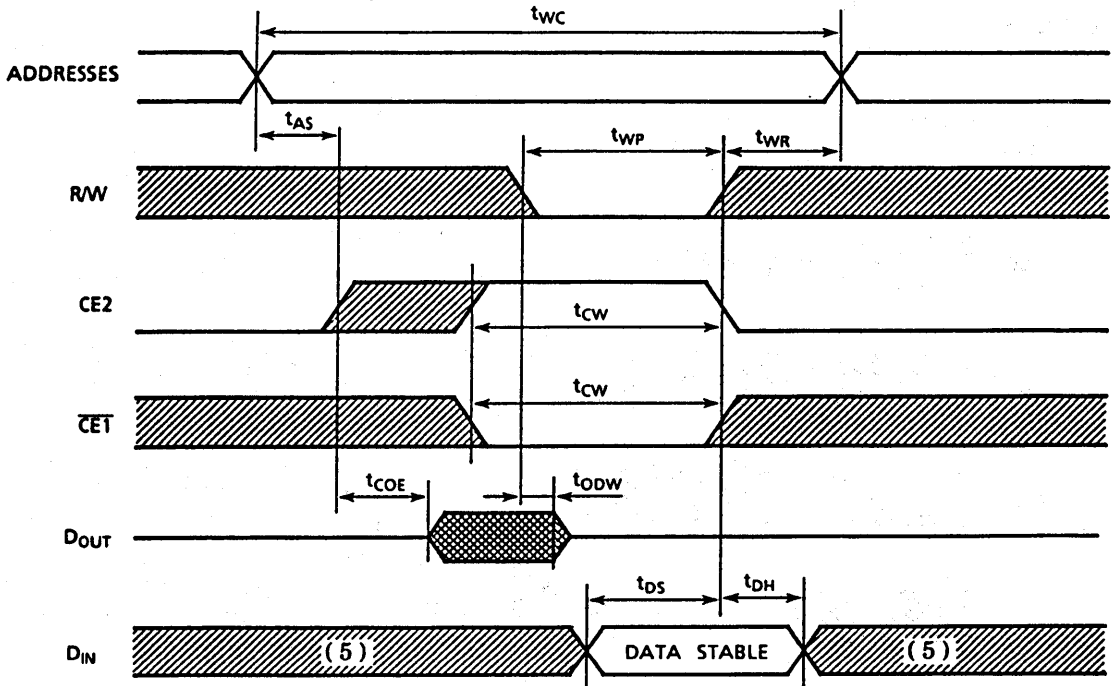
Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE1}}$ Controlled Write)



Write Cycle 3 ⁽⁴⁾ (CE2 Controlled Write)



Notes:

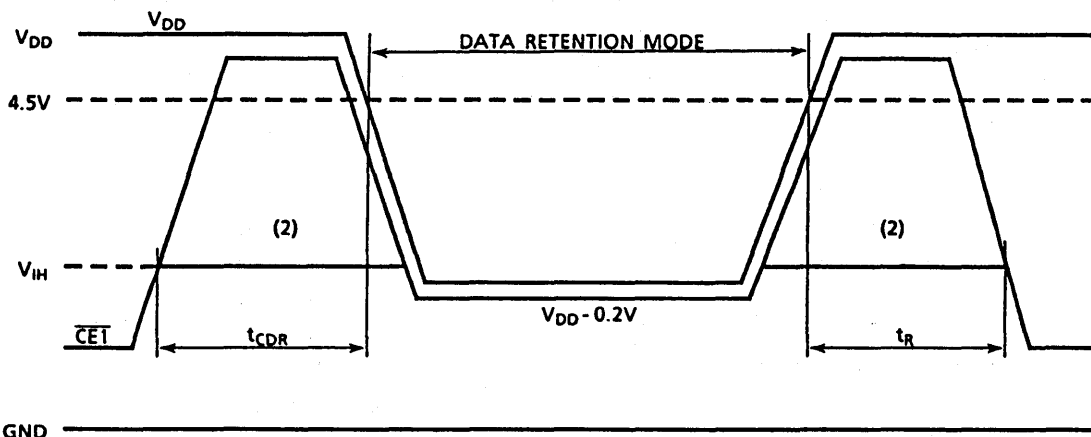
1. R/W is high for read cycles.
2. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

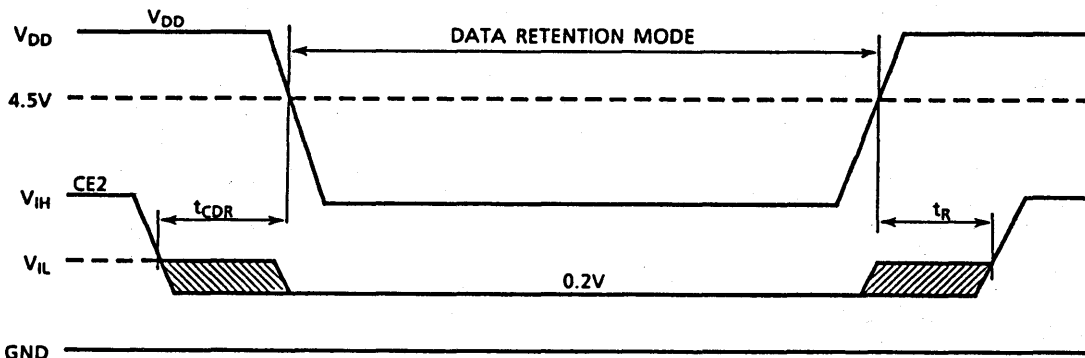
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I _{DSS2}	Standby Current				μA
		V _{DH} = 3.0V	—	15*	
		V _{DH} = 5.5V	—	30	
t _{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t _R	Recovery Time	5	—	—	ms

*3μA (max.) Ta = 0 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode ⁽¹⁾



CE2 Controlled Data Retention Mode ⁽³⁾



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DSS1} current flows.
3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition $CE2 \leq 0.2V$.