4,194,304 WORD x 1 BIT/1,048,576 WORD x 4 BIT CMOS STATIC RAM

Description

The TC551402J is a 4,194,304 bit high speed CMOS static random access memory that is configurable to an organization of either 4,194,304 words by 1 bit or 1,048,576 words by 4 bits when power is initially applied to the device. The mode (x1/x4) is selected by the input level of pin 17 (B1/$\overline{B4}$). The TC551402J operates from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551402J features low power dissipation when the SRAM is deselected using chip enable ($\overline{CE}$), and has an output enable input ($\overline{OE}$) for fast memory access. It is suitable for use in high speed applications such as cache memory, high speed storage, and main memory. All inputs and outputs are TTL compatible.

The TC551402J is available in a 32-pin, 400mil SOJ package suitable for high density assembly.

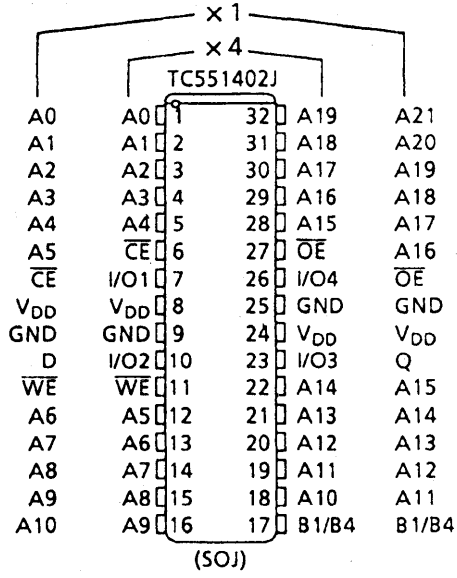
Features

- Fast access time
  - TC551402J-20 20ns (max.)
  - TC551402J-25 25ns (max.)
  - TC551402J-30 30ns (max.)
- Low power dissipation
  - Operation:
  - TC551402J-20 160mA (max.)
  - TC551402J-25 160mA (max.)
  - TC551402J-30 150mA (max.)
  - Standby: 10mA (max.)
- Fully static operation
- Single power supply: 5V±10%
- Output buffer control: $\overline{OE}$
- Inputs and outputs TTL compatible
- Separate data I/O (x1 mode)
- Common data I/O (x4 mode)
- Package
  - TC551402J: SOJ32-P-400A

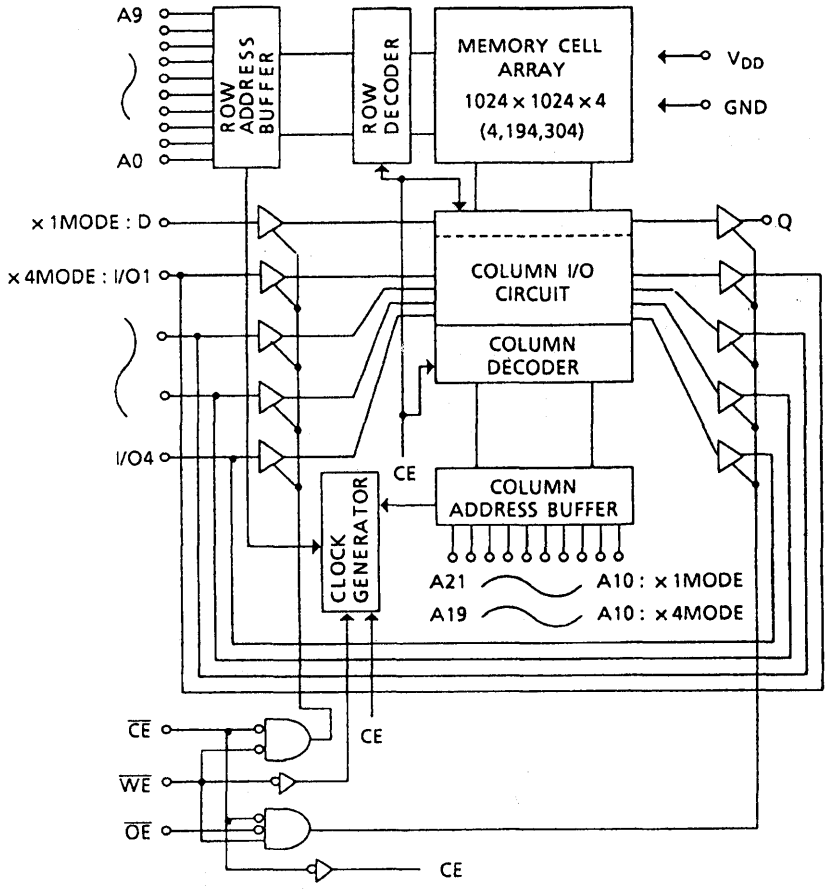
Pin Names

A0 ~ A21	Address Inputs
I/O1 ~ I/O4	Data Inputs/Outputs
D	Data Input
Q	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
B1/$\overline{B4}$	Bit Select (x1/x4)

Pin Connection (Top View)



Block Diagram



Operating Mode

The memory organization of the TC551402J can be selected to be either 4M words by 1 bit or 1M word by 4 bits. The configuration must be selected when power is initially applied to the device using pin 17 (B1/$\overline{B4}$). Changing the state of this pin is prohibited after power up. The 4M word by 1 bit mode is selected if B1/$\overline{B4}$ is high, the 1M word by 4 bit mode is selected if B1/$\overline{B4}$ is low.

MODE		B1/$\overline{B4}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
x1 MODE	Read	H	L	L	H	D_{OUT}	I_{DDO}
	Write	H	L	*	L	D_{IN}	I_{DDO}
	Output Disabled	H	L	H	H	High-Z	I_{DDO}
	Standby	H	H	*	*	High-Z	I_{DDS}
x4 MODE	Read	L	L	L	H	D_{OUT}	I_{DDO}
	Write	L	L	*	L	D_{IN}	I_{DDO}
	Output Disabled	L	L	H	H	High-Z	I_{DDO}
	Standby	L	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
V_{OUT}	Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -3V with pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0~V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, Other Inputs = V_{IH}/V_{IL}	-20	–	–	160	mA
			-25	–	–	160	
			-30	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V, Other Inputs = V_{DD} -0.2V or 0.2V		–	–	10	mA

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	8	pF
$C_{I/O}$, C_{OUT}	I/O, Output Capacitance	V_{OUT} = GND	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C [1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551402J-20		TC551402J-25		TC551402J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	ns
t_{ACC}	Address Access Time	–	20	–	25	–	30	
t_{CO}	Chip Enable Access Time	–	20	–	25	–	30	
t_{OE}	Output Enable Access Time	–	10	–	12	–	14	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{ODO}	Output Disable Time From $\overline{OE}$	–	8	–	10	–	12	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	20	–	25	–	30	

Write Cycle

SYMBOL	PARAMETER	TC551402J-20		TC551402J-25		TC551402J-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	–	25	–	30	–	ns
t_{WP}	Write Pulse Width	11	–	13	–	15	–	
t_{AW}	Address Valid to End of Write	17	–	20	–	23	–	
t_{CW}	Chip Enable to End of Write	17	–	20	–	23	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Setup Time	10	–	12	–	14	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	10	–	12	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

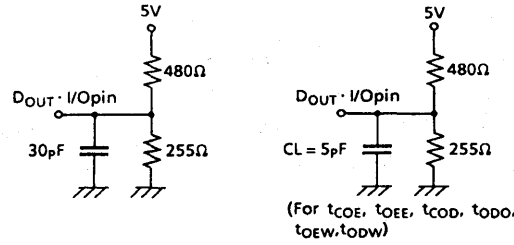
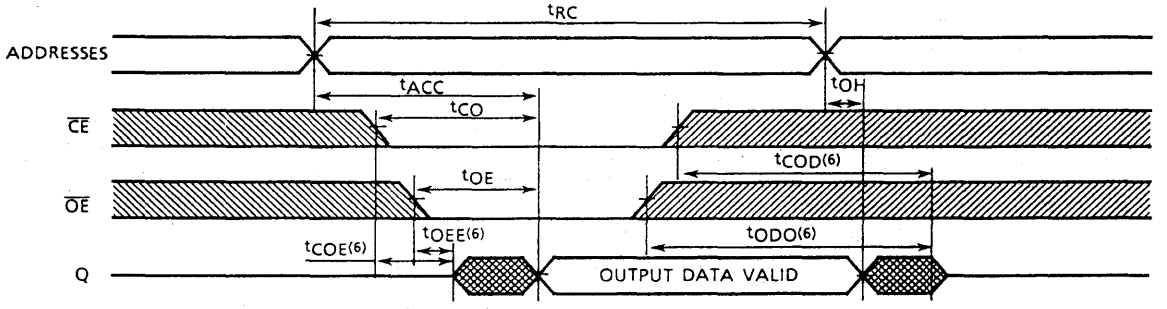


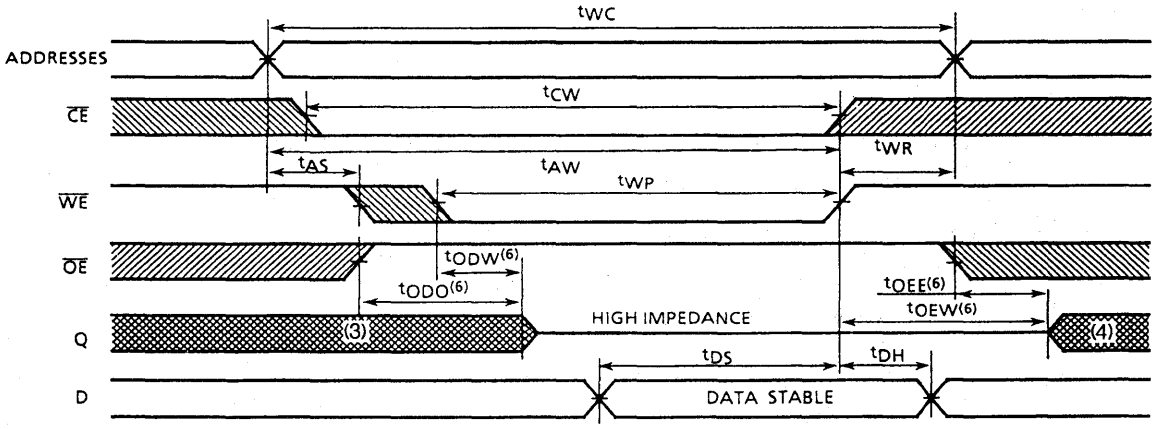
Figure 1.

Timing Waveforms

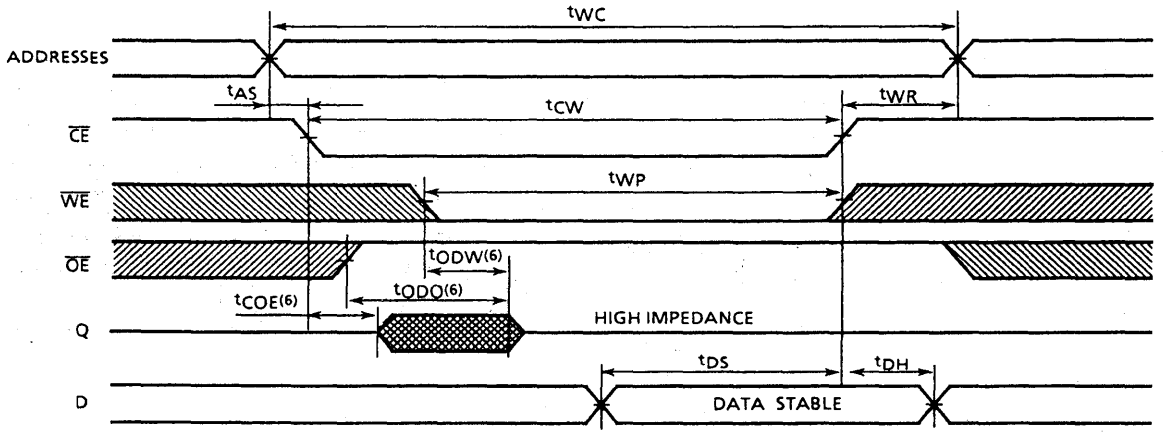
Read Cycle (2)



Write Cycle 1 (5) ($\overline{WE}$ Controlled Write)



Write Cycle 2 [5] ($\overline{CE}$ Controlled Write)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{WE}$ is high for read cycles.
3. If the $\overline{CE}$ low transition occurs coincident with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
4. If the $\overline{CE}$ high transition occurs coincident with or prior to the $\overline{WE}$ high transition, outputs remain in a high impedance state.
5. If $\overline{OE}$ is high during a write cycle, the outputs will be in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time