

SILICON GATE CMOS

32,768 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551632J is a 524,288 bit high speed CMOS static random access memory organized as 32,768 words by 16 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551632J features low power dissipation when the device is deselected using chip enable (\overline{CE}), and has an output enable input (\overline{OE}) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC551632J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551632J is available in a 400mil width, 40-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC551632J-20 20ns (max.)
 - TC551632J-25 25ns (max.)
 - TC551632J-35 35ns (max.)

- Low power dissipation

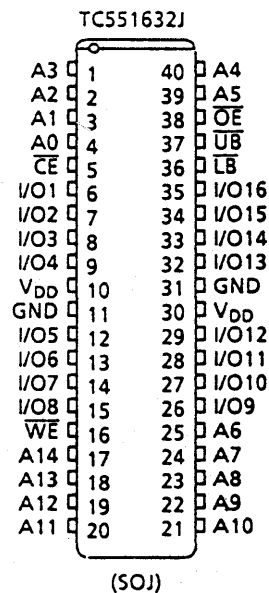
Cycle Time	20	25	35	100	ns
Operation (max.)	220	200	170	130	mA

- Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Data byte controls: \overline{LB} , \overline{UB}
- Package: SOJ40-P-400

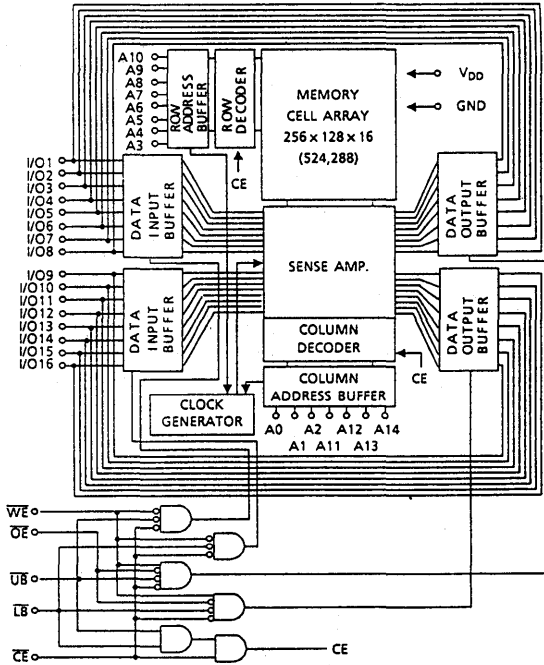
Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB} , \overline{UB}	Data Byte Control Inputs
V_{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	CE	OE	WE	LB	UB	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I _{BDO}
				H	L	High Impedance	Output	I _{BDO}
				L	H	Output	High Impedance	I _{BDO}
Write	L	*	L	L	L	Input	Input	I _{BDO}
				H	L	High Impedance	Input	I _{BDO}
				L	H	Input	High Impedance	I _{BDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I _{BDO}
	L	*	*	H	H	High Impedance	High Impedance	I _{BDS}
Standby	H	*	*	*	*	High Impedance	High Impedance	I _{BDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0* ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 10	μA	
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	–	–	± 10	μA	
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	–	–	mA	
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	–	–	mA	
I_{DDO}	Operating Current	$\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, Other Inputs = V_{IH}/V_{IL}	$t_{\text{cycle}} = 20\text{ns}$	–	–	220	mA
			$t_{\text{cycle}} = 25\text{ns}$	–	–	200	
			$t_{\text{cycle}} = 35\text{ns}$	–	–	170	
			$t_{\text{cycle}} = 100\text{ns}$	–	–	130	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, or $\overline{UB} = \overline{LB} = V_{IH}$ Other Inputs = V_{IH}/V_{IL}	–	–	30	mA	
		$\overline{CE} = V_{DD} - 0.2V$, or $\overline{UB} = \overline{LB} = V_{DD} - 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	–	–	1		

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C⁽¹⁾, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	20	–	25	–	35	–	ns
t _{ACC}	Address Access Time	–	20	–	25	–	35	
t _{CO}	\overline{CE} Access Time	–	20	–	25	–	35	
t _{OE}	\overline{OE} Access Time	–	10	–	12	–	17	
t _{BA}	\overline{UB} , \overline{LB} Access Time	–	20	–	25	–	35	
t _{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t _{COE}	Output Enable Time from \overline{CE}	5	–	5	–	5	–	
t _{OEE}	Output Enable Time from \overline{OE}	1	–	1	–	1	–	
t _{BE}	Output Enable Time from \overline{UB} , \overline{LB}	1	–	1	–	1	–	
t _{COD}	Output Disable Time from \overline{CE}	–	8	–	8	–	8	
t _{ODO}	Output Disable Time from \overline{OE}	–	8	–	8	–	8	
t _{BD}	Output Disable Time from \overline{UB} , \overline{LB}	–	8	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC551632J-20		TC551632J-25		TC551632J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	20	–	25	–	35	–	ns
t _{WP}	Write Pulse Width	10	–	12	–	16	–	
t _{CW}	Chip Enable to End of Write	13	–	15	–	17	–	
t _{BW}	\overline{UB} , \overline{LB} Enable to End of Write	13	–	15	–	17	–	
t _{AW}	Address Valid to End of Write	12	–	14	–	16	–	
t _{AS}	Address Setup Time	0	–	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	0	–	
t _{DS}	Data Setup Time	10	–	10	–	10	–	
t _{DH}	Data Hold Time (\overline{WE})	0	–	0	–	0	–	
t _{DH1}	Data Hold Time (\overline{CE} , \overline{UB} , \overline{LB})	1	–	1	–	1	–	
t _{OEW}	Output Enable Time from \overline{WE}	1	–	1	–	1	–	
t _{ODW}	Output Disable Time from \overline{WE}	–	8	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

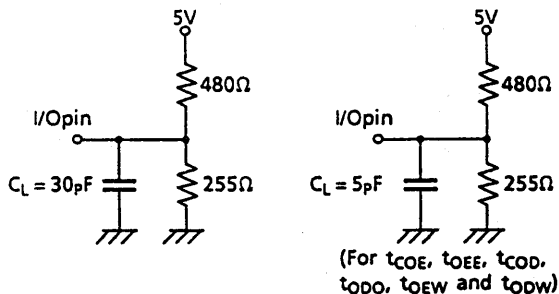
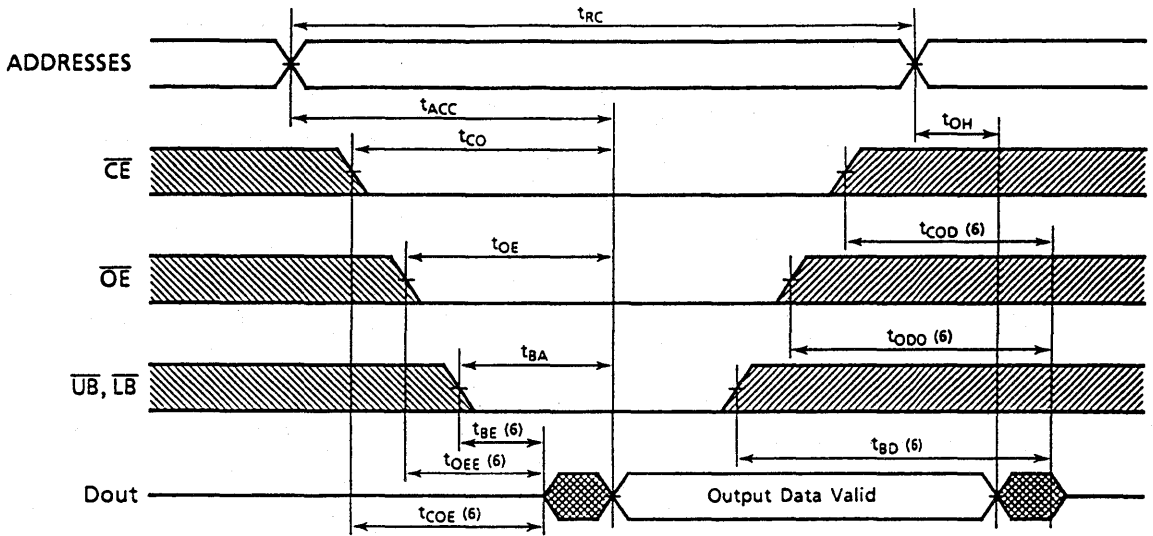


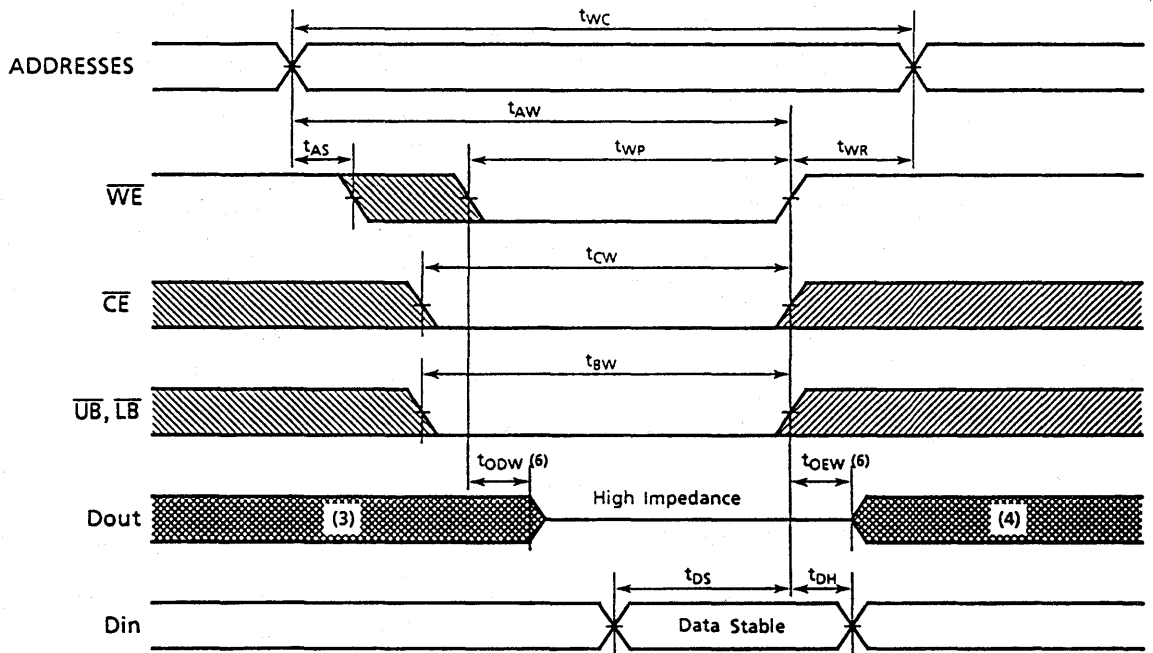
Figure 1.

Timing Waveforms

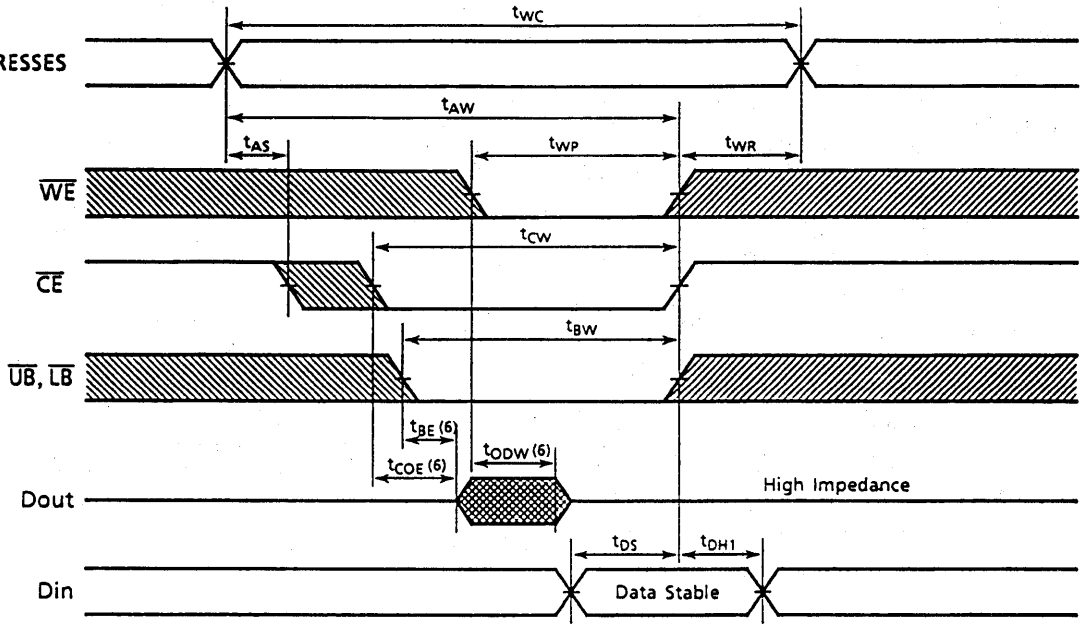
Read Cycle ⁽²⁾



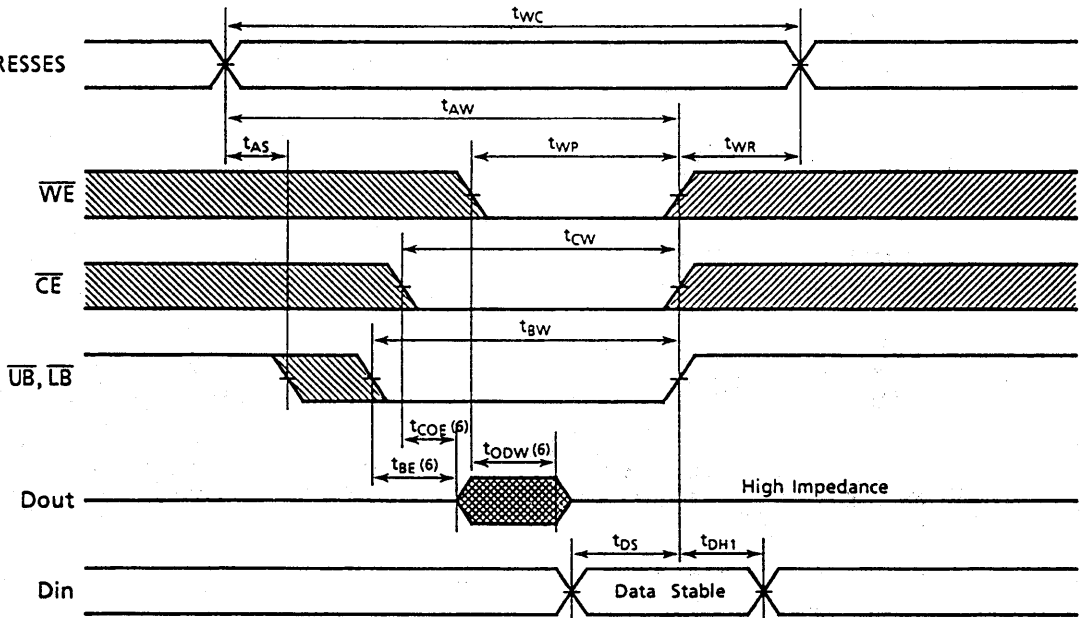
Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled)



Write Cycle 2 ⁽⁵⁾ (\overline{CE} Controlled)



Write Cycle 3 ⁽⁵⁾ ($\overline{UB}, \overline{LB}$ Controlled)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the \overline{CE} low transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the \overline{CE} high transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 (A) t_{COE} , t_{OEE} , t_{BE} , t_{OEw} Output Enable Time
 (B) t_{COD} , t_{ODO} , t_{BD} , t_{ODW} Output Disable Time

