SILICON GATE CMOS

65,536 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551664J is a 1,048,576 bit high speed CMOS static random access memory organized as 65,536 words by 16 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

The TC551664J features low power dissipation when the device is deselected using chip enable ($\overline{CE}$), and has an output enable input ($\overline{OE}$) for fast memory access. Byte access is supported by upper and lower byte controls.

The TC551664J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551664J is available in a 400mil width, 44-pin SOJ suitable for high density surface assembly.

Features

- Fast access time
  - TC551664J -15 15ns (max.)
  - TC551664J -20 20ns (max.)
  - TC551664J -25 25ns (max.)
- Low power dissipation

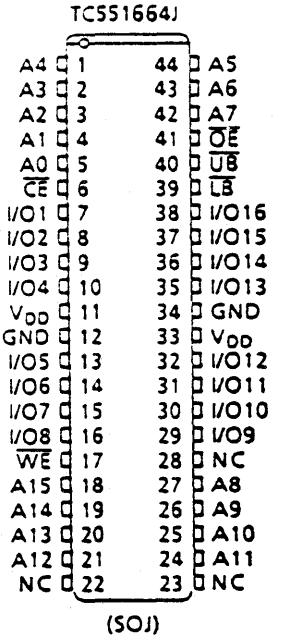
Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

  - Standby: 1mA (max.)
- Single 5V power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Data byte controls: $\overline{LB}$, $\overline{UB}$
- Package: SOJ44-P-400

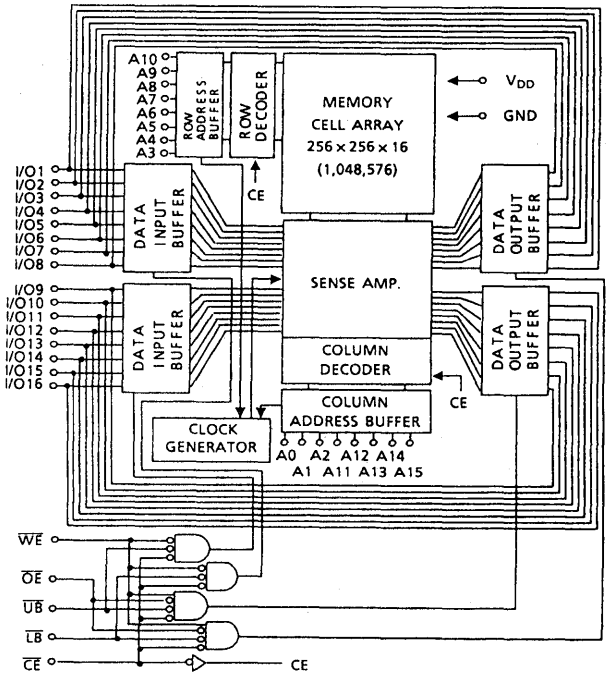
Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	CE	OE	WE	LB	UB	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H	High Impedance	High Impedance	I_{DDO}
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	t_{cycle} = 15ns	–	–	260	mA
			t_{cycle} = 20ns	–	–	220	
			t_{cycle} = 25ns	–	–	200	
			t_{cycle} = 30ns	–	–	180	
			t_{cycle} = 50ns	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C(1), V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551664J -15		TC551664J -20		TC551664J -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	20	–	25	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	–	12	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	–	10	–	12	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC551664J -15		TC551664J -20		TC551664J -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	12	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	9	–	12	–	14	–	
t_{AW}	Address Valid to End of Write	9	–	12	–	14	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

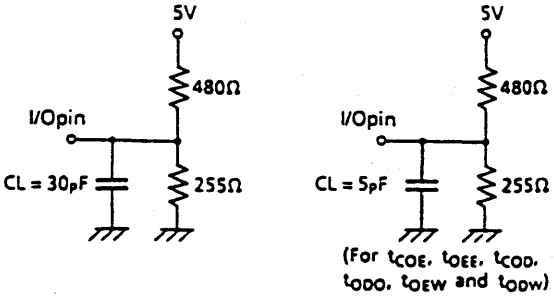
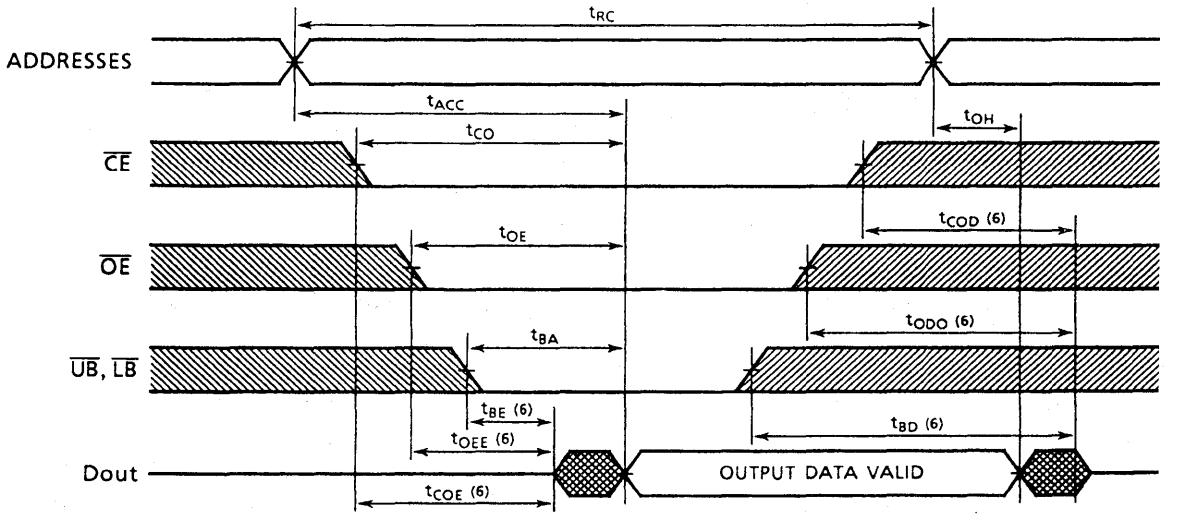


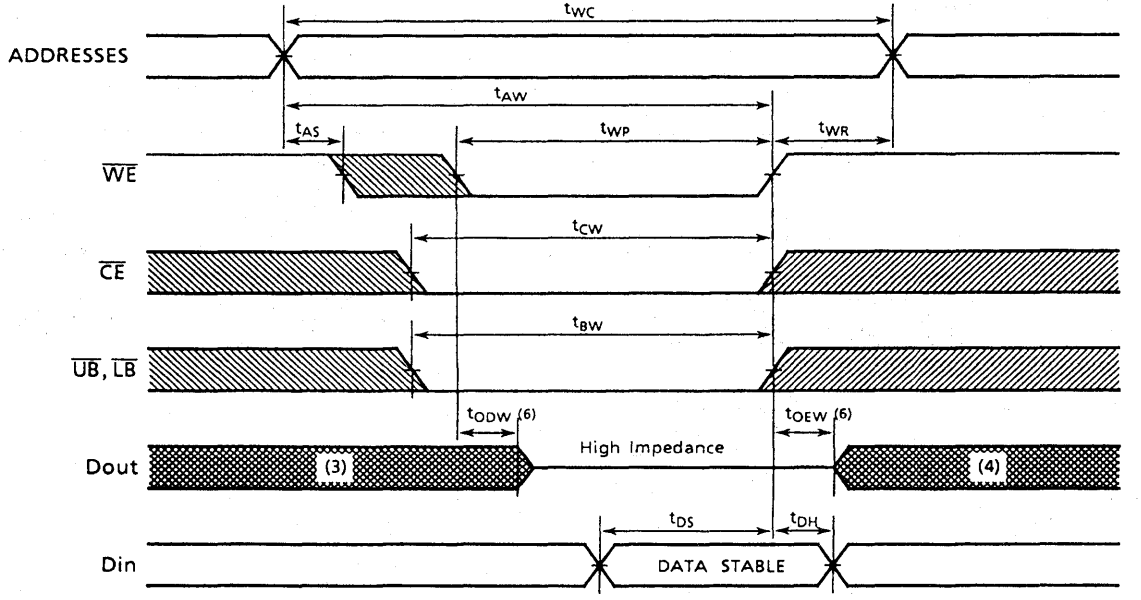
Figure 1.

Timing Waveforms

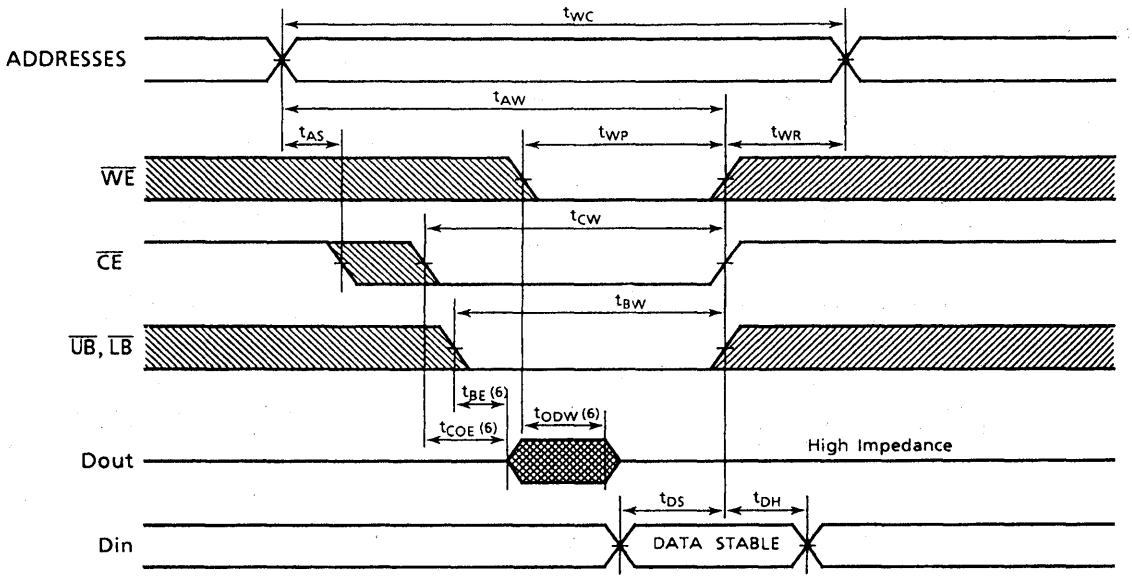
Read Cycle (2)



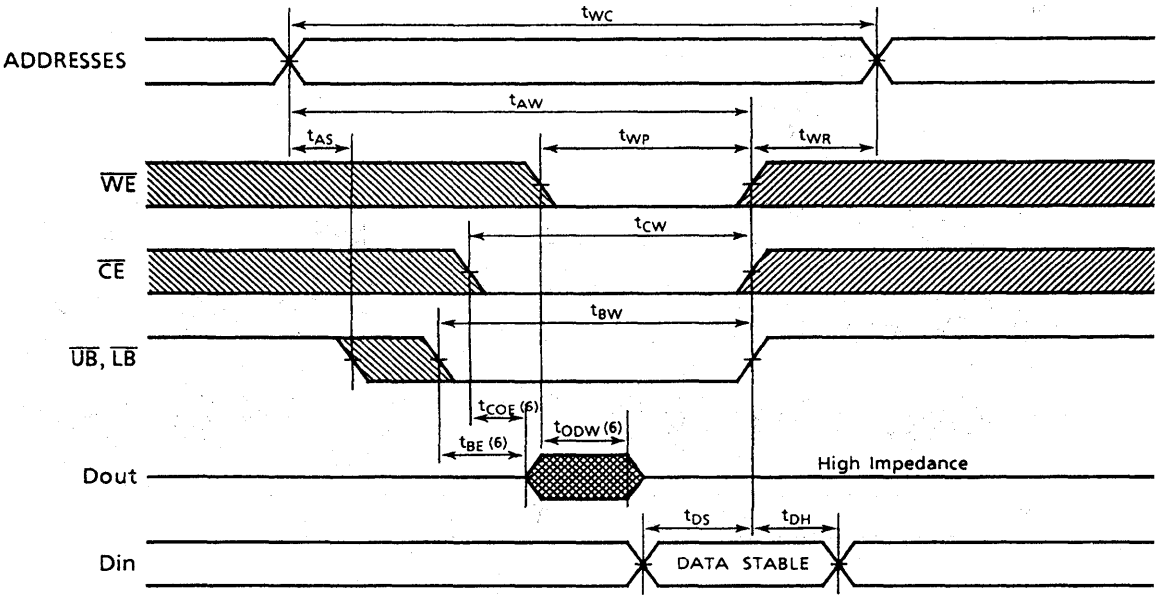
Write Cycle 1 (5) ($\overline{WE}$ Controlled)



Write Cycle 2 [5] ($\overline{CE}$ Controlled)



Write Cycle 3 [5] ($\overline{UB}$, $\overline{LB}$ Controlled)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is high for read cycles.

3. If the $\overline{CE}$ low transition occurs coincident with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

4. If the $\overline{CE}$ high transition occurs coincident with or prior to the $\overline{WE}$ high transition, outputs remain in a high impedance state.

5. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

6. The following parameters are measured using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} . . . . Output Disable Time